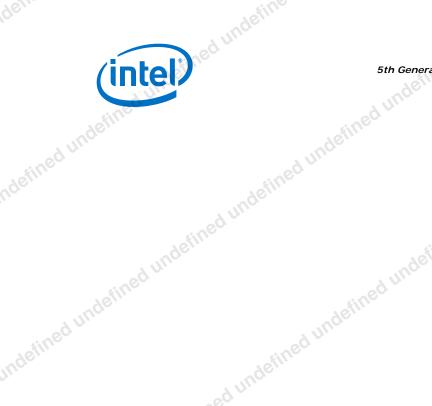


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Available on select Intel® processors. Requires an Intel® HT Technology-enabled system. Your performance varies depending on the specific hardware and software you use. Learn more by visiting: http://www.intel.com/info/hyperthreading.

Requires 3D glasses and a 3D-capable display. Physical risk factors may be present when viewing 3D material.

Requires a system with a 64-bit enabled processor, chipset, BIOS and software. Performance varies depending on the specific hardware and software you use. Check with your manufacturer for more information. Learn more at http://www.intel.com/info/em64t.

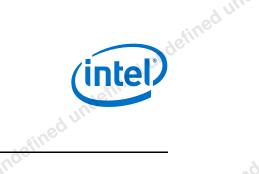
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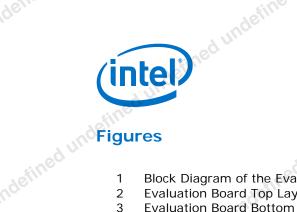
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1.1

Introduction

About this Evaluation Kit

The 5th Generation Intel[®] CoreTM i5-5350U Processor Evaluation Kit Based on Intel[®] Intelligent System Extended (ISX) Form Factor Reference Design is an Internet-of-Things (IoT) evaluation platform that can be used as-is by end-customers or can be customized by software vendors, driver developers, and system integrators.

The evaluation kit is based on the Intel[®] Intelligent System Extended (ISX) Form Factor Reference Design. It's a fanless design in a small form factor, made possible through process optimization, performance improvements, dynamic power, and thermal framework enhancements in the 5th generation Intel[®] CoreTM (U series) processor.

The evaluation kit is a dual-channel DDR3L mobility platform that uses a new 4.4×6.1 inch board form factor. It's a full performance computing platform in the smallest form factor possible that supports the 5th generation Intel[®] CoreTM (U series) processor in the BGA-type package. The Modular Board Design (MBD) of the Intel[®] ISX completes the critical signal paths for the processor and the supporting components according to Intel Design Guidelines.

This evaluation kit provides you with the necessary items to enable you to customize the board design to suit your requirements. Alternatively, for faster time to market, the board design can be used as-is out of the box.

The 5th generation Intel[®] CoreTM (U series) processor was formerly known as the Broadwell-U CPU.

1.2 Terminology

undefined undef Table 1.

Note:

defineo	Broadwell-U (CPU.	
undein 1.2	Terminol	ogy	ned un
Table 1.	Terminology	od unde	d undefined un
	Term	Definition	med
ed un	APS	Automated Power Switch	
stine	BIOS	Basic Input Output System	
inde	CMOS	Refers to the non-volatile configuration memory in the PCH	
edu	CPU	Central Processing Unit	
undefined undefined un	DDR3L	Double Data Rate Synchronous Dynamic Random Access Memory third generation (low power)	d ut
U	GND	Signal Ground	since
	HDD	Hard disk drive	nder
	HDMI	High Definition Multimedia Interface	dui
11.	LAN	Local Area Network	fine
ed t	LED	Light Emitting Diode	0 *
defili	LPC	Low Pin Count	
undefined undefined un	LVDS	Low-Voltage Differential Signaling	
	ME	Intel Management Engine	
defil	OS	Operating System	1
unc.	PCI	Peripheral Component Interface	ine ^o
	PCIe*	Peripheral Component Interface Express*	defin
	ndefine	defined a	sined une
-d 1		5th Generation Intel [®] Core TM i5-5350U Processor Evalu	ation Kit
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red	POST	Power-On Self Test	2
defin.	RTC	Real Time Clock	y unc
n	S3	"Save to RAM" Sleep State	ineo
	S5	"Soft Off" Sleep State	detti
	SATA	Serial - Advanced Technology Attachment	d une
int	SIO	Super Input Output	neu
defined undefined un	SLP	Sleep	5 °
efine	SO-DIMM	Small Outline Dual In-line Memory Module	
Inde	SSD	Solid State Drive	
edu	USB	Universal Serial Bus	
1. stine	VCC	Used to signify circuit logic voltage	, inc
INOC	VDDQ	Used to signify DIMM logic supply voltage	ed
	VGA	Video Graphics Array	1efille
	VID	Voltage Identification	unos
	VTT	Used to signify signal termination voltage	red
1.3 ned un	Evaluatio	on Board Parts unde	lu.

1.3 ned un undefined unde

Evaluation Board Parts

The evaluation board includes the following parts listed in Table 2 unless stated tined unde otherwise.

Table 2.

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List of Evaluation Board Parts

otherwise.	inde	
ist of Evaluation Board Parts	ined unde	
Evaluation Board Parts	Model	Quantity
4 GB 204-PIN DDR3L SDRAM Unbuffered SODIMM	Apacer (78.B2GCY.4000C)	Quantity 2
mSATA SSD-64 G (half-size mPCIe*)	SANDISK (SDSA5FK-064 G)	1 6110
MA 2.4 G Terminal antenna (external)	UNI LINK (TLB-2400-2.5B L)	2
Power adapter: Input: 100-240 V, AC 50/60 Hz Output:12 VDC, 4000 mA	KUANTECH (KSAH1200400W1UK)	elined 1
Intel WiFi* module	Intel (6300 633AN.HMWG)	1
mPCIe* half to full-size extender bracket	SC2MPCIEEXTOB1100P	1
3G/WiFi* Mini PCIe* card (half-size mPCIe*)‡	Option (GTM671W)	1 Jefinec
	5 § §	Lefined un
Vote: [‡] Optional and would require a separ would be a separ st [®] Core [™] i5-5350U Processor Evaluation Kit	defined un	April 2016 Number: 334089-001US
ndefined L	defined unc	stined under.
[®] Core TM i5-5350U Processor Evaluation Kit Form Factor Reference Design	ed une	April 2016
med under	Document	Number: 334089-00105

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2.0

Getting Started

Before using the evaluation kit, verify that all the items listed in this section are received, and that the evaluation board is functioning by going through the following:

- Check the contents of the evaluation kit
- Inspect the evaluation board for any defects
- Power-on the evaluation board and verify that it is functioning correctly.

Before You Begin

Verify the contents of the evaluation kit and the condition of the evaluation board. If any of the items are missing or if the evaluation board is damaged, contact Intel before you proceed.

2.1.1 Check the Contents of the Evaluation Kit

The 5th Generation Intel[®] CoreTM i5-5350U Processor Evaluation Kit Based on Intel[®] Intelligent System Extended (ISX) Form Factor Reference Design contains the following items:

- 5th Generation Intel[®] Core[™] i5-5350U Processor Evaluation Kit Based on Intel[®] Intelligent System Extended (ISX) Form Factor Reference Design System
- 12 V@4 A DC Power Adapter
- System Drivers + User Guide (CD)
- Safety Flyer
- China RoHS Declaration
- WCL

Intel[®] Evaluation Vehicles Terms and Conditions

2.1.2 Inspect the Evaluation Board

To check the evaluation board for damages, set it on an anti-static surface and inspect the evaluation board to ensure that the components are not missing, bent, or cracked.

The evaluation board may be damaged if it is not placed on an anti-static surface.

Caution:

2.1.3 Power-on the Evaluation Board

Once the evaluation board is free from any visible defects, power-on the evaluation board and verify that the evaluation board is functioning correctly using the following steps:

1. Connect the supplied DC power adapter to the evaluation board.

Note: Only use the DC power adapter supplied with the evaluation kit

2. Press the POWER BUTTON.

- 3. Select the **Del** key as the system boots to enter the BIOS setup screen.
- 4. Check the time, date, and configuration settings. The default settings should be sufficient for most users with the exception of Intel SpeedStep[®] Technology. This feature is disabled by default and can be enabled in setup.
- 5. Save and exit the BIOS setup.

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6. The system will reboot and would then be ready for use.

Note:

- The evaluation board can be powered down with the following methods:
 - Use the Windows* Start menu (or equivalent) shutdown option
 - Press the **POWER BUTTTON** to begin the power-down process
- .U undefined und If the above does not work, hold down the **POWER BUTTON** for four seconds to asynchronously shut down the system (not recommended).

Reference Documents

Table 3.

2.2

Technical Reference Documents

inc	<u> </u>	7112	
redu	Document Description	Document Number/Location	2
ndefined unic	5th Generation Intel® Core [™] Processor Family and Intel® Core [™] M Processor Family (Broadwell U/Y) – External Design Specification (EDS) Volume 1 of 2	514405	undefined unr
	Broadwell Mobile U-Processor and Y-Processor External Design Specification (EDS) Volume 2 of 2	514525	unden
d un	5th Generation Intel [®] Core™ i5-5350u Processor Evaluation kit based on Intel [®] ISX Reference Design – System Reference Design Schematic and Board File	556749	
definec.	5th Generation Intel [®] Core™ i5-5350u Processor Evaluation Kit Based on Intel® ISX Reference Design BIOS Image – BIOS Reference Code	557335	
ed uno	5th Generation Intel [®] Core™ i5-5350u Processor Evaluation kit based on Intel ISX Reference Design - Mechanical Reference Design Files	557242	
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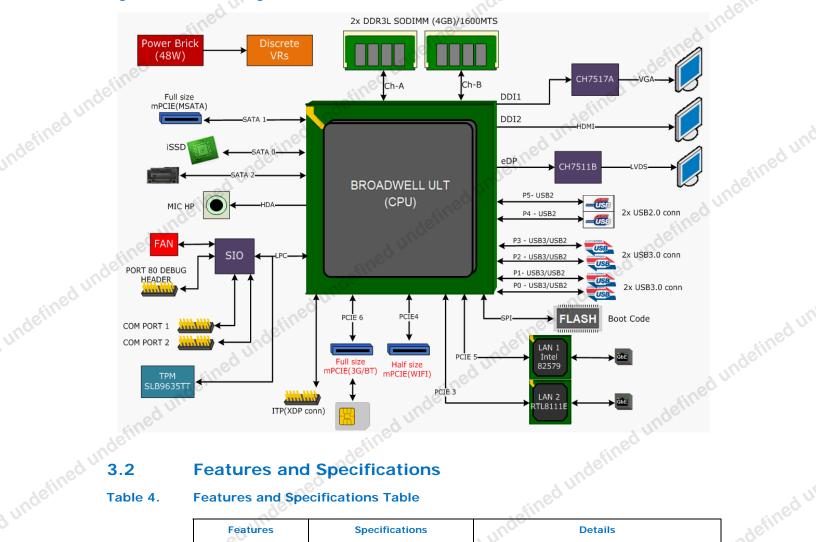


ndefined undefined Evaluation Kit Overview

Block Diagram

Figure 1.

Block Diagram of the Evaluation Kit

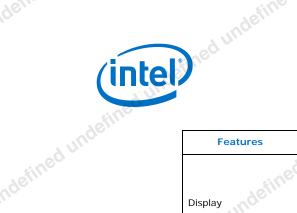


3.2 Features and Specifications

Features and Specifications Table

3.2	Features and	I Specifications	INOC	
Table 4.	Features and Spe	ecifications Table	atined	ined ut
0	Features	Specifications	Details	defin
ned un	СРИ	Family Model Package type TDP	Broadwell-U Mobile 5th Generation Intel [®] Core™ i7/i5/i3 Processor BGA 1168 Maximum up to 15 W	une
tined undefilt	Memory	RAM type Maximum RAM size Maximum RAM speed RAM slot	DDR3L (1.35 V) 16GB ¹ 1600MT/s 2	
unden	BIOS	SPI model	W25Q128FV; 128 M-bit SOIC-8 serial flash memory	ed V
d d	EC/SIO	LPC-IO	IT8728F	defille
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(intel	5th Generation Intel [®] Core TM i5-5350U Processor Evaluation Kit				
		d unde.	indefine		
Indefin	Features	Specifications	Details]	
	Display	Graphic type Integrated audio Maximum resolution Display option Others	Integrated Supported 3840 × 2160 at 60 Hz 1 × VGA connector 1 × Standard HDMI connector 1 × Dual-channel LVDS header 3 Display supported	undefined und	
sined uno	Storage	mSATA (default) HDD/SSD iSSD (optional) ²	Full-size Mini PCIe* slot Standard SATA 3.0 connector Soldered down iSSD (optional) ²		
ndefined undefined unde	Audio	Integrated HD Audio Codec Codec model Port	Supported Realtek ALC662 1 × 3.5 mm jack with line out and mic		
ndefill	USB	USB 3.0 USB 2.0	4 × USB 3.0 port 2 × USB 2.0 port	d un	
<i>y</i>	Network	Gigabit LAN port Intel LAN controller model 2nd LAN controller model 3G + WiFi* WiFi*	2 × RJ45 port Clarksville (i218-LM) with Intel [®] AMT support Realtek (RTL8111E) 1 × Full-size Mini PCIe slot + 1 × Micro SIM slot 1 × Half-size Mini PCIe slot	undefine	
sineo	Serial Port	COM port header	2 × RS232 header		
unden	Power Supply	Mobile mode 48 W power adapter	12V @4 A input DC power		
undefined undefined und	Others undering	Clocks RTC Processor VR TPM LPC ITP	Fully integrated clocking Battery-backed real-time clock ISL95812; Intel VR12.5 Serial VID (SVID) compliant SLB9635TT; TPM ver 1.2 1 × LPC debug header 1 × XDP debug port	undefined ut	
	System Form Factor Dimension	System Form Factor (W \times L \times H)	4.6" × 7.2" × 1.7"		
dundefille	PCB Dimensions	Board Form Factor Board Z-height PCB layer count	4.4" × 6.1" 1.61" 10 layers		
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3.3

Power Management States

Table 5.

Power Management States Description

		(c)		
Table 5 lists the power The Controller Link (Cl	0		•	unde
Power Management	States Description	indefine		defined
State	e e	Description	A UM	
G0/S0	Full on mode. Display on.		siner	
G0/S0	Connected standby mode.	Display off.	der	
G1/S3-Cold	Suspend-to-RAM (STR). Co the processor).	ontext saved to memory (S3	3-Hot is not supported by	
G1/S4	Suspend-to-Disk (STD). Al	ll power lost (except wakeup	o on PCH).	
G2/S5	Soft off. All power lost (exe	cept wakeup on PCH). Total	system reboot.	5.
G3	Mechanical off. All power s	source (AC and battery) rem	oved from the system.	dui.
The voltage of the eva Table 6. Evaluation Board Po		nets at different activi	ty states is shown in	Indefinee
POWER NET	VOLTAGE	POWER WELL	ACTIVITY STATES	

Table 6. undefined undefined

Evaluation Board Power States

7 A.				lei!!	_
Indefined undefined u.	POWER NET	VOLTAGE	POWER WELL	ACTIVITY STATES	
den	+VDCIN	12 V	ALWAYS ON	S0-S5	
dull	+V5 A	5 V	ALWAYS ON	S0-S5	1
	+V3.3 A	3.3 V	ALWAYS ON	S0-S5	1
nder	16/110		sineo		ndefined
	LAN1_V3P3	3.3 V	LAN	S0-S5	since
	+V3.3 M	3.3 V	ME	S0–S5	nde.
A	+V1.05 M	1.05 V	ME	S0–S5	0.
undefined undefined und		dei	· ·	sine	
eo -	+VSM	1.355 V	DDR3L	S0-S3	
defin	+VSM_VTT	0.675 V	DDR3L	S0	
A UNC		nder.	÷	efine	
aneo	+V12S	12 V	CORE	S0	
detti	+V5S	5 V	CORE	S0	
	+V3.3S	3.3 V	CORE	SO	sineu
	+V1.05S	1.05 V	CORE	SO	den
	+ VCORE	1.5 V-1.85 V	CORE	SO	Un
0	+V1.8S	1.8 V	EDP to LVDS	S0	·
ed u.	+V1.5S	1.5 V	CORE	SO SO	
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Evaluation Kit Setup 4.0

This section provides the following details:

- Lists the major components and their locations on the evaluation board, front panel and back panel
- Describes the pinouts of the headers
- Lists the LED indicator location and colors for different power states
- · Provides the configuration settings to clear the BIOS.

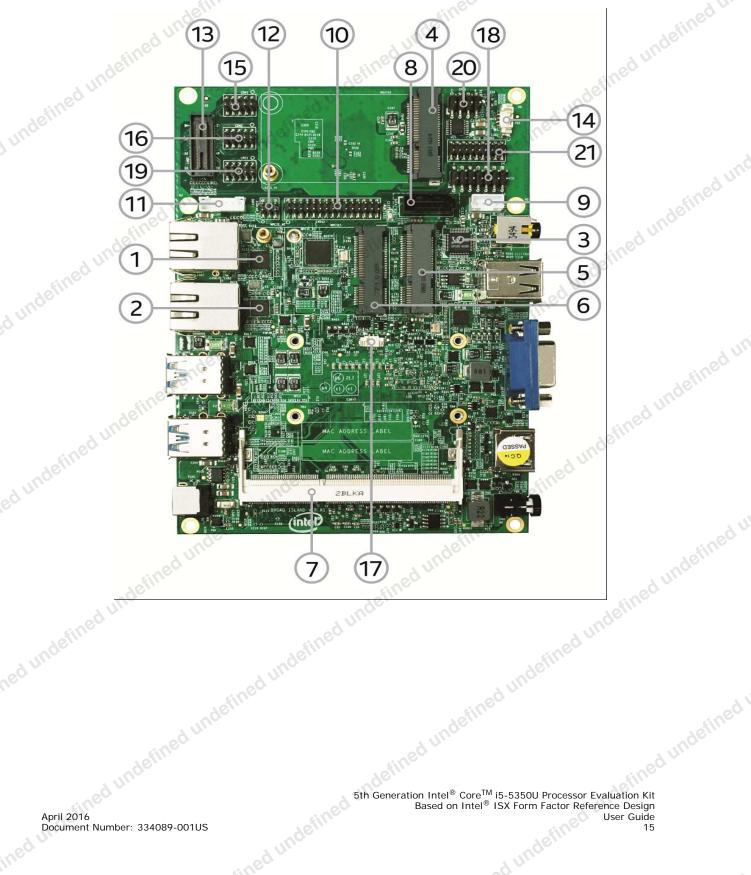
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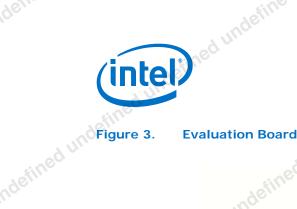
5th Generation Intel[®] Core[™] i5-5350U Processor Evaluation Kit indefined Based on Intel[®] ISX Form Factor Reference Design User Guide 14



Figure 2.

Evaluation Board Top Layer





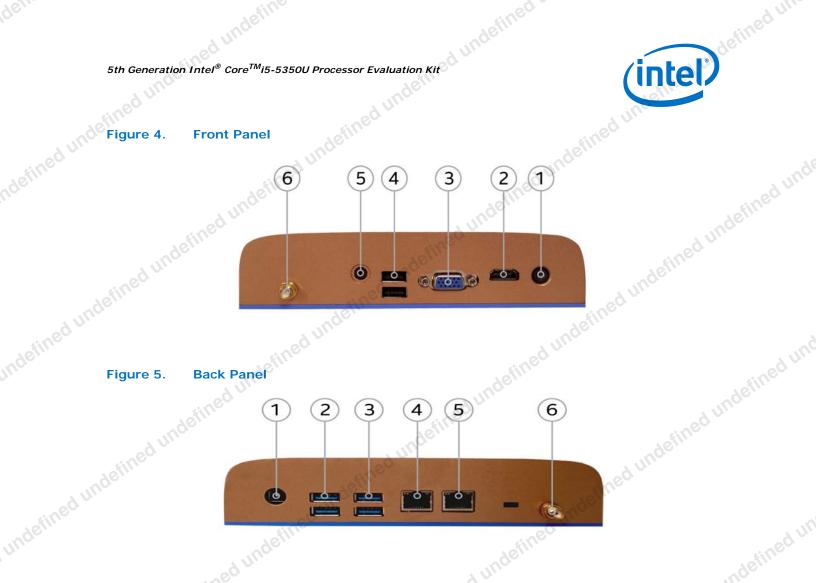
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Evaluation Board Bottom Layer



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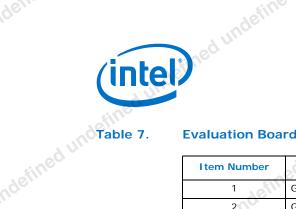
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List of Components 4.2

.gna The following tables list the major components and the reference designator of the ane

5th Generation Intel[®] CoreTM i5-5350U Processor Evaluation Kit Based on Intel[®] ISX Form Factor Reference Design User Guide



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undefined undefined un

Evaluation Board Top Layer

tem Number	Description	Reference Designator U5 U32 U4	
1 611	GbE controller 2 (RTL8111E)	U5	.6
210	GbE controller 1 (Clarkville- i128LM)	U32	
0 3	Audio Codec (ALC662)	U4	
4	Mini PCIe connector (full size) - MSATA	MSATA1	
5	3G + WiFi*	MPCIE2	
6	Mini PCIe connector (half size)	MPCIE1	
7	Non-ECC DDR3 sodimm connector (CH A)	JI	
8	SATA 3.0 connector	SATA1	
9	SATA power header	SATA_PWR1	
10	LVDS signals header	SATA_PWR1 LVDS1 INVT1 LCDPWR_SEL1	
11,00	LVDS inverter power	INVT1	
12	LVDS VDD selection power jumper	LCDPWR_SEL1	
13	XDP connector	XDP1	
14	Fan 4-pin header	FAN1	
15	Serial port header (COM 1)	COM1	
16	Serial port header (COM 2)	COM2	
17	RTC header	J_RTC1	
18	APS header	APS1	
19	Port 80 LPC header	LPC1	
20	SPI flash header	LPC1 SPI1 DEBUG1	
21	Debug header	DEBUG1	11-

Table 8.

Evaluation Board Bottom Layer

	0.	76,	0 is	
a undefined undefined un	Item Number	Description	Reference Designator	
1 etine	1	CPU (Broadwell U)	01	
unole	2	EC/SIO (IT8728F)	U11	
red	3	Non-ECC DDR3 sodimm connector (CH B)	J2	
defill	4	SPI chip (W25Q128FV)	U3	. U
und	5	TPM (SLB9635TT)	U2	ed
		Micro SIM slot	SIM1	d undefined u
	6117	ISSD (optional)	U29	, unc.
5th Generation Int Based on Intel [®] IS User Guide 18	Indefine	Processor Evaluation Kit nce Design	April 2016 ent Number: 334089-001US	ed undefined i



Table 9.

Front Panel

ntel [®] Core [™] i5-535 Front Panel	OU Processor Evaluation Kit	inter
Item Number	Description	Reference Designator
1 6110	Power button	PWR_SW1
2	HDMI connector	HDMI1
3	VGA connector	VGA1
4	Dual USB 2.0 stacked connector	USB3
5	Single port audio jack	AUD1
6	Antenna SMA connector 1	100
Back Panel	ndefine	defined b.
1		

undefined undefineu ... **Back Panel**

		Antenna SMA connector 1	100-
A UN TAble TO. Ba	ck Panel	ndefine	Reference Designator
ned und Table 10. Ba	Item Number	Description	Reference Designator
	1 10	DC power jack	DC_IN1
	2	Dual USB 3.0 stacked connector 1	USB2
	CO 3	Dual USB 3.0 stacked connector 2	USB1
ed undefined unde	4	Single LAN RJ45 connector 1	LAN1
4 Unc	5	Single LAN RJ45 connector 2	LAN2
tine ⁰	6	Antenna SMA connector 2	inor
undefined undefi	neo	Single LAN RJ45 connector 2 Antenna SMA connector 2	afined undefine
	undef	ned uns	
	ined t	Lefined une	ine

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5th Generation Intel[®] CoreTMi5-5350U Processor Evaluation Kit

Header Pinout Configuration

ndefined und 4.3 4.3.1 **Evaluation Board Header Pinout**

undefined undefined undefined unde The following tables list the pinout configuration for the headers, and their corresponding signal names, on the evaluation board.

Table 11. **Evaluation Board Connector Functions**

defined undefined und	Label		
ndefinec		Function	10th
nder	XDP1	XDP Debug Port	dundefined undefinet
	COM1	COM1	tipeo -
du	COM2	COM2	defin
	LPC1	Low Pin Count Bus interface	d une
0*	INVT1	Inverter Power	30 dui
	LCDPWR_SEL1	LVDS Operating VDD Selection	ofine
	LVDS1	LVDS Connector	inde
	J_RTC1	RTC Battery Connector	ed u
, un	SATA_PWR1	SATA Power	etine
	APS1	APS Debug Port	Inde
dein	Debug1	Debug Port	edu
	SPI1	SPI Flash Programming Connector	10tin-
	FAN1	System Fan Connector	Inoc
			e ⁰
stined undefine		ed undefineo	d undefined un
	tined under.	d undefi	inc indefineo
defined	Indefined under.	offined undefined undefi	red undermed

sation Kit 5th Generation Intel[®] Core[™] i5-5350U Processor Evaluation Kit Based on Intel[®] ISX Form Factor Reference Design User Guide 20

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Table 12.

med unc		nder			
		ed un		une	
Table 12.	XDP Debug Port (XI	DP1)			
atined und ^{eltable} 12.	XDP Debug Port (XI	Signal Name	Pin 1001	Signal Name	
	Stines	GND	2	GND	defined
	3	PREQ	4	CFG17	
	à U.	PRDY	6	CFG16	
lefined undefined unde	7	GND	8	GND	
	9	CFG0	10	CFG8	
ed u.	11	CFG1	12	CFG9	
stine	13	GND	14	GND	
inde	15	CFG2	14	CFG10	
ed U.	17	CFG2 CFG3	18		
	19	GND	20	CFG11 GND	
	21	BPM0	20	CFG19	
	21			CFG19	ndefined
	23	BPM1 GND	24	CFG18 GND	
6	23	9.5	28	CFG12	
d Une	27	CFG4	30		
	31	CFG5	30	CFG13	
delli	31	GND	32	GND	
d une	33	CFG6		CFG14	
	35	CFG7	36 38	CFG15	
9611	37	GND	40	GND	
defined undefined und	39	VCCST_PWRGD		CLK_P	terined
		PWRBTN	42	CLK_N	der.
	43	1.05V	44	1.05V	01.
nı,	45	PWR_DEBUG		PLT_RESET	
	47	SYS_PWROK	48	PM_RESET	
ad undefined un	49	GND	50	GND	
Inos	51	SMB_DATA	52	TDO	
		SMB_CLK	54	TRST	
defill	55	NC	56	TDI	
10.5	57	TCK	58	TMS	
Idefined une	57 59 646 meetinee Maaimeetinee Maaimeetinee Maaimeetinee Maaimeetinee	GND	54 56 58 60 net under fine of the second sec	GND	defille
Indefined undefined un	afinee		ned t	8	une
		def			
		a une		nder	
10fille				dui	
unoe					
red		une		der	
defin.			d u		
Inc	den		stine		
	4 un		inde		yetin,
			ed v.		, unu-
	der		ine		
24		the state	version Int-I® or TM		
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Serial Port (COM1/COM2)

	ned undefin		undefine
Serial Port (COM1	/COM2)		tined L.
Pin	Signal Name	Pin	Signal Name
1.	DCD	2	SIN
3	SOUT	4	DTR
5	GND	6	DSR
7	RTS	8	CTS
9	NC	10	NC
Low Pin Count Bus	(LPC1)		ned unoc
Pin	Signal Name	Pin	Signal Name

Table 14. Judefined unde

Low Pin Count Bus (LPC1)

Pin	Signal Name	Pin	Signal Name	
1	AD0	2	RESET	101
3	AD1	4,000	FRAME	ofined un
5	AD2	6	3.3 V	atine
1000 T	AD3	8	GND	nde
9	Clk	10	NC	
Inverter Power (IN	IVT1) ed unde	_	ndefined undefin	
Pin	Signal Name			
1	BKL_PWR 12 V		den	
2	BKL_PWR 12 V	d ^{ul}		
3	BKL_ENABLE	sinec		ed u.
4	BKL_CONTROL	der		Aine

Table 15. Jle undefined undefin **Inverter Power (INVT1)**

	00	1 Ult
Pin	Signal Name	ned undefined undefined un
1	BKL_PWR 12 V	oden
2	BKL_PWR 12 V	dull
3	BKL_ENABLE	ed land
4	BKL_CONTROL	nder
5	GND	dun.
6	GND	ine
Pin	Signal Name	Lefined U.
1-2	+3.3 V (Default)	unoc
3-4	+5 V	
detti	tined unde	times and undefined t
undefined	under	odefined undefine
el [®] Core TM i5-5350U Processo X Form Factor Reference Desig	- Evaluation Kit	LCDPWR_SEL1)
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Table 16. undefined undef

Jundefined undefin	Pin	Signal Name	sinec
edu	1-2	+3.3 V (Default)	nder
10fille	3-4	+5 V	ad un
unoc	5-6	+12 V	afine
a undefined undefined u	ndefined un	undefined unde	April 2016
ed undefine	Indefined undefine	50	efined undefined undefined undefined
5th Generation Inte Based on Intel [®] IS	el [®] Core TM i5-5350U Proces: X Form Factor Reference De	sor Evaluation Kit	Inde
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Table 17.

LVDS Connector (LVDS1)

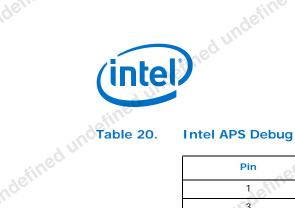
thed un.		ned unoc		Intern
ndefined under Table 17.	LVDS Connector (LV	DS1)	efil	
sineo	Pin	Signal Name	Pin	Signal Name
der	3910	VDD	2	VDD
	3	VDD	4	NC
	5	GND	6	GND
36	7	DATA0-	8	DATA0+
undefined undefined undef	9	DATA1-	10	DATA1+
eq e	11	DATA2-	12	DATA2+
defin.	13	GND	14	GND
, unc.	15	CLK1-	16	CLK1+
cine ⁰	17	DATA3-	18	DATA3+
detti	19	DATA4-	20	DATA4+
nuc.	21	DATA5-	22	DATA5+
	23	DATA6-	24	DATA6+
	25	GND	26	GND
nde	27	CLK2-	28	CLK2+
ed V.	29	DATA7-	30	DATA7+
Table 18.	RTC Battery Connec	tor (J_RTC1)	led undefined unde	tined un
eineu	Pin	Signal Name	unoc	
del	1 110	Battery +	ed t	
UI.	2	Battery -	defin.	
Table 19.	SATA Power (SATA_	PWR1)	led un.	-0
, uno	Pin	Signal Name	Ţ	lefines

RTC Battery Connector (J_RTC1)

Pin	Signal Name
	Battery +
2	Battery -
1 cine0	<u> </u>

undefined unoTable 18.	RTC Battery Connect	or (J_RTC1)	sined	
ined u	Pin	Signal Name	under	
defin	1 finet	Battery +	ed to	d un
Ull	20	Battery -	defili	stinet
Table 19.	SATA Power (SATA_I	PWR1)	Preration Intel [®] Core TM i5-5350U Processor Eval Based on Intel [®] ISX Form Factor Reference	d unde.
undefined undefined u	Pin	Signal Name		stinec
sineu	1	+12 V	uno.	
nder	2	GND	sineo	
ed u.	3	GND	- dell	
retine	4	+5 V	dui	. u
uno	ndell		letine	aned -
0	d un.		unoc	detin
	efine		ined	d une
a undefined undefined	unoc	de	Ur.	stines
ined .		d un	inc	
detti		afine	ned t	
d un			defin	
afines	ned		dune	
Inde	defin		stinet	ed \
20 T	dune			Actine
			edu	a uno
	inder	20	Still-	sineu
ed	V.	5th Ge	eneration Intel [®] Core TM i5-5350U Processor Eval	uation Kit
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Intel APS Debug Port (APS1)

Intel APS Debug Por	t (APS1)		need undefineers
Pin	Signal Name	Pin	Signal Name
1.610	+3.3 A	2	SLP_S3
3	+3.3 A	4	+3.3 A
5	SLP_S4	6 G	SLP_A
7	NC	8	GND
9	RTC_RST	10	GND
11	PWRBTN	12	GND
13	RSTBTN	14	GND
Debug Port (Debug1	nde	unde	
Pin	Signal Name	Pin	Signal Name

undefined undefined und Debug Port (Debug1)

Pin	Signal Name	Pin	Signal Name
UNC	SPI_MISO	2	SPI_MOSI
3	SPI_CS	4	SPI_CLK
e ^T 5	GND	6	GPIO0
7	NC	8	GPI01
9	I2C_SDA	10	I2C_SCL
11	SMB_ALERT	12	GND
13	SMB_DATA	14	SMB_CLK
15	NC	16	GND
17	+3.3A	18	+5A
SPI Programming C	onnector (SPI1)	d undern	
		Pin Pin	

undefined undefined un Table 22.

SPI Programming Connector (SPI1)

Pin	Signal Name	inec Pin	Signal Name
1	+3.3 V	2	GND
3	SPI_CS	4	SPI_CLK
5	SPI_MISO	6	SPI_MOSI
7	NC NC	8	DETECT
System Fan Conne	ector (FAN1)	ned undefined	une
Pin	Signal Name	nden	
sineu	GND	dui	
2	+12 V	fine	
3	FAN FB		

undefined undefin Table 23.

System Fan Connector (FAN1)

d un.	7	NC	8	DETECT	
undefined under Table 23.	System Fan Connec	ctor (FAN1)	ned u		A V
3 UIL	Pin	Signal Name	undefined u		definec
	sin ^{eu} 1	GND	du.		unos
	2	+12 V	fine		
- A V	3	FAN_FB		4efin.	
	4	FAN_PWM		a une	
d undefined undefined u		ed undefine	2	undefined undefin	
ed under	tined undefin		4 undefinet		ndefined
	under		Jefineo	A	led un
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Push-Buttons and LED Indicators

Power-On Button

Indefine The evaluation kit system has a single push-button POWER button. The POWER button enables or disables power to the entire evaluation kit system causing it to boot or shut down.

The location of the POWER button is shown in Table 24.

Table 24.

4.4

4.4.1

Push-Buttons Location Table

Description	Reference Designator
Power button	PWR_SW1

4.4.2 LED Indicators

There are two LED indicators in the evaluation kit system: power button LED and standby LED. The power button LED is located at the POWER button (PWR_SW1) while the standby LED is located at LED1.

The location, power state, and color of the LED indicators are shown in Table 25.

Table 25. **LED Indicators Table**

Description	Reference Designator	Power State	Color
Standby LED	LED1	S4/S5	Red
Power button LED	PWR_SW1	SO ATT	Blue

4.5 **Configuration Settings**

4.5.1

Note:

J_RTC1 — Clear CMOS or ME Settings

Clearing the contents of all BIOS or ME settings will restore the evaluation kit system to factory default values.

J_RTC1 is connected to a coin battery by default.

To restore the BIOS settings:

- 1. Turn off the evaluation kit system, and unplug the power cord.
- 2. Remove the 3.3 V coin battery from J RTC1 for a few seconds, and then install the undefined undefined 3.3 V coin battery.
- 3. Turn on the evaluation kit system undefined undefined undefined

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5.0

Thermal and Mechanical Design Information for the Evaluation Kit System

The evaluation Kit based on Intel[®] Intelligent System Extended (ISX) Reference Design offers a powerful computing performance in a compact chassis measuring 4.6×7.2 inch $\times 1.7$ inch.

Inside the chassis is a 4.4 \times 6.1 inch motherboard. To meet the thermal requirements of the 5th generation $Intel^{\circledast}$ CoreTM (U series) processor, the chassis is designed to ensure adequate airflow in order to support the thermal solution for the processor and critical components.

The evaluation board is enclosed in a full metal chassis. As this is a fanless system, the heat generated by the Intel[®] Core[™] i5-5350u Processor is dissipated to the chassis by means of conduction. The metal chassis acts as a heat sink.

Warning:

The surface of the chassis may get hot when the processor is operating in a high workload. The chassis surface is hot enough to burn when it comes into contact with human touch.

The evaluation kit system is designed to meet the 35? C ambient temperature.

As part of the Intel[®] ISX Form Factor Reference Design program, the mechanical design files for the chassis are mass production ready. The program also gives the flexibility for embedded design houses to modify the mechanical design according to their requirements, which provides opportunities to incorporate the reference design into their custom designs, gain the benefits that Intel[®] architecture provides, and accelerate their time-to-market.

undefined undef Note:

For the 2D drawings and 3D design files, kindly refer to Table 3, CDI #557242.

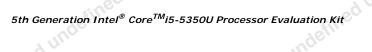
5.1

Evaluation Kit System Design and Specification

, undefined undefined undefined undefined Figure 6 shows the design of the evaluation kit system while Table 26 shows its ed undefined undefined undefined undefined specification.

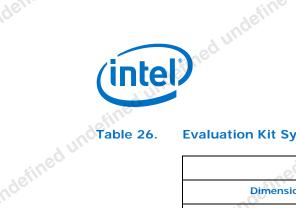
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Evaluation Kit System Specification

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mol	ĥ	efill
SYS	TEM	
Dimensions	4.6 × 7.2 × 1.7 inch	ettined undefined un
Thickness	1.7 inch	
Weight	~760 g	d ull
TOP	COVER	Aetine
Material	Aluminum	4 UNOC
Color	Copper brown (Pantone 876)	
Finishing	Sandblast	9e.
Weight TOP Material Color Finishing BOTTO	A COVER	
Material	Aluminum	
Color	Blue (Pantone 2727)	
Finishing FEAT Security VESA Mount Date: Embedded design houses have specifications according to their	Sandblast	
FEAT	URES	defined undefined u
Security	Kensington lock slot	ed u.
VESA Mount	>19" Displays	defill
aned undefill	S S S	4 undefined t
dett.	nedt	afineo
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6.0

Disassembly and Reassembly Procedure

This section provides details regarding the following:

- Precautions and safety handling of the evaluation kit system
- Disassembly and Reassembly of the evaluation kit system

Precautions and Safety Handling of the evaluation Kit 6.1 **System**

The evaluation kit system contains components that are static-sensitive. Electrostatic can cause underlying damages to the system, resulting in failures occurring weeks or months later. Therefore, Electrostatic Discharge (ESD) prevention is important when handling the system.

Observe the following precautions and safety handling before disassembling the evaluation kit system:

- Ensure that the working area is properly grounded using the highest level of ESD protection available. It is recommended to use a wrist strap, ground cords, a table mat, a floor mat, ESD shoes, and an ESD chair.
- Do not wear nylon clothing when handling the system.
- Before touching the system, touch an electrical ground to remove any electrostatic charge from the body that may have accumulated.
- If possible, handle the system's components by holding on to the package and not by the leads.
- Use ESD protection bags when storing or moving the system's components.
- Ensure that all power source is removed from the system.

Warning:

Failing to comply with the proper grounding and handling procedures may cause damage to the evaluation kit system.

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Evaluation Kit System Disassembly and Reassembly

It is not recommended to disassemble the evaluation kit system for repair purposes. If the system is faulty and requires repair, send it to the nearest Intel Service Center.

The following disassembly procedure should only be performed if necessary. Jundefined undefined undefined undefined

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Evaluation Kit Completed Assembly Indefined undefined undefined undefined

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Evaluation Board Removal

stined und undefined undefined undefined undefined 1. Remove the four M3×6 screws from the bottom cover as shown in Figure 9.

Figure 9. undefined undefined undefined

6.2.1

Bottom Cover Screws Removal

ation Kit 5th Generation Intel^® Core^{TM} i5-5350U Processor Evaluation Kit Based on Intel^® ISX Form Factor Reference Design User Guide 32

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2. Gently remove the bottom cover from the chassis.

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Figure 10. **Bottom Cover Removal**

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3. Remove the six M3×4 screws from the evaluation board as shown in Figure 11. undefined undefined undefined undefined undefined

Inderned underned und

Figure 11. **Evaluation Board Screws Removal** Indefined undefined undefined undefined

M3 X 4 SCREW

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Lift PCBA from this side



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4. Remove the evaluation board by lifting it up at an angle as shown in Figure 12. undefined undefined unde

ndefined undefined Figure 12. **Evaluation Board Removal**

Note:

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5th Generation Intel[®] CoreTM i5-5350U Processor Evaluation Kit Based on Intel[®] ISX Form Factor Reference Design User Guide



6.2.2 **Debug Ports Access**

Note:

lefined unde fined undefined undefined unde The debug ports can be easily accessed without having to remove the bottom cover.

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- 1. Remove the four M2×4 screws as shown in Figure 13.
- Figure 13. Remove the four screws undefined undefined undefin

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ad undefined undefined undefined undefined

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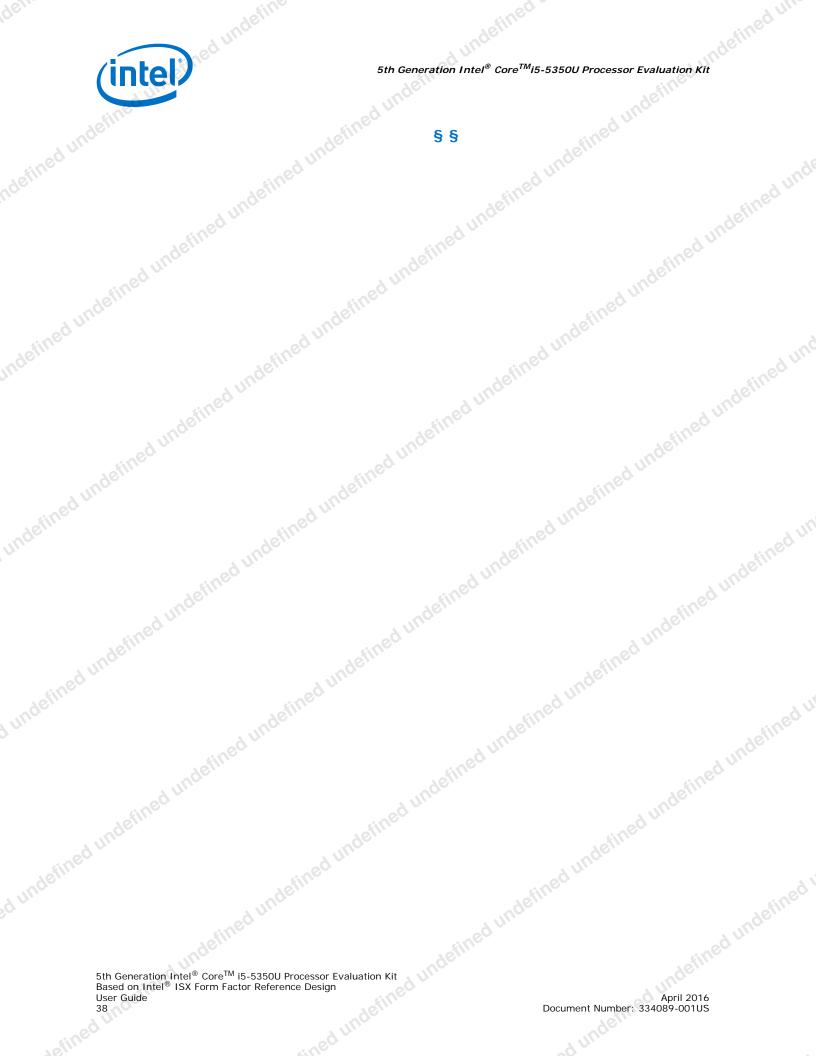
2. Gently remove the debug port access window from the chassis.

ndefined undefined Figure 14. **Debug Port Access Window Removal** undefined undefined undefined undefined

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