Intel® 852GM Chipset Platform

Design Guide

For Use with the Mobile Intel® Pentium® 4 Processor-M, Mobile Intel® Celeron® Processor on .13 Micron Process in the 478-Pin Package, and Intel® Celeron® M Processor

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Revision History

Rev	Order No.	Description	Date
001	252338	Initial Release	January 2003
002	252338	Revisions include: • Added support for the Intel Celeron M Processor	January 2004
003	252338	Revisions include: • Updated sheets 40 and 41 of the Intel Celeron M / 852GM CRB schematics	January 2005

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1. Introduction

This design guide organizes and provides Intel's design recommendations for the Intel® 852GM chipset based systems. These design guidelines have been developed to ensure maximum flexibility for board designers while reducing the risk of board related issues.

The following processors can be combined with the Intel 852GM GMCH chipset:
- Mobile Intel® Pentium® 4 Processor-M
- Mobile Intel® Celeron® processor
- Intel® Celeron® M processor

1.1. Terminology

Term	Definition
AC	Audio Codec
AMC	Audio/Modem Codec
Anti-Etch	Any plane-split, void or cutout in a VCC or GND plane is referred to as an anti-etch
ASF	Alert Standards Format
BER	Bit Error Rate
CMC	Common Mode Choke
EMI	Electro Magnetic Interference
ESD	Electrostatic Discharge
FS	Full Speed – Refers to USB 1.1 Full Speed.
FWH	Firmware Hub – A non-volatile memory device used to store the system BIOS.
HS	High Speed – Refers to USB 2.0 High Speed.
ICH4-M	I/O Controller Hub Fourth Generation – Mobile
LCI	LAN Connect Interface
LOM	LAN on Motherboard
LPC	Low Pin Count
LS	Low Speed – Refers to USB 1.0 Low Speed.
MC	Modem Codec
GMCH	Graphics Memory Controller Hub
PCM	Pulse Code Modulation
PLC	Platform LAN Connect
FSB	Front Side Bus – Processor to GMCH
RTC	Real Time Clock
SMBus	System Management Bus – A two-wire interface through which various system components can communicate

Term	Definition
SPD	Serial Presence Detect
STD	Suspend-To-Disk
STR	Suspend-To-Ram
TCO	Total Cost of Ownership
TDR	Time Domain Reflectometry
UBGA	Micro Ball Grid Array
USB	Universal Serial Bus
VRM	Voltage Regulator Module

1.2. Referenced Documents

Contact your Intel Field Representative for the latest revsions.

Document	Location
Mobile Intel® Pentium ® 4 Processor –M Datasheet (250686)	http://developer.intel.com
Mobile Intel® Celeron® Processor Datasheet (251308)	http://developer.intel.com
Intel® Celeron® M Processor Datasheet (300302)	http://developer.intel.com
PCI Local Bus Specification 2.2	www.pcisig.com
Intel® 82801DBM I/O Controller Hub 4 Mobile (ICH4-M) Datasheet (252337-001)	http://developer.intel.com
Intel® 852GM Chipset (GMCH) Datasheet	http://developer.intel.com
Application Note AP-728: ICH Family Real Time Clock (RTC) Accuracy and Considerations Under Test Conditions (Application Note AP-728)	Contact your Intel Field Representative
ITP700 Debug Port Design Guide	Contact your Intel Field Representative
JEDEC Standard, JESD79, Double Data Rate (DDR) SDRAM Specification	Contact your Intel Field Representative
Intel® DDR 200 JEDEC Spec Addendum	http://developer.intel.com
FWH Datasheet Specification	http://developer.intel.com
PC2100 DDR SDRAM Unbuffered SO-DIMM Reference Design Specification	http://developer.intel.com

2. System Overview

The Intel 852GM GMCH is a graphics memory controller hub (GMCH) component for mobile platforms. It provides the processor interface, system memory interface (DDR-SDRAM), Hub interface, CRT, LVDS, and one DVO port.

An ACPI-compliant Intel 852GM chipset platform can support the *Full-On (S0), Power On Suspend (S1-M), Suspend to RAM (S3), Suspend to Disk (S4), and Soft-Off (S5)* power management states. Through the use of an appropriate LAN device, the chipset also supports *wake-on LAN** for remote administration and troubleshooting. The chipset architecture removes the requirement for the ISA expansion bus that was traditionally integrated into the I/O subsystem of PCIsets/AGPsets.

2.1. Intel® 852GM Chipset Platform System Features

The Intel 852GM chipset contains two core components: the Intel 852GM GMCH and the Intel ICH4-M. The GMCH integrates the following:

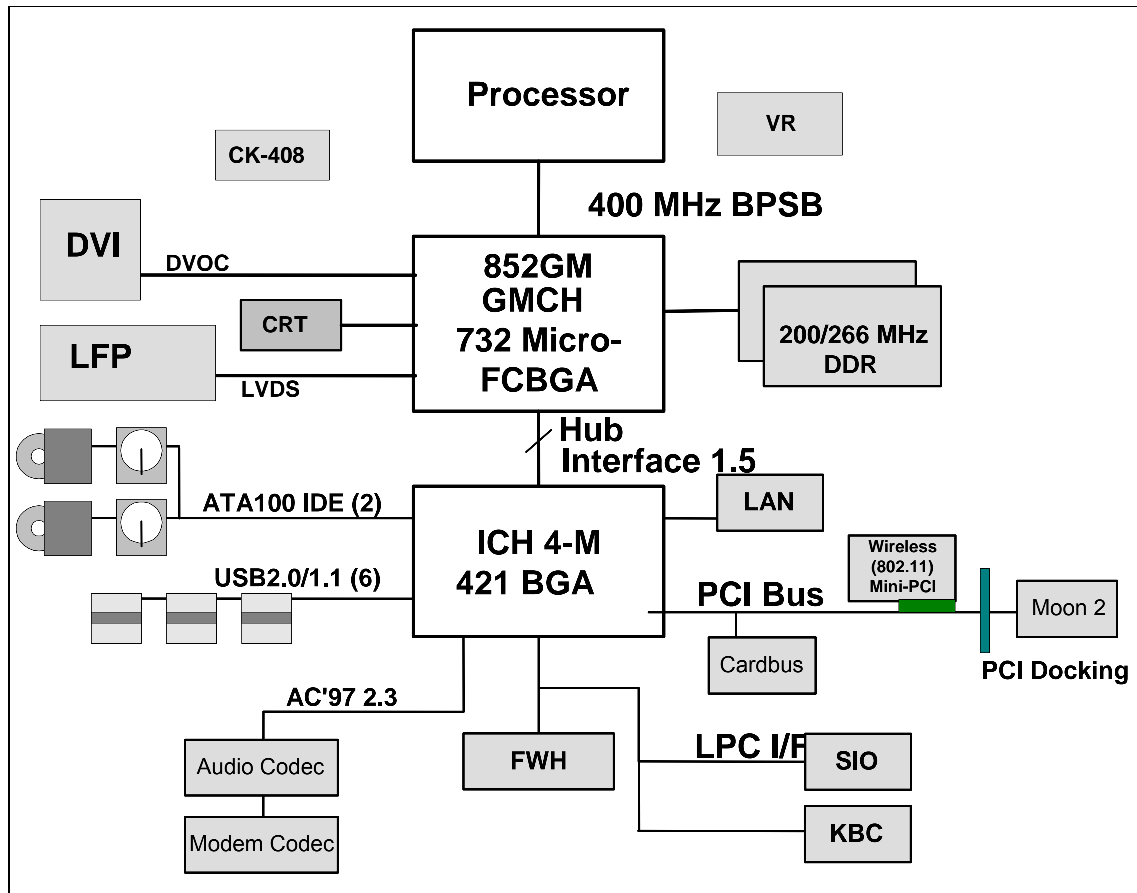
- 400-MHz processor Front Side Bus (FSB) controller
- Graphics controller interface
- Dual Channel 18 bit LVDS interface for TFT panel support
- One Digital Video Out Port (DVO)
- Supports DDR200/266 MHz memory technology
- High-speed Accelerated Hub Architecture interface for communication with the ICH4-M

The ICH4-M integrates the following:

- Ultra ATA 100/66/33 controller
- USB host controller that supports the USB 1.1 and USB 2.0 specification
- LPC interface
- FWH Flash BIOS interface controller
- PCI interface controller
- AC'97 digital controller with Enhanced 20-bit Audio support
- Hub Interface for communication with the GMCH

Figure 1 provides a basic system block diagram of the Intel 852GM chipset.

Figure 1. Intel 852GM Chipset System Block Diagram



2.2. Processor Interface

The 852GM GMCH supports a FSB frequency of 400 MHz (100-MHz HCLK respectively) using scaleable FSB VCC.

All processors are design on the .13 micron process, maintain compatibility with IA-32 software, and are designed for uni-processor based value systems

2.2.1. Mobile Intel Celeron Processor

The processor utilizes flip-chip pin grid array (FC-PGA2) package technology, which plugs into a 478-pin surface mount, zero insertion force (ZIF) socket, referred to as the mPGA478B socket.

Processor features include:

- On-die, 256-kB second level cache
- Hyper pipelined technology
- 400-MHz Front Side Bus quad-pumped bus running off a 100-MHz system clock making 3.2 GB/sec data transfer rates possible

- The execution trace cache is a first level cache that stores approximately 12-k decoded micro-operations, which removes the decoder from the main execution path.

2.2.2. Mobile Intel Pentium 4 Processor-M

The processor utilizes flip-chip pin grid array (FC-PGA2) package technology, which plugs into a 478-pin surface mount, zero insertion force (ZIF) socket, referred to as the mPGA478B socket.

Processor features include:

- On-die 512-kB second level cache
- Hyper pipelined technology
- 400-MHz Front Side Bus quad-pumped bus running off a 100-MHz system clock making 3.2 GB/sec data transfer rates possible
- Supports Streaming SIMD Extensions 2 (SSE2)
- Enhanced Intel® SpeedStep® technology which enables real-time dynamic switching of the voltage and frequency between two performance modes.
- 35-W thermal design power

2.2.3. Intel Celeron M Processor

The Intel Celeron M processor utilizes stocketable Micro Flip-Chip Pin Grid Array (Micro-FCPGA) and surface mount Micro Flip-Chip Ball Grid Array(Micro-FCBGA) package technology. The Micro-FCPGA package plugs into a 479-hole, surface-mount, zero insertion force (ZIF) socket, which is referred to as the mPGA479M socket.

Processor features include:

- On-die primary 32-kB, instruction cache and 32-kbyte, write-back data cache
- On-die 512-kB second level cache
- Supports Streaming SIMD Extensions 2 (SSE2)
- Advanced Gunning Transceiver Logic (AGTL+) bus driver technology
- Supports host bus dynamic bus inversion (DINV)
- Dynamic power down of Data Bus buffers
- BPRI# control to Disable Address/Control buffers
- Package/Power
  - Micro-FCPGA and 479-ball Micro-FCBGA packages
  - VCC-CORE: Offered in 1.356 V standard voltage and 1.004 V ultra low voltage cores
  - VCCA (1.8 V)
  - VCCP (1.05 V)

The following list provides some of the key enhancement features on this processor:

- Supports Intel Architecture with Dynamic Execution

- AGTL+ bus driver technology with integrated GTL termination resistors (gated AGTL+ receivers for reduced power)
- Supports 32 bit
- AGTL+ bus addressing (no support for 36-bit address extension)
- Supports uniprocessor systems
- 400-MHz, source-synchronous FSB
- 2X Address, 4X data
- High performance, low power core
- Advanced Branch Prediction and Data Prefetch Logic
- Advanced Power Management features

2.3. Intel 852GM Graphics Memory Controller Hub

2.3.1. Processor Front Side Bus Support

- AGTL+ bus driver technology (gated AGTL+ receivers for reduced power)
- Supports 32-bit AGTL+ bus addressing (no support for 36-bit address extension)
- Supports Uniprocessor (UP) systems
- 400 MT/s FSB support
- Supports in-order and dynamic deferred transactions

2.3.1.1. Integrated System Memory DRAM Controller

- PC1600/2100 system memory interface
- ECC not support
- Maximum of 1 GB of system memory by using 512-Mb technology devices
- Supports up to two double-sided SO-DIMMs (4 rows populated)
- Supports 64-Mb, 128-Mb, 256-Mb, and 512-Mb technologies for x8 and x16 width devices
- Supports 200-MHz and 266-MHz DDR devices
- 64-bit data interface
- Supports up to 16 simultaneous open pages
- Support for SO-DIMM Serial Presence Detect (SPD) scheme via SMBus interface
- S3 (STR) power management support via self refresh mode using CKE

2.3.2. Integrated Graphics Controller

- Graphics Core Frequency of 133 MHz

- 3D Graphics Engine
  - 3D Setup and Render Engine
  - High quality performance Texture Engine
- Analog Display Support
  - 350-MHz integrated 24-bit RAMDAC
  - Hardware color cursor support
  - Accompanying I2C and DDC channels provided through multiplexed interface
  - Hotplug and display support
  - Dual independent pipe for dual independent display
- Digital Video Out Port (DVO) support
  - Single channel DVO Port with 165-MHz dot clock support for a 12-bit interface
  - Compliant with DVI Specification 1.0
- Dedicated LFP (local flat panel) interface
  - Single or dual channel LVDS TFT panel support up to SXGA+ panel resolution with frequency range from 25 MHz to 112 MHz per channel
  - SSC support of 0.5%, 1.0%, and 2.5% center and down spread with external SSC clock
  - Dual Display Twin (Single pipe LVDS+CRT) is not supported if SSC is enabled
  - Supports data format of 18 bpp
  - LCD panel power sequencing compliant with SPWG timing specification
  - Compliant with ANSI/TIA/EIA –644-1995 spec
  - Integrated PWM interface for LCD backlight inverter control
  - Compliant with CPIS Specification 1.5
  - Bi-linear Panel fitting

2.3.2.1. Packaging/Power

- 732-pin Micro-FCBGA (37.5 mm x 37.5 mm)
- VTTLF, VTTHF (*1.05 V*);
- VCC, VCCASM, VCCHL, VCCAHPLL, VCCAGPLL, VCCADPLLA, VCCADPLLB (*1.2 V*);
- VCCADAC, VCCDVO, VCCDLVDS, VCCALVDS, (*1.5 V*);
- VCCSM, VCCQSM, VCCTXLVDS (*2.5 V*);
- VCCGPIO (*3.3 V*)

2.3.3. I/O Controller Hub (ICH4-M)

The ICH4-M provides the I/O subsystem with access to the rest of the system:

- Upstream Accelerated Hub Architecture interface for access to the GMCH
- PCI 2.2 interface (6 PCI Request/Grant Pairs)
- Bus Master IDE controller (supports Ultra ATA 100/66/33)
- USB 1.1 and USB 2.0 Host Controllers
- High Speed Debug port via USB interface
- SMBus 2.0 Controller

- FWH Interface
- LPC Interface
- AC'97 2.3 Interface
- Alert-On-LAN*
- IRQ Controller
- IPAA security

2.3.3.1. Packaging/Power

- 421-pin, BGA package (31 mm x 31 mm)
  VCC1_5 (1.5 V main logic voltage);
  VCCSUS1_5 (1.5 V resume logic voltage);
  VCCLAN1_5 (1.5 V LAN logic voltage);
  VCC3_3 (3.3 V main I/O voltage);
  VCCSUS3_3 (3.3 V resume I/O voltage);
  VCCLAN3_3 (3.3 V LAN I/O voltage);
  V5REF (5 V);
  V5REF_SUS (5 V);
  VCCRTC;
  VCCHI (1.5 V);
  VCCP (1.2-1.3 V)

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3. General Design Considerations

This section provides motherboard layout and routing guidelines. It does not discuss the functional aspects of any bus, or the layout guidelines for an add-in device.

If the guidelines listed in this document are not followed, thorough signal integrity and timing simulations should be ompleted for each design. Even when the guidelines are followed, Intel recommends that critical signals be simulated to ensure proper signal integrity and flight time. Any deviation from the guidelines should be simulated.

The trace impedance typically noted (i.e. 55 Ω ± 15%) is the "nominal" trace impedance for a 5-mil wide external trace and a 4-mil wide internal trace. However, some stack-ups may lead to narrower or wider traces on internal or external layers in order to meet the 55-Ω impedance target, that is, the impedance of the trace when not subjected to the fields created by changing current in neighboring traces. Note the trace impedance target assumes that the trace is not subjected to the EM fields created by changing current in neighboring traces. It is important to consider the minimum and maximum impedance of a trace based on the switching of neighboring traces when calculating flight times. Using wider spaces between the traces can minimize this trace-to-trace coupling. In addition, these wider spaces reduce settling time.

Coupling between two traces is a function of the coupled length, the distance separating the traces, the signal edge rate, and the degree of mutual capacitance and inductance. In order to minimize the effects of trace-to-trace coupling, the routing guidelines documented in this section should be followed. In addition, all high speed, impedance controlled signals (e.g. FSB signals) should have continuous GND referenced planes and cannot be routed over or under power/GND plane splits.

3.1. Nominal Board Stack-Up

The Intel 852GM chipset based platforms require a board stack-up yielding a target impedance of 55 Ω ± 15%. An example of an 8-layer board stack-up is shown in Figure 2. The left side of the figure illustrates the starting dimensions of the metal and dielectric material thickness as well as drawn trace width dimensions prior to lamination, conductor plating, and etching. After the motherboard materials are laminated, conductors plated, and etched, somewhat different dimensions result. Dielectric materials may become thinner, as under/over etching of conductors alters their trace width, and conductor plating makes them thicker. It is important to note that for the purpose of extracting electrical models from transmission line properties, the final dimensions of signals after lamination, plating, and etching should be used.

The stack-up uses 1.2-mil (1 oz) copper on power planes to reduce I*R drops and 0.6-mil copper thickness on the signal layers: primary side layer (L1), Layer 3 (L3), Layer 6 (L6), and secondary side layer (L8).

To ensure impedance control of 55 Ω, the primary and secondary side layer micro-strip lines should reference solid ground planes on Layer 2 and Layer 7, respectively.

Figure 2. Recommended Board Stack-Up Dimensions

Stackup	Dielectric Thickness (mils)	Layer No.	Layer Type	Copper Weight (oz)	Trace Width (mils)	Trace Impedance (ohms)
S		1	SIGNAL	1/2+plating	5.0	55
PREPREG	5.0					
P		2	PLANE	1		
CORE	5.0					
S		3	SIGNAL	1	4.0	55
PREPREG	12.0					
P		4	PLANE	1		
CORE	10.0					
P		5	PLANE	1		
PREPREG	12.0					
S		6	SIGNAL	1	4.0	55
CORE	5.0					
P		7	PLANE	1		
PREPREG	5.0					
S		8	SIGNAL	1/2+plating	5.0	55

Internal signal traces on Layer 3 and Layer 6 are unbalanced strip-lines. To meet the nominal 55-Ω characteristic impedance for these traces, they reference a solid ground plane on Layer 2 and Layer 7. Since the coupling to Layer 4 and Layer 5 is still significant, (especially true when thinner stack-ups use balanced strip-lines on internal layers) these layers are converted to ground floods in the areas of the motherboard where the speed critical interfaces like the FSB or DDR system memory are routed. In the remaining sections of the motherboard layout the Layer 4 and Layer 5 layers are used for power delivery.

The secondary side layer (L8) is also used for power delivery in many cases, since it benefits from the thick copper plating of the external layer plating as well as referencing the close Layer 7 ground plane. The benefit of such a stack-up is low inductance power delivery.

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3.2. Alternate Stack Ups

OEMs may choose to use different stack-ups (number of layers, thickness, trace width, etc.) from the one example outlined in Figure 2. However, the following key elements should be observed:

1. Final post lamination, post etching, and post plating dimensions should be used for electrical model extractions.
2. Power plane layers should be 1 oz thick and signal layers should be ½ oz thick. External layers become 1 – 1.5 oz (1.2 – 2 mils) thick after plating.
3. All high-speed signals should reference solid ground planes through the length of their routing and should not cross plane splits. To guarantee this, both planes surrounding strip-lines should be GND.
4. Intel recommends that high-speed signal routing be done on internal, strip-line layers.
5. For high-speed signals transitioning between layers next to the component, the signal pins should be accounted for by the GND stitching vias that would stitch all the GND plane layers in that area of the motherboard. Due to the arrangement of the Processor and 852GM GMCH pin-maps, GND vias placed near all GND lands will also be very close to high-speed signals that may be transitioning to an internal layer. Thus, no additional ground stitching vias (besides the GND pin vias) are required in the immediate vicinity of the Processor and 852GM GMCH packages to accompany the signal transitions from the component side into an internal layer.
6. High-speed routing on external layers should be minimized in order to avoid EMI. Routing on external layers also introduces different delays compared to internal layers. This makes it extremely difficult to do length matching if some routing is done on both internal and external layers.
7. If Intel's recommended stackup guidelines are not implemented, then the OEM is liable for all aspects of their board design and simulations should be performed based on OEM stackup (i.e. understanding impacts of SI and power distribution).

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4. Mobile Intel Pentium 4 Processor–M and Mobile Intel Celeron Processor FSB Design Guidelines

The following layout guidelines support designs using the Mobile Intel Pentium 4 Processor–M / Mobile Intel Celeron Processor and the Intel 852GM chipset. Due to on-die Rtt resistors on both the processor and the chipset, additional resistors do not need to be placed on the motherboard for most FSB signals. The exception to these are the RESET# and BPM[5:0]# signals that require a 51.1-Ω pull-up, and the BR0 signal that requires 220-Ω + 5% pull-up to Vtt on the processor end of the transmission line.

4.1. Processor Front Side Bus (FSB) Routing Guidelines

Table 1 summarizes the layout recommendations for the Mobile Intel Pentium 4 Processor–M and expands on specific design issues and their recommendations.

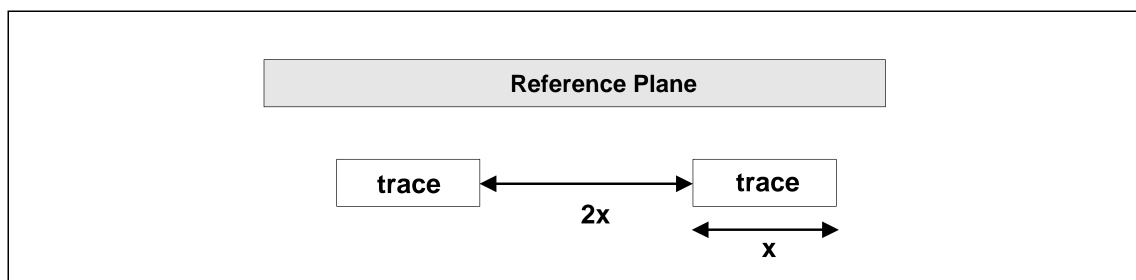
Table 1. Front Side Bus Routing Summary for the Processor

Parameter	Processor Routing Guidelines
Line to line spacing	Greater than or equal to 2:1 edge-to-edge spacing versus trace width. See Figure 3 for an illustration of this recommendation.
Data Line lengths (agent to agent spacing)	0.5 inches–5.5 inches from pin-to-pin. • Data signals of the same source synchronous group should be routed to the same pad-to-pad length within ± 0.100 inches of the associated strobes. • The pad is defined as the attach point of the silicon die to the package substrate. • Length must be added to the system board to compensate for package length differences. • Signals in the same source synchronous group should be routed on the same layer and referenced to Vss with 2:1 spacing.
DSTBn/p[3:0]#	• A data strobe and its complement should be routed within ± 0.025 inches of the same pad-to-pad length. • The pad is defined as the attach point of the silicon die to the package substrate. • Length must be added to the system board to compensate for package length differences. • DSTBn/p# should be routed on the same layer as their associated data group and referenced to Vss.
Address line lengths (agent to agent spacing)	0.5 inches – 6.5 inches from pin-to-pin. • Address signals of the same source synchronous group should be routed to the same Pad-to-Pad length within± 0.200 inches of the associated strobes. • The pad is defined as the attach point of the silicon die to the package substrate. • Length must be added to the system board to compensate for package length differences. • A layer transition may occur if the reference plane remains the same (Vss) and the layers are of the same configuration (all stripline or all microstrip).

Parameter	Processor Routing Guidelines
ADSTBn/p[1:0]#	• An address strobe and its complement should be routed within ± 0.200 of the same Pad-to-Pad length. • The pad is defined as the attach point of the silicon die to the package substrate. • Length must be added to the system board to compensate for package length differences. • A layer transition may occur if the reference plane remains the same (Vss) and the layers are of the same configuration (all stripline or all microstrip).
Common Clock line lengths	0.5 inches – 6.5 inches
Topology	Stripline
Routing priorities	• All associated signals and strobes should be routed on same layer for entire length of bus. • All signals should be referenced to Vss. Ideally, layer changes should not occur for any signals. • If a layer change must occur, reference plane must be Vss and the layers must all be of the same configuration (all stripline or all microstrip for example).
Clock keepout zones	A spacing requirement of 16-20 mils should be maintained around all clocks.
Trace Impedance	55 ohms ± 15%
Source Synchronous routing restrictions	• There are no length-matching routing restrictions between (or within) either the source-synchronous data or address groups. • As long as the strobe and associated line length routing guidelines are met for each group, there is no need to length-match between the groups. For example, one data group may be routed to the minimum allowable length while another data group could be routed to the maximum allowable length. • Simulations have verified that the FSB will still function correctly even under this extreme condition.

Refer to the *Intel® 852GM Chipset GMCH Datasheet* for GMCH package dimensions and refer to the *Mobile Intel® Pentium® 4 Processor–M Datasheet* for processor package dimensions.

Figure 3. Cross-Sectional View of 2:1 Ratio



NOTE: This is the edge-to-edge trace spacing versus width.

A trace spacing to width ratio of 2 to 1 ensures a low crosstalk coefficient (based on geometries defined in 8 layer reference stackup). All the effects of crosstalk are difficult to simulate. The timing and layout guidelines for the processor have been created with the assumption of 2 to 1 trace spacing to width ratio. A smaller ratio would have an unpredictable impact due to crosstalk.

4.1.1. Return Path Evaluation

The return path is the route current takes to return to its source. It may take a path through ground planes, power planes, other signals, integrated circuits, vias, VRMs, etc. Think of the return path as following a path of least impedance back to the original source. Discontinuities in the return path often have signal integrity and timing effects that are similar to the discontinuities in the signal conductor. Therefore, the return paths need to be given similar considerations. A simple way to evaluate return path parasitic inductance is to draw a loop that traces the current from the driver through the signal conductor to the receiver, and then back through the ground/power plane to the driver again. The smaller the area of the loop, the lower the parasitic inductance will be.

The following set of return path rules apply:

- Always trace out the return current path and provide as much care to the return path as the path of the signal conductor.
- Decoupling capacitors do not adequately compensate for a plane split.
- Do not allow splits in the reference planes in the path of the return current.
- Do not allow routing of signals on the reference planes near Front Side Bus signals.
- Maintain Vss as a reference plane for all Front Side Bus signals.
- Do not route over via anti-pads or socket anti-pads.

4.2. Processor Configuration

This section provides more details for routing Mobile Intel Pentium 4 Processor–M- based systems. This information is preliminary and subject to change. Both recommendations and considerations are presented.

For proper operation of the Mobile Pentium 4 Processor-M and the Intel 852GM chipset, it is necessary that the system designer meet the timing and voltage specifications of each component. The following recommendations are Intel's best guidelines based on extensive simulation and experimentation that make assumptions, which may be different than an OEM's system design. The most accurate way to understand the signal integrity and timing of the Front Side Bus in your platform is by performing a comprehensive simulation analysis. It is conceivable that adjustments to trace impedance, line length, termination impedance, board stackup and other parameters can improve system performance.

Refer to the *Mobile Intel® Pentium® 4 Processor–M Datasheet* for a Front Side Bus signal list, signal types and definitions.

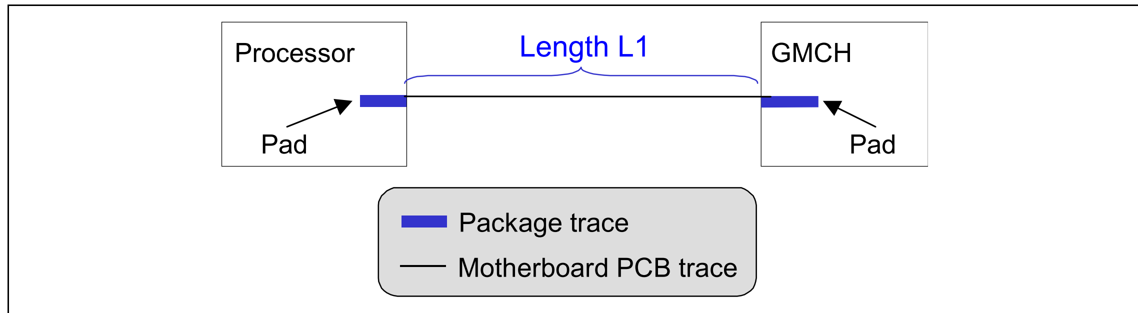
4.3. General Topology and Layout Design Guidelines

The following topology and layout guidelines are based on routing recommendations implemented on Intel Customer reference board. The guidelines are derived from empirical testing with Intel 852GM chipset package models. Below are the design recommendations for the data, address, strobes, and common clock signals. For the following discussion, the pad is defined as the attach point of the silicon die to the package substrate.

4.3.1. Source Synchronous (SS) Signal Group

Source synchronous groups and associated strobes should be routed on the same layer for the entire length of the bus. This results in a significant reduction of the flight time skew since the dielectric thickness, line width, and velocity of the signals will be uniform across a single layer of the stackup. There is no guarantee of a relationship of dielectric thickness, line width, and velocity between layers.

Figure 4. Processor Topology



4.3.1.1. Source Synchronous Data Group

Data signals of the same source synchronous group should be routed to the same **pad-to-pad** length within ± 0.100 of the associated strobes (within the min & max of both strobe). As a result, additional trace will be added to some data nets on the system board in order for all trace lengths within the same data group to be the same length (± 0.100 inches) from the **pad** of the processor to the **associated pad** of the chipset.

A data strobe and its complement should be routed to a length equal to their corresponding data group's mean **pad-to-pad** length ± 0.025 inches.

Equation 1. Calculation to Determine Package Delta Addition to Motherboard Length for UP Systems

$$\text{delta}_{\text{net,strobe}} = (\text{cpu_pkglen}_{\text{net}} - \text{cpu_pkglen}_{\text{strobe*}}) + (\text{cs_pkglen}_{\text{net}} - \text{cs_pkglen}_{\text{strobe}})$$

Refer to the *Intel® 852GM Chipset GMCH Datasheet* for GMCH package dimensions and refer to the *Mobile Intel® Pentium® 4 Processor–M Datasheet* for package dimensions.

Note: * Strobe package length is the average of the strobe pair.

Table 2. Processor Front Side Bus Data Signal Routing Guidelines

Signal Names		Transmission Line Type	Total Trace Length		Nominal Impedance (Ω)	Width & Spacing (mils) 1:3
CPU	GMCH		Min (inches)	Max (inches)		
DBI[3:0]#	DINV[3:0]#	Strip-line	0.5	5.5	55 ± 15%	4 & 12
D[63:0]#	HD[63:0]#	Strip-line	0.5	5.5	55 ±15%	4 & 12
DSTBN[3:0]#	HDSTBN[3:0]#	Strip-line	0.5	5.5	55 ± 15%	4 & 12
DSTBP[3:0]#	HDSTBP[3:0]#	Strip-line	0.5	5.5	55 ±15%	4 & 12

NOTES:
1. The Data signals within each group must be routed to within ± 0.100 inches of its associated “reference” strobe (within the min & max of both strobe).
2. The complement strobe must be routed to within ± 0.025 inches of the associate “reference” strobe.
3. All traces within each signal group must be routed on the same layer (required).
4. Intel recommends that length of the strobes be centered to the average length of associated data or address traces to maximize setup/hold time margins.

4.3.1.2. Source Synchronous Address Group

Address signals follow the same rules as data signals except they should be routed to the same **pad-to-pad** length within ± 0.200 inches of the associated strobes. Address signals may change layers if the reference plane remains Vss.

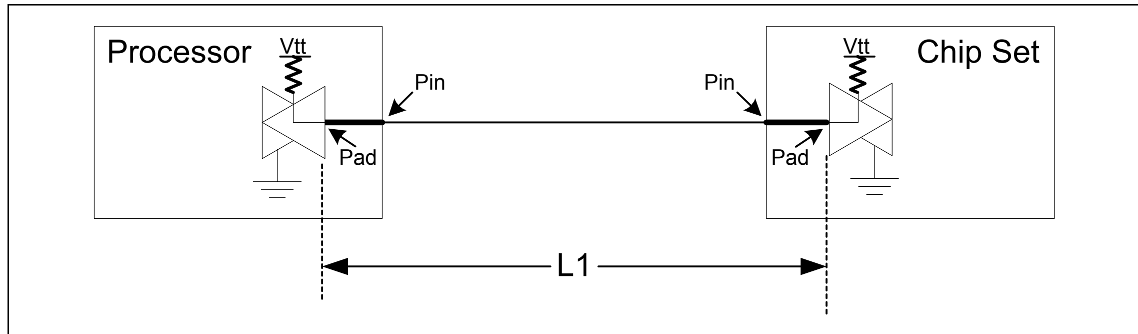
An address strobe should be routed to a length equal to their corresponding signal group's mean **pad-to-pad** length ± 0.025 inches.

Table 3. Processor Front Side Bus Address Signal Routing Guidelines

Signal Names		Transmission Line Type	Total Trace Length		Nominal Impedance (Ω)	Width & Spacing (mils)
CPU	GMCH		Min (inches)	Max (inches)		
A[31:3]#	HA[31:3]#	Strip-line	0.5	6.5	55 ± 15%	4 & 8
REQ[4:0]#	HREQ[4:0]#	Strip-line	0.5	6.5	55 ± 15%	4 & 8
ADSTB[1:0]#	HADSTB[1:0]#	Strip-line	0.5	6.5	55 ± 15%	4 & 8

NOTES:
1. The Address signals within each group must be routed to within ± 0.200 of its associated strobe.
2. All traces within each signal group must be routed on the same layer (required).
3. It is recommended that length of the strobes be centered to the average length of associated data or address traces to maximize setup/hold time margins.

Figure 5. SS Topology for Address and Data



4.3.2. FSB Data and Address Routing Example

Figure 6, Figure 7, Figure 8, and Figure 9 provide examples of a board routing for the Data signal group. The majority of the Data signal route is on an internal layer; both external layers can be used for parallel termination R-pack placement.

Figure 6. FSB Host Data Routing Example Layer 3

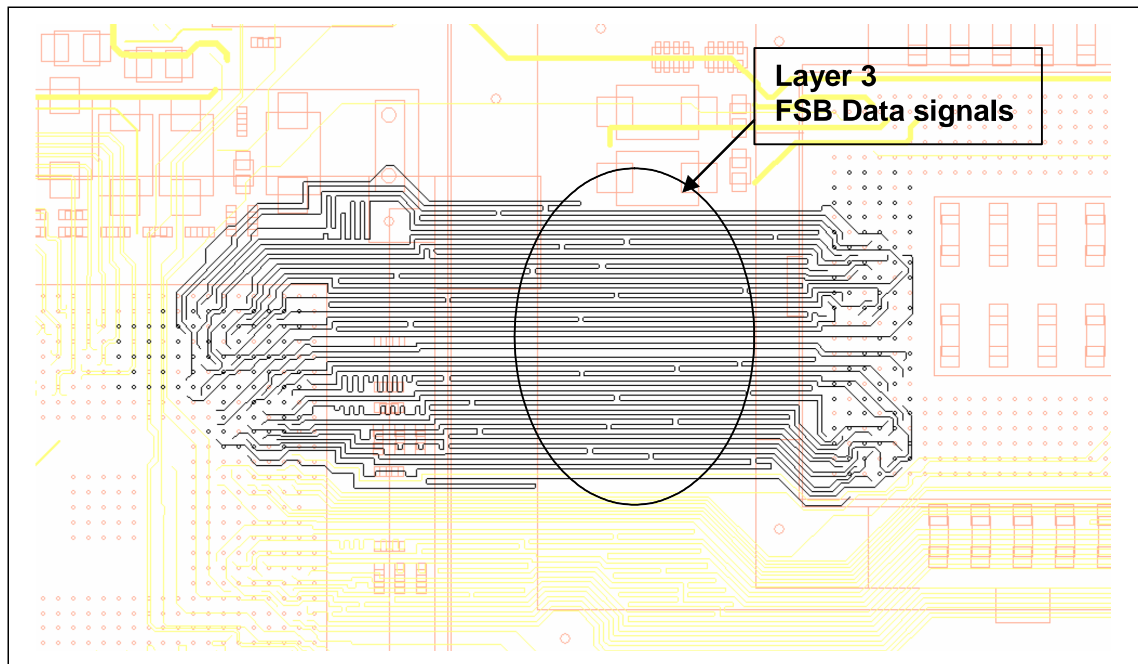


Figure 7. FSB Host Address Routing Example Layer 3

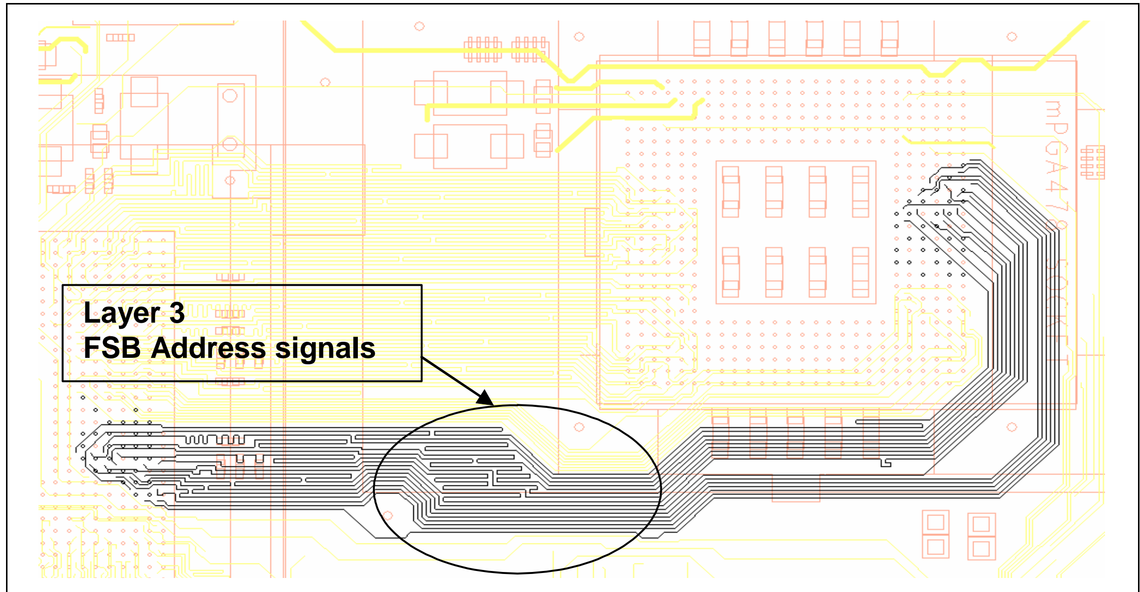


Figure 8. FSB Host Data Routing Example Layer 6

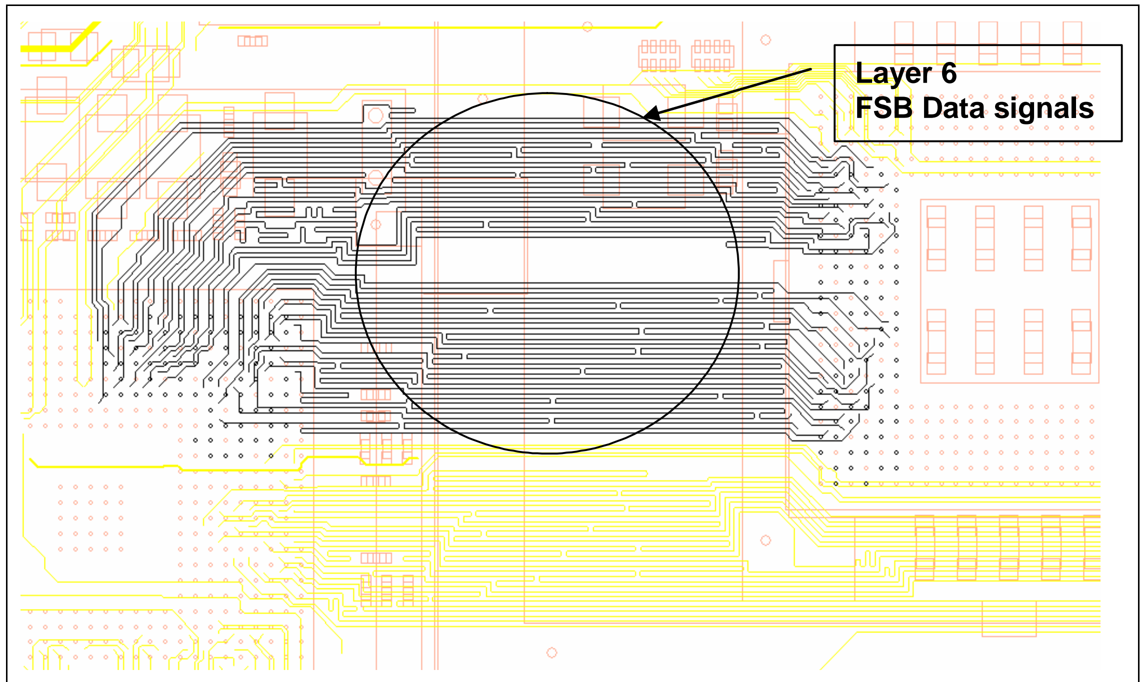
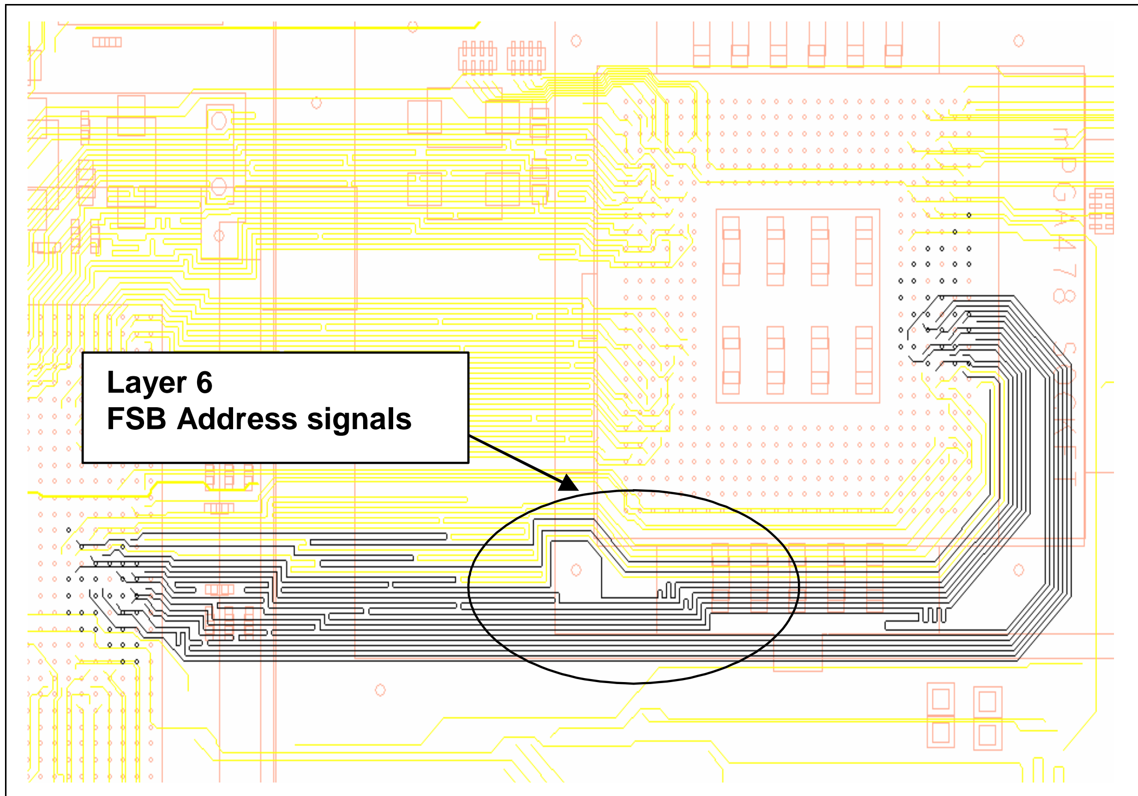


Figure 9. FSB Host Address Routing Example Layer 6



4.3.3. Common Clock (CC) AGTL+ Signal Group

Common clock signals should be routed to a minimum pin-to-pin motherboard length of **0.5** inches and a maximum motherboard length of **6.5** inches.

Table 4. Processor Front Side Bus Control Signal Routing Guidelines

Signal Names		Topology	Routing Trace Length (Pin-to-Pin)		Nominal Impedance (ohms)	Width & Spacing (mils)
CPU	GMCH		Max (inches)	Min (inches)		
RESET#	CPURST#	Stripline	6.5	0.5	55 ± 15%	4 & 8
BR0#	BREQ0#	Stripline	6.5	0.5	55 ± 15%	4 & 8
BNR#	BNR#	Stripline	6.5	0.5	55 ± 15%	4 & 8
REQ[4:0]#	HREQ[4:0]#	Stripline	6.5	0.5	55 ± 15%	4 & 8
BPRI#	BPRI#	Stripline	6.5	0.5	55 ± 15%	4 & 8
DEFER#	DEFER#	Stripline	6.5	0.5	55 ± 15%	4 & 8
LOCK#	HLOCK#	Stripline	6.5	0.5	55 ± 15%	4 & 8
TRDY#	HTRDY#	Stripline	6.5	0.5	55 ± 15%	4 & 8
DRDY#	DRDY#	Stripline	6.5	0.5	55 ± 15%	4 & 8
ADS#	ADS#	Stripline	6.5	0.5	55 ± 15%	4 & 8
DBSY#	DBSY#	Stripline	6.5	0.5	55 ± 15%	4 & 8
HIT#	HIT#	Stripline	6.5	0.5	55 ± 15%	4 & 8
HITM#	HITM#	Stripline	6.5	0.5	55 ± 15%	4 & 8
RS[2:0]#	RS[2:0]#	Stripline	6.5	0.5	55 ± 15%	4 & 8

NOTES:
1. Trace width of 4 mils and trace spacing of 8 mils within signal groups. Entire trace for each signal routed on one layer (recommended)
2. RESET# and BR0# are common clock AGTL+ signals without ODT (On die termination). These signals require an external Rtt. The Rtt should be placed near CPU: L2<= 0.5 inches. Rtt = 51.1 ±1%.

4.3.4. Asynchronous AGTL+ Signals

All signals must meet the AC and DC specifications as documented in the *Mobile Intel® Pentium® 4 Processor–M Datasheet.*

4.3.4.1. Topology 1A: Open Drain (OD) Signals Driven by the Processor – IERR# and FERR#

The Topology 1A OD signals IERR# and FERR# should adhere to the following routing and layout recommendations. Table 5 lists the recommended routing requirements for the IERR# and FERR# signals of the Mobile Intel Pentium 4 Processor–M. The routing guidelines allow the signal to be routed

as either micro-strip or strip-lines using 55 Ω ± 15% characteristic trace impedance. The pull-up voltage for termination resistor Rtt is VCCP.

Due to the dependencies on system design implementation, IERR# can be implemented in a number of ways to meet design goals. IERR# can be routed as a test point or to any optional system receiver. It is recommended that the FERR# signal of the Intel Mobile Intel Pentium 4 Processor–M be routed to the FERR# signal of the Intel ICH4-M.

Figure 10. Routing Illustration for Topology 1A

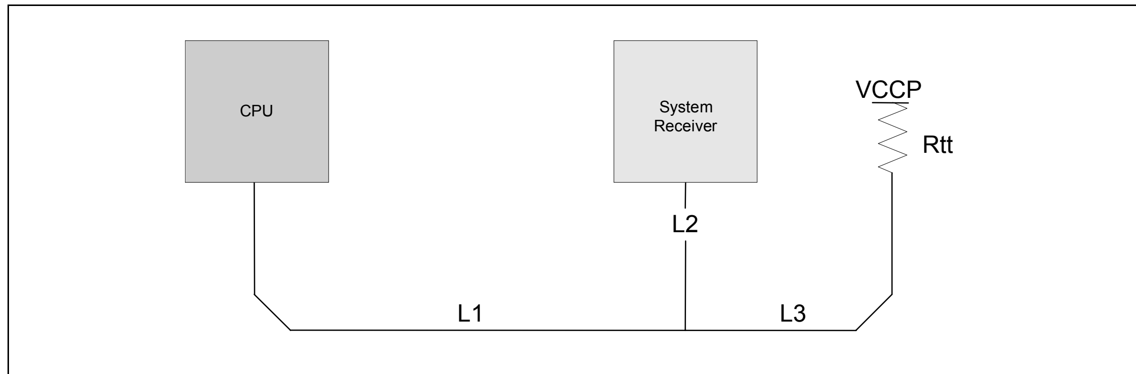


Table 5. Layout Recommendations for Topology 1A

L1	L2	L3	Rtt	Transmission Line Type
0.5” – 12.0”	0” – 3.0”	0” – 3.0”	56 Ω ± 5%	Micro-strip
0.5” – 12.0”	0” – 3.0”	0” – 3.0”	56 Ω ± 5%	Strip-line

4.3.4.2. Topology 1B: Open Drain (OD) Signals Driven by the Processor – THERMTRIP#

The Topology 1B OD signal THERMTRIP# should adhere to the following routing and layout recommendations. Table 6 lists the recommended routing requirements for the THERMTRIP# signals of the Mobile Intel Pentium 4 Processor–M. The routing guidelines allow the signal to be routed as either micro-strip or strip-lines using 55 Ω ± 15% characteristic trace impedance. The pull-up voltage for termination resistor Rtt is VCCP.

THERMTRIP# can be implemented in a number of ways to meet design goals. It can be routed to the ICH4-M or any optional system receiver. Intel recommneds that the THERMTRIP# signal of the Mobile Intel Pentium 4 Processor–M be routed to the THRMTRIP# signal of the ICH4-M. The ICH4-M’s THRMTRIP# signal is a new signal to the I/O controller hub architecture that allows the ICH4-M to quickly put the whole system into an S5 state whenever the catastrophic thermal trip point has been reached.

Figure 11. Routing Illustration for Topology 1B

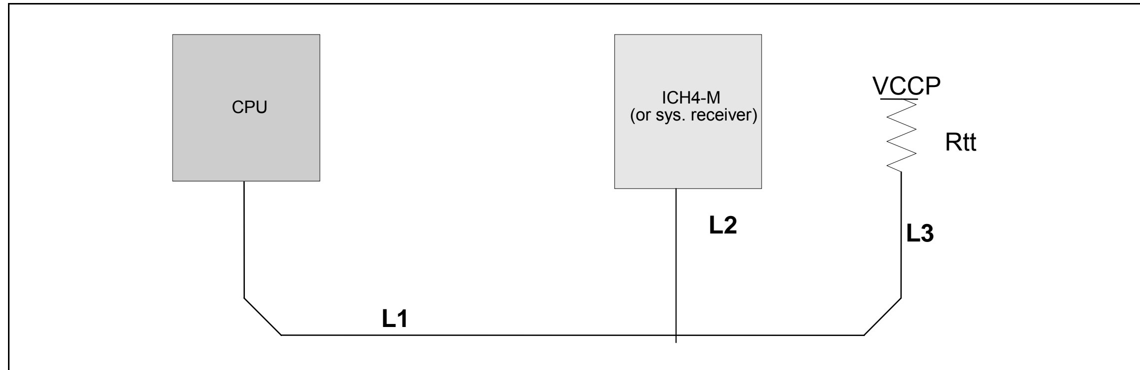


Table 6. Layout Recommendations for Topology 1B

L1	L2	L3	Rtt	Transmission Line Type
0.5" – 12.0"	0" – 3.0"	0" – 3.0"	56 Ω ± 5%	Micro-strip
0.5" – 12.0"	0" – 3.0"	0" – 3.0"	56 Ω ± 5%	Strip-line

4.3.4.3. Topology 1C: Open Drain (OD) Signals Driven by the Processor – PROCHOT#

The Topology 1C OD signal PROCHOT#, should adhere to the following routing and layout recommendations. Table 7 lists the recommended routing requirements for the PROCHOT# signal. The routing guidelines allow the signal to be routed as either a micro-strip or strip-line using 55 Ω ± 15% characteristic trace impedance. Figure 12 shows the recommended implementation for providing voltage translation between the processor's PROCHOT# signal and a system receiver that utilizes a 3.3-V interface voltage (shown as VCCP).

Series resistor Rs is a component of the voltage translation logic and serves as a driver isolation resistor. Rs is shown separated by distance L3 from the first bipolar junction transistor (BJT), Q1, to emphasize the placement of Rs with respect to Q1. The placement of Rs a distance L3 before the Q1 BJT is a specific implementation of the generalized voltage translator circuit shown in Figure 17. Rs should be placed at the beginning of the T-split from the PROCHOT# signal. The pull-up voltage for termination resistor Rtt is VCCP.

Intel recommends that PROCHOT# be routed using the voltage translation logic shown in Figure 12.

Figure 12. Routing Illustration for Topology 1C

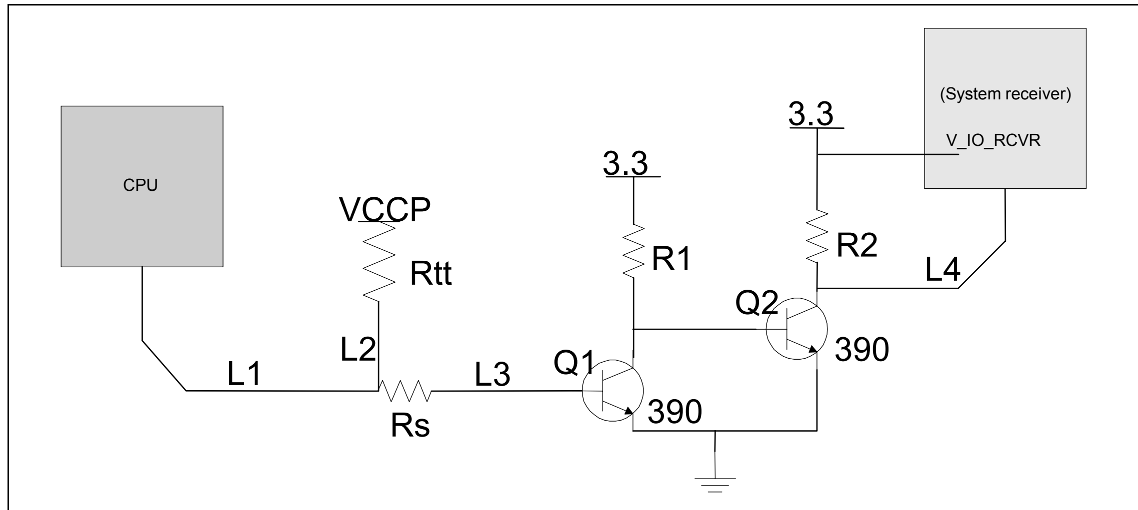


Table 7. Layout Recommendations for Topology 1C

L1	L2	L3	L4	Rs	R1	R2	Rtt	Transmission Line Type
0.5 – 12.0”	0 - 3.0”	0 – 3.0”	0.5 – 12.0”	330 Ω ± 5%	1.3 kΩ ± 5 %	330 Ω ± 5%	56 Ω ± 5%	Micro-strip
0.5 – 12.0”	0 - 3.0”	0 – 3.0”	0.5 – 12.0”	330 Ω ± 5%	1.3 kΩ ± 5%	330 Ω ± 5%	56 Ω ± 5%	Strip-line

4.3.4.4. Topology 2A: Open Drain (OD) Signals Driven by ICH4-M – PWRGOOD

The Topology 2A OD signal PWRGOOD should adhere to the following routing and layout recommendations.

Table 8 lists the recommended routing requirements for the PWRGOOD signal of the Mobile Intel Pentium 4 Processor–M. The routing guidelines allow the signal to be routed as either micro-strip or strip-lines using 55 Ω ± 15% characteristic trace impedance. The pull-up voltage for termination resistor Rtt is VCCP. Note that the Intel ICH4-M’s CPUPWRGD signal should be routed point-to-point to the Mobile Intel Pentium 4 Processor–M’s PWRGOOD signal. The routing from the Mobile Intel Pentium 4 Processor–M’s PWRGOOD pin should fork out to both to the termination resistor, Rtt, and the ICH4-M. Segments L1 and L2 from Figure 13 should not T-split from a trace from the Mobile Intel Pentium 4 Processor–M pin.

Figure 13. Routing Illustration for Topology 2A

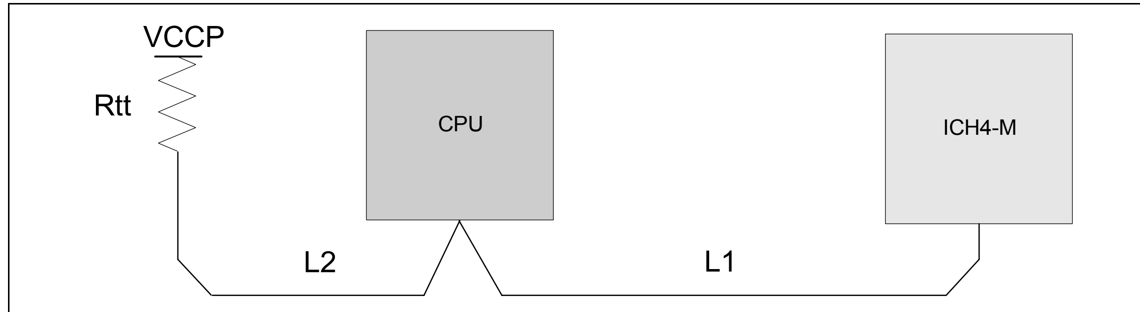


Table 8. Layout Recommendations for Topology 2A

L1	L2	Rtt	Transmission Line Type
0.5” – 12.0”	0” – 3.0”	300 Ω ± 5%	Micro-strip
0.5” – 12.0”	0” – 3.0”	300 Ω ± 5%	Strip-line

4.3.4.5. Topology 2B: CMOS Signals Driven by ICH4-M – DPSLP#

The Topology 2B CMOS DPSLP# signal should adhere to the following routing and layout recommendations illustrated in Figure 14. As listed in Table 9, the L1 and L2 segments of the DPSLP# signal topology can be routed as either micro-strip or strip-lines using 55 Ω ± 15% characteristic trace impedance. Note that the Intel ICH4-M’s DPSLP# signal should be routed point-to-point with the daisy chain topology shown. The routing of DPSLP# at the CPU should fork out to both the ICH4-M and the GMCH. Segments L1 and L2 from Figure 14 should not T-split from a trace from the Mobile Intel Pentium 4 Processor–M pin.

Figure 14. Routing Illustration for Topology 2B

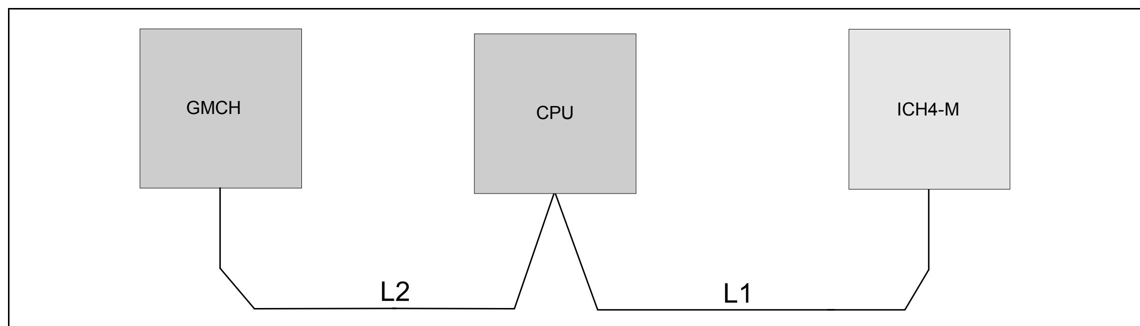


Table 9. Layout Recommendations for Topology 2B

L1	L2	Transmission Line Type
0.5” – 12.0”	0.5” – 6.5”	Micro-strip
0.5” – 12.0”	0.5” – 6.5”	Strip-line

4.3.4.6. Topology 2C: CMOS Signals Driven by ICH4-M – A20M#, IGNNE#, LINT0/INTR, LINT1/NMI, SLP#, SMI#, and STPCLK#

The Topology 2C CMOS A20M#, IGNNE#, LINT0/INTR, LINT1/NMI, SLP#, SMI#, and STPCLK# signals should implement a point-to-point connection between the ICH4-M and the Mobile Intel Pentium 4 Processor–M. The routing guidelines allow both signals to be routed as either micro-strip or strip-lines using 55 Ω ± 15% characteristic trace impedance. No additional motherboard components are necessary for this topology.

Figure 15. Routing Illustration for Topology 2C

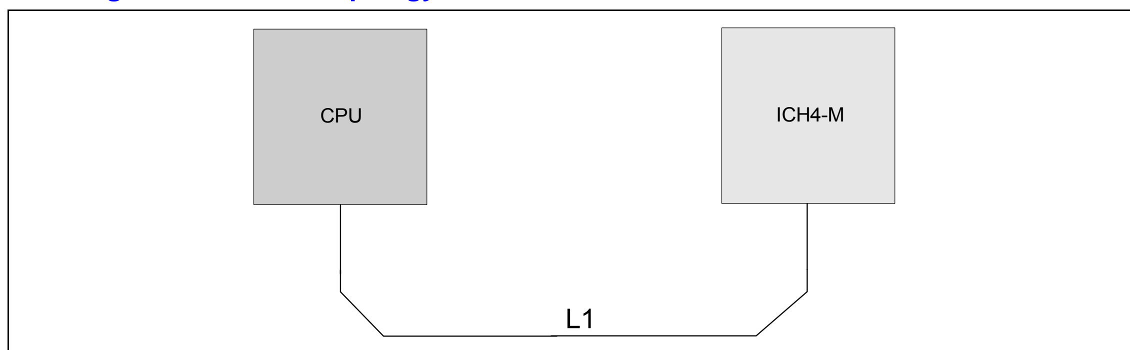


Table 10. Layout Recommendations for Topology 2C

L1	Transmission Line Type
0.5" – 12.0"	Micro-strip
0.5" – 12.0"	Strip-line

4.3.4.7. Topology 3: CMOS Signals Driven by ICH4-M to CPU and FWH – INIT#

The signal INIT# should adhere to the following routing and layout recommendations.

Table 11 lists the recommended routing requirements for the INIT# signal of the ICH4-M. The routing guidelines allow both signals to be routed as either micro-strip or strip-lines using 55 Ω ± 15% characteristic trace impedance.

Figure 16 shows the recommended implementation for providing voltage translation between the ICH4-M's INIT# voltage signaling level and any firmware hub (FWH) that utilizes a 3.3-V interface voltage (shown as a supply 3.3V). For convenience, the entire topology and required transistors and resistors for the voltage translator is shown in Figure 16.

Series resistor Rs is a component of the voltage translator logic circuit and serves as a driver isolation resistor. Rs is shown separated by distance L3 from the first bipolar junction transistor (BJT), Q1, to emphasize the placement of Rs with respect to Q1. The routing recommendations of transmission line L3 in Figure 16 is listed in

Table 11 and Rs should be placed at the beginning of the T-split of the trace from the ICH4-M's INIT# pin.

Figure 16. Routing Illustration for Topology 3

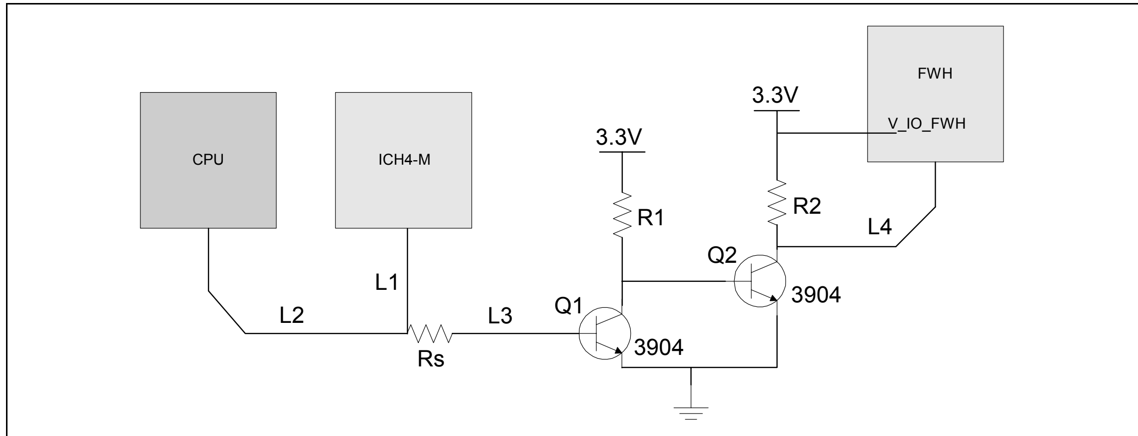
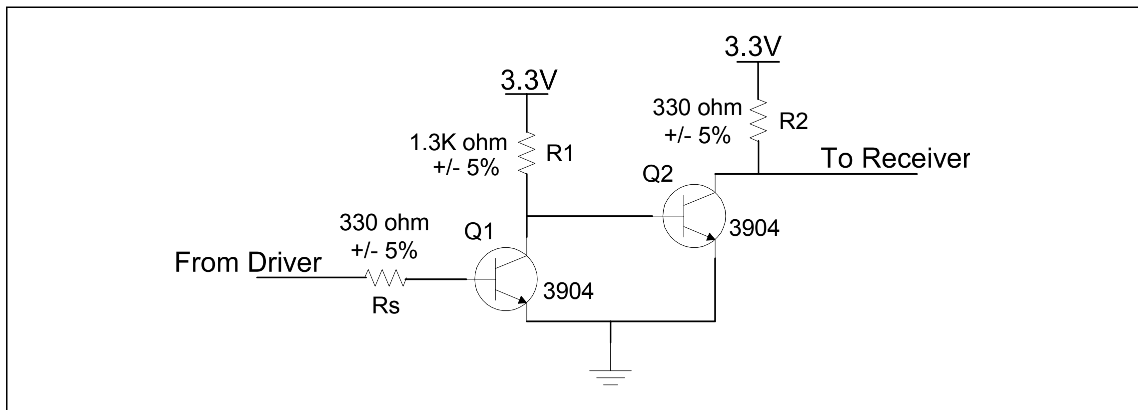


Table 11. Layout Recommendations for Topology 3

L1 + L2	L3	L4	Rs	R1	R2	Transmission Line Type
0.5" – 12.0"	0" – 3.0"	0.5" – 6.0"	300 Ω ± 5%	2kΩ ± 5%	300 Ω ± 5%	Micro-strip
0.5" – 12.0"	0" – 3.0"	0.5" – 6.0"	300 Ω ± 5%	2kΩ ± 5%	300 Ω ± 5%	Strip-line

Figure 17. Voltage Translation Circuit for 3.3-V Receivers



4.4. ITP Debug Port

Please refer to the *ITP700 Debug Port Design Guide*, which can be found on http://developer.intel.com/design/Xeon/guides/249679.htm.

Note: This change is effective for all future processors and includes information on both ITP700 and ITP700 Flex.

4.4.1. Logic Analyzer Interface (LAI)

Intel is working with two logic analyzer vendors to provide logic analyzer interfaces (LAIs) for use in debugging the Mobile Intel Pentium 4 Processor–M based system. Tektronix* and Agilent* should be contacted to get specific information about their logic analyzer interfaces. The following information is general in nature. Specific information must be obtained from the logic analyzer vendor.

Due to the complexity of the Mobile Intel Pentium 4 Processor–M based system, the LAI is critical in providing the ability to probe and capture Front Side Bus signals. There are two sets of considerations to keep in mind when designing a Mobile Intel Pentium 4 Processor–M that can make use of an LAI: mechanical and electrical.

4.4.1.1. Mechanical Considerations

The LAI is installed between the processor socket and the Mobile Intel Pentium 4 Processor–M. The LAI pins plug into the socket, while the Mobile Intel Pentium 4 Processor–M plugs into a socket on the LAI. Cabling that is part of the LAI egresses the system to allow an electrical connection between the Mobile Intel Pentium 4 Processor–M and a logic analyzer. The maximum volume occupied by the LAI, known as the keepout volume, as well as the cable egress restrictions, should be obtained from the logic analyzer vendor. System designers must make sure that the keepout volume remains unobstructed inside the system. Note that it is possible that the keepout volume reserved for the LAI may include space normally occupied by the Mobile Intel Pentium 4 Processor–M heat sink. If this is the case, the logic analyzer vendor will provide a cooling solution as part of the LAI.

4.4.1.2. Electrical Considerations

The LAI will also affect the electrical performance of the Front Side Bus; therefore, it is critical to obtain electrical load models from each of the logic analyzers in order to run system level simulations to prove that their tool will work in the system. Contact the logic analyzer vendor for electrical specifications and load models for the LAI solution they provide.

4.5. Mobile Intel Pentium 4 Processor–M and Intel 852GM Chipset FSB Signal Package Lengths

Table 12 lists the preliminary package trace lengths of the Mobile Intel Pentium 4 Processor–M and the Intel 852GM GMCH for the source synchronous data and address signals. Refer to Section 4.3.1 for further details. The Mobile Intel Pentium 4 Processor–M and Intel 852GM GMCH package traces are routed as micro-strip lines with a nominal characteristic impedance of 55 Ω ± 15%.

Table 12. Mobile Intel Pentium 4 Processor-M and Intel 852GM Chipset Package Lengths

Processor lengths			GMCH Lengths		
Signal	**Processor Ball**	**Length (inches)**	**Signal**	**GMCH ball**	**Length (mils)**
Address Group 0					
ADSTB[0]#	L5	0.210	HADSTB[0]#	T26	419
A[3]#	K2	0.368	HA[3]#	P23	468
A[4]#	K4	0.265	HA[4]#	T25	353

Processor lengths			GMCH Lengths		
A[5]#	L6	0.155	HA[5]#	T28	551
A[6]#	K1	0.415	HA[6]#	R27	523
A[7]#	L3	0.304	HA[7]#	U23	274
A[8]#	M6	0.144	HA[8]#	U24	333
A[9]#	L2	0.372	HA[9]#	R24	327
A[10]#	M3	0.327	HA[10]#	U28	560
A[11]#	M4	0.246	HA[11]#	V28	566
A[12]#	N1	0.394	HA[12]#	U27	522
A[13]#	M1	0.408	HA[13]#	T27	501
A[14]#	N2	0.349	HA[14]#	V27	562
A[15]#	N4	0.241	HA[15]#	U25	375
A[16]#	N5	0.198	HA[16]#	V26	491
REQ[0]#	J1	0.427	HREQ[0]#	R28	569
REQ[1]#	K5	0.207	HREQ[1]#	P25	378
REQ[2]#	J4	0.270	HREQ[2]#	R23	247
REQ[3]#	J3	0.337	HREQ[3]#	R25	383
REQ[4]#	H3	0.356	HREQ[4]#	T23	276
Address Group 1					
ADSTB[1]#	R5	0.214	HADSTB[1]#	AA26	504
A[17]#	T1	0.470	HA[17]#	Y24	457
A[18]#	R2	0.404	HA[18]#	V25	389
A[19]#	P3	0.303	HA[19]#	V23	284
A[20]#	P4	0.246	HA[20]#	W25	414
A[21]#	R3	0.334	HA[21]#	Y25	429
A[22]#	T2	0.388	HA[22]#	AA27	545
A[23]#	U1	0.458	HA[23]#	W24	382
A[24]#	P6	0.156	HA[24]#	W23	353
A[25]#	U3	0.379	HA[25]#	W27	536
A[26]#	T4	0.281	HA[26]#	Y27	556
A[27]#	V2	0.417	HA[27]#	AA28	631
A[28]#	R6	0.166	HA[28]#	W28	579
A[29]#	W1	0.493	HA[29]#	AB27	558
A[30]#	T5	0.217	HA[30]#	Y26	484
A[31]#	U4	0.285	HA[31]#	AB28	617
Data Group 0					
DSTBN[0]#	E22	0.338	HDSTBN[0]#	J28	763
DSTBP[0]#	F21	0.326	HDSTBP[0]#	K27	662

Processor lengths			GMCH Lengths		
D[0]#	B21	0.414	HD[0]#	K22	329
D[1]#	B22	0.475	HD[1]#	H27	620
D[2]#	A23	0.538	HD[2]#	K25	438
D[3]#	A25	0.608	HD[3]#	L24	387
D[4]#	C21	0.386	HD[4]#	J27	600
D[5]#	D22	0.386	HD[5]#	G28	693
D[6]#	B24	0.535	HD[6]#	L27	518
D[7]#	C23	0.464	HD[7]#	L23	329
D[8]#	C24	0.515	HD[8]#	L25	458
D[9]#	B25	0.590	HD[9]#	J24	438
D[10]#	G22	0.274	HD[10]#	H25	504
D[11]#	H21	0.203	HD[11]#	K23	319
D[12]#	C26	0.589	HD[12]#	G27	620
D[13]#	D23	0.462	HD[13]#	K26	494
D[14]#	J21	0.183	HD[14]#	J23	393
D[15]#	D25	0.550	HD[15]#	H26	554
DBI[0]#	E21	0.309	DINV[0]#	J25	514
Data Group 1					
DSTBN[1]#	K22	0.301	HDSTBN[1]#	C27	788
DSTBP[1]#	J23	0.306	HDSTBP[1]#	D26	736
D[16]#	H22	0.272	HD[16]#	F25	593
D[17]#	E24	0.480	HD[17]#	F26	634
D[18]#	G23	0.358	HD[18]#	B27	834
D[19]#	F23	0.418	HD[19]#	H23	412
D[20]#	F24	0.443	HD[20]#	E27	714
D[21]#	E25	0.508	HD[21]#	G25	522
D[22]#	F26	0.513	HD[22]#	F28	731
D[23]#	D26	0.597	HD[23]#	D27	766
D[24]#	L21	0.176	HD[24]#	G24	493
D[25]#	G26	0.524	HD[25]#	C28	837
D[26]#	H24	0.412	HD[26]#	B26	815
D[27]#	M21	0.171	HD[27]#	G22	453
D[28]#	L22	0.245	HD[28]#	C26	768
D[29]#	J24	0.401	HD[29]#	E26	691
D[30]#	K23	0.313	HD[30]#	G23	464
D[31]#	H25	0.473	HD[31]#	B28	914
DBI[1]#	G25	0.458	DINV[1]#	E25	628

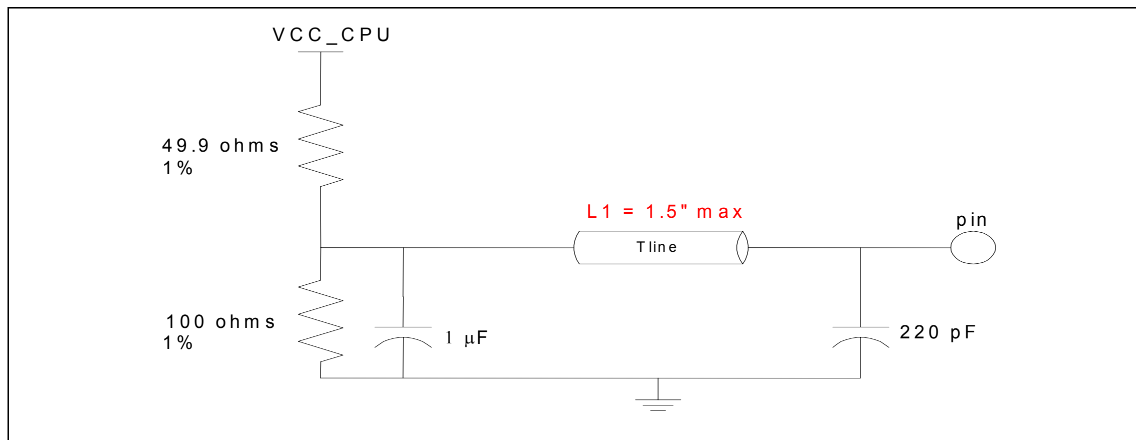
Processor lengths			GMCH Lengths		
Data Group 2					
DSTBN[2]#	K22	0.252	HDSTBN[2]#	E22	538
DSTBP[2]#	J23	0.266	HDSTBP[2]#	E21	502
D[32]#	M23	0.300	HD[32]#	B21	664
D[33]#	N22	0.226	HD[33]#	G21	501
D[34]#	P21	0.178	HD[34]#	C24	683
D[35]#	M24	0.371	HD[35]#	C23	675
D[36]#	N23	0.271	HD[36]#	D22	633
D[37]#	M26	0.454	HD[37]#	C25	747
D[38]#	N26	0.437	HD[38]#	E24	619
D[39]#	N25	0.383	HD[39]#	D24	655
D[40]#	R21	0.165	HD[40]#	G20	358
D[41]#	P24	0.343	HD[41]#	E23	608
D[42]#	R25	0.381	HD[42]#	B22	828
D[43]#	R24	0.329	HD[43]#	B23	726
D[44]#	T26	0.420	HD[44]#	F23	563
D[45]#	T25	0.380	HD[45]#	F21	460
D[46]#	T22	0.221	HD[46]#	C20	647
D[47]#	T23	0.279	HD[47]#	C21	654
DBI[2]#	P26	0.441	DINV[2]#	B25	784
Data Group 3					
DSTBN[3]#	W22	0.298	HDSTBN[3]#	D18	505
DSTBP[3]#	W23	0.300	HDSTBP[3]#	E18	463
D[48]#	U26	0.419	HD[48]#	G18	372
D[49]#	U24	0.324	HD[49]#	E19	511
D[50]#	U23	0.270	HD[50]#	E20	548
D[51]#	V25	0.384	HD[51]#	G17	326
D[52]#	U21	0.167	HD[52]#	D20	575
D[53]#	V22	0.252	HD[53]#	F19	469
D[54]#	V24	0.341	HD[54]#	C19	598
D[55]#	W26	0.447	HD[55]#	C17	541
D[56]#	Y26	0.454	HD[56]#	F17	372
D[57]#	W25	0.426	HD[57]#	B19	649
D[58]#	Y23	0.336	HD[58]#	G16	347
D[59]#	Y24	0.386	HD[59]#	E16	490
D[60]#	Y21	0.222	HD[60]#	C16	522
D[61]#	AA25	0.426	HD[61]#	E17	431

Processor lengths			GMCH Lengths		
D[62]#	AA22	0.268	HD[62]#	D16	509
D[63]#	AA24	0.394	HD[63]#	C18	579
DBI[3]#	V21	0.202	DINV[3]#	G19	431

4.5.1. Mobile Intel Pentium 4 Processor-M GTLREF Layout and Routing Recommendations

There are four AGTL+ GTLREF pins on the processor that are used to set the reference voltage level for the AGTL+ signals (GTLREF). Because all of these pins are connected inside the processor package, the GTLREF voltage only needs to be supplied to one of the four pins. The other three pins can be left unconnected.

Figure 18. GTLREF Routing



- The processor must have one dedicated voltage divider.
- Decouple the voltage divider with a 1-µF capacitor.
- Keep the voltage divider within 1.5 inches of the GTLREF pin
- Decouple each pin with a high frequency capacitor (such as a 220 pF 603) as close to the pin as possible
- Keep signal routing at least 10 mils separated from the GTLREF routes. Use a minimum of a 7-mil trace for routing.
- Do not allow signal lines to use the GTLREF routing as part of their return path (i.e., do not allow the GTLREF routing to create splits or discontinuities in the reference planes of the Front Side Bus signals.)

4.5.2. AGTL+ I/O Buffer Compensation

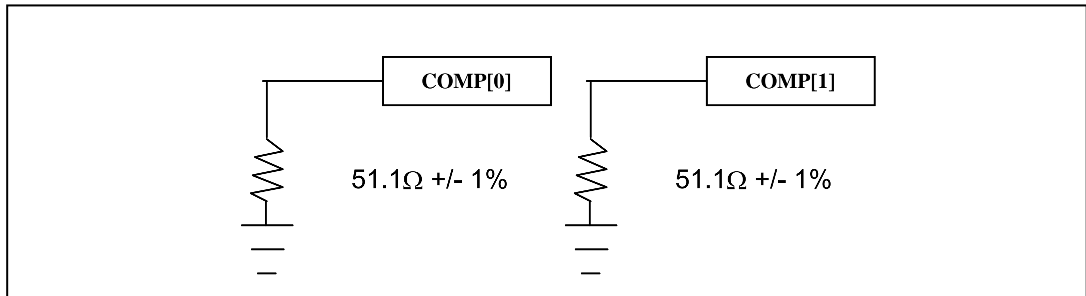
The Mobile Intel Pentium 4 Processor–M has 2 pins, COMP[1:0], and the Intel 852GM chipset GMCH has 2 pins, HXRCOMP and HYRCOMP, that require compensation resistors to adjust the AGTL+ I/O buffer characteristics to specific board and operating environment characteristics. Also, the GMCH requires two special reference voltage generation circuits to pins HXSWING and HYSWING for the

same purpose described above. Refer to the *Mobile Intel® Pentium® 4 Processor–M Datasheet* and *Intel® 852GM GMCH Chipset Datasheet* for details on resistive compensation.

4.5.2.1. Mobile Intel Pentium 4 Processor–M AGTL+ I/O Buffer Compensation

For the Mobile Intel Pentium 4 Processor–M, the COMP[1:0] pins (see Figure 19) must each be pulled-down to ground with 51.1 Ω ± 1% resistors and should be connected to the Mobile Intel Pentium 4 Processor–M processor with a Zo = 51.1 Ω trace that is less than 0.5 inches from the processor pins. COMP[1:0] traces should be at least 25 mils (> 50 mils preferred) away from any other toggling signal.

Figure 19. Mobile Intel Pentium 4 Processor-M COMP[1:0] Resistive Compensation



5. Intel Celeron M Processor Front Side Bus Design Guidelines

The following layout guidelines support designs using the Intel Celeron M processor and the Intel 852GM GMCH chipset. Due to on-die Rtt resistors on both the processor and the chipset, additional resistors do not need to be placed on the motherboard for most FSB signals. A simple point-to-point interconnect topology is used in these cases.

5.1. Intel Celeron M Processor Front Side Bus Design Recommendations

For proper operation of the Intel Celeron M processor and the GMCH FSB interface, it is necessary that the system designer meet the timing and voltage specification of each component. The following recommendations are Intel's best guidelines based on extensive simulation and experimentation that make assumptions, which may be different than an OEM's system design. The most accurate way to understand the signal integrity and timing of the FSB in your platform is by performing a comprehensive simulation analysis. It is possible that adjustments to trace impedance, line length, termination impedance, board stack-up, and other parameters can be made that improve system performance.

Refer to the *Intel® Celeron® M Processor Datasheet* for a FSB signal list, signal types, and definitions. Below are the design recommendations for the data, address, and strobes. For the following discussion, the pad is defined as the attach point of the silicon die to the package substrate. The following topology and layout guidelines are preliminary and subject to change. The guidelines are derived from empirical testing with GMCH package models.

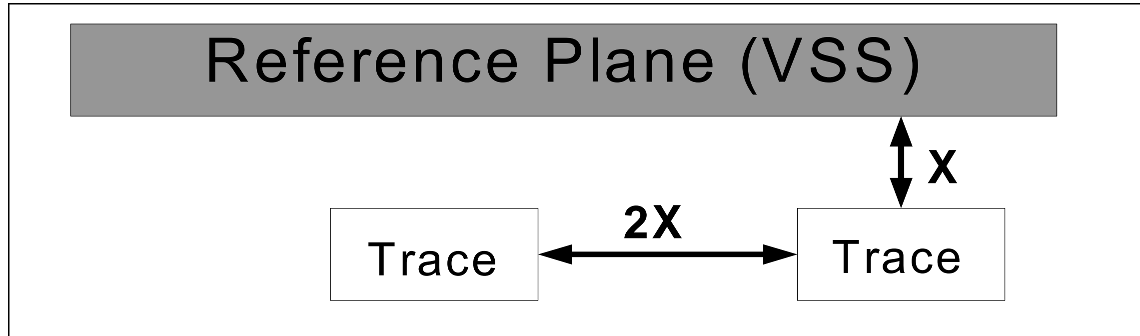
5.2. Recommended Stack-up Routing and Spacing Assumptions

The following section describes in more detail, the terminology and definitions used for different routing and stack-up assumptions that apply to the recommended motherboard stack-up shown in Section 3.1.

5.2.1. Trace Space to Trace – Reference Plane Separation Ratio

Figure 22 illustrates the recommended relationship between the edge-to-edge trace spacing (2X) versus the trace to reference plane separation (X). An edge-to-edge trace spacing (2X) to trace – reference plane separation (X) ratio of 2 to 1 ensures a low crosstalk coefficient. All the effects of crosstalk are difficult to simulate. The timing and layout guidelines for the processor have been created with the assumption of a 2:1 trace spacing to reference plane ratio. A smaller ratio would have an unpredictable impact due to crosstalk.

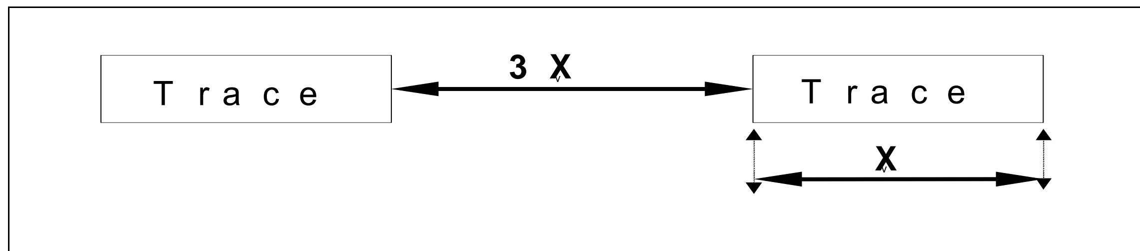
Figure 22. Trace Spacing vs. Trace to Reference Plane Example



5.2.2. Trace Space to Trace Width Ratio

Figure 20 illustrates the recommended relationship between the edge-to-edge trace spacing versus trace width ratio for the best signal quality results. In general, a 3:1 trace space to trace width ratio is preferred and highly recommended. In case of routing difficulties on the motherboard, using a 2:1 ratio would be acceptable **only** if additional simulations conclude that it is possible, which may include some changes to the stack-up or routing assumptions.

Figure 23. Three to One Trace Spacing to Trace Width Example



5.3. Common Clock Signals

All common clock signals use an AGTL+ bus driver technology with on die integrated GTL termination resistors connected in a point-to-point, Zo = 55 Ω, controlled impedance topology between the processor and the GMCH. No external termination is needed on these signals. These signals operate at the FSB frequency of 100 MHz.

Common clock signals should be routed on an internal layer while referencing solid ground planes. Based on current simulation results, routing on internal layers allows for a minimum pin-to-pin motherboard length of approximately 1.0 inch and a maximum of 6.5 inches. Trace length matching for the common clock signals is not required. For details on minimum motherboard trace length requirements, please refer to Section 4.9.3.3 and Table 13 for more details. Intel recommends routing these signals on the same internal layer for the entire length of the bus. If routing constraints require routing of these signals with a transition to a different layer, a minimum of one ground stitching via for every two signals should be placed within 100 mils of the signal transition vias.

Routing of the common clock signals should use 2:1 trace spacing to trace width. This implies a minimum of 8 mils spacing (i.e., 12-mil minimum pitch) for a 4-mil trace width for routing on internal layers. Practical cases of escape routing under the GMCH or processor package outline and vicinity may not allow the implementation of 2:1 trace spacing requirements. Although every attempt should be made

to maximize the signal spacing in these areas, it is allowable to have 1:1 trace spacing underneath the GMCH and the processor package outlines and up to 200 – 300 mils outside the package outline.

Table 13 summarizes the list of common clock and key routing. RESET# (CPURST# of GMCH) is also a common clock signal but requires a special treatment for the case where an ITP700FLEX debug port is used. See Section 5.6 for further details.

Table 13. FSB Common Clock Signal Internal Layer Routing Guidelines

Signal Names		Transmission Line Type	Total Trace Length		Nominal Impedance (Ω)	Spacing & Width
CPU	GMCH		Min (mils)	Max (inches)		
ADS#	ADS#	Strip-line	997	6.5	55 ± 15%	2:1
BNR#	BNR#	Strip-line	1298	6.5	55 ± 15%	2:1
BPRI#	BPRI#	Strip-line	1215	6.5	55 ± 15%	2:1
BR0#	BR0#	Strip-line	1411	6.5	55 ± 15%	2:1
DBSY#	DBSY#	Strip-line	1159	6.5	55 ± 15%	2:1
DEFER#	DEFER#	Strip-line	1291	6.5	55 ± 15%	2:1
DPWR#	DPWR#	Strip-line	1188	6.5	55 ± 15%	2:1
DRDY#	DRDY#	Strip-line	1336	6.5	55 ± 15%	2:1
HIT#	HIT#	Strip-line	1303	6.5	55 ± 15%	2:1
HITM#	HITM#	Strip-line	1203	6.5	55 ± 15%	2:1
LOCK#	HLOCK#	Strip-line	1198	6.5	55 ± 15%	2:1
RS0#	RS0#	Strip-line	1315	6.5	55 ± 15%	2:1
RS1#	RS1#	Strip-line	1193	6.5	55 ± 15%	2:1
RS2#	RS2#	Strip-line	1247	6.5	55 ± 15%	2:1
TRDY#	HTRDY#	Strip-line	1312	6.5	55 ± 15%	2:1
RESET#[1]	CPURST#	Strip-line	1101	6.5	55 ± 15%	2:1

NOTE: For topologies where an ITP700FLEX debug port is implemented, see Section 5.6 for RESET# (CPURST#) implementation details.

5.3.1. Processor Common Clock Signal Package Length Compensation

Trace length matching for the common clock signals is not required. However, **package compensation** for the common clock signals is required for the minimum board trace. Please refer to Table 14 and the example below for more details. Package length compensation should not be confused with length matching. Length matching refers to constraints on the min and max length bounds of a signal group based on clock length, whereas package length compensation refers to the process of compensating for package length variance across a signal group.

All common clock signals are required to meet the minimum pad-to-pad requirement of **2.212** inches, based on ADS# (as this signal has the longest package lengths). This implies a minimum pin-to-pin motherboard trace length of **997 mils**. Additional motherboard trace will be added to some of the shorter

common clock nets on the system board in order to meet the same minimum requirement for trace lengths from the **die-pad** of the processor to the **associated die-pad** of the chipset.

For example:

ADS# = 997 mils board trace + 454 CPU PKG + 761 GMCH PKG = 2212 pad-to-pad length

BR0# = X mils board trace + 336 CPU PKG + 465 GMCH PKG = 2212 pad-to-pad length

Therefore: X = BR0# board trace = 2212 - 336 - 465 = 1411 pin to pin length.

Figure 20. Common Clock Topology

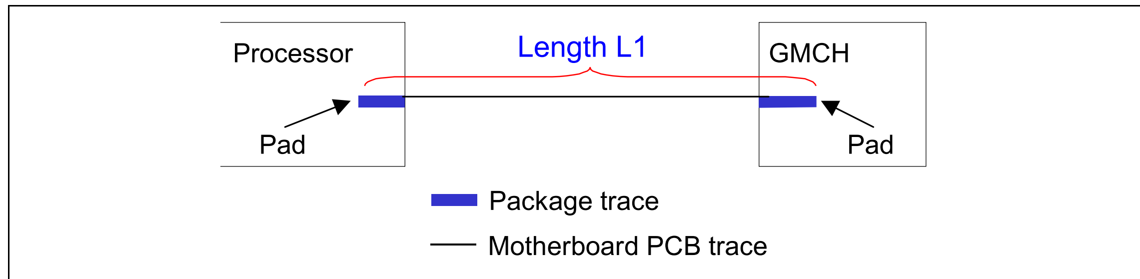


Table 14. Processor and GMCH FSB Common Clock Signal Package Lengths and Minimum Board Trace Lengths

Signal Names		Package Length		Total Pad-to-Pad Min. Length Requirements L1 (mils)	Min. Board Trace Length (mils)
CPU	GMCH	Intel Celeron M processor	GMCH		
ADS#	ADS#	454	761	2212	997
BNR#	BNR#	506	408	2212	1298
BPRI#	BPRI#	424	573	2212	1215
BR0#	BR0#	336	465	2212	1411
DBSY#	DBSY#	445	608	2212	1159
DEFER#	DEFER#	349	572	2212	1291
DPWR#	DPWR#	506	518	2212	1188
DRDY#	DRDY#	529	347	2212	1336
HIT#	HIT#	420	489	2212	1303
HITM#	HITM#	368	641	2212	1203
LOCK#	HLOCK#	499	515	2212	1198
RS0#	RS0#	576	321	2212	1315
RS1#	RS1#	524	495	2212	1193
RS2#	RS2#	451	514	2212	1247
TRDY#	HTRDY#	389	511	2212	1312
RESET#	CPURST#	455	656	2212	1101

5.4. Source Synchronous Signals General Routing Guidelines

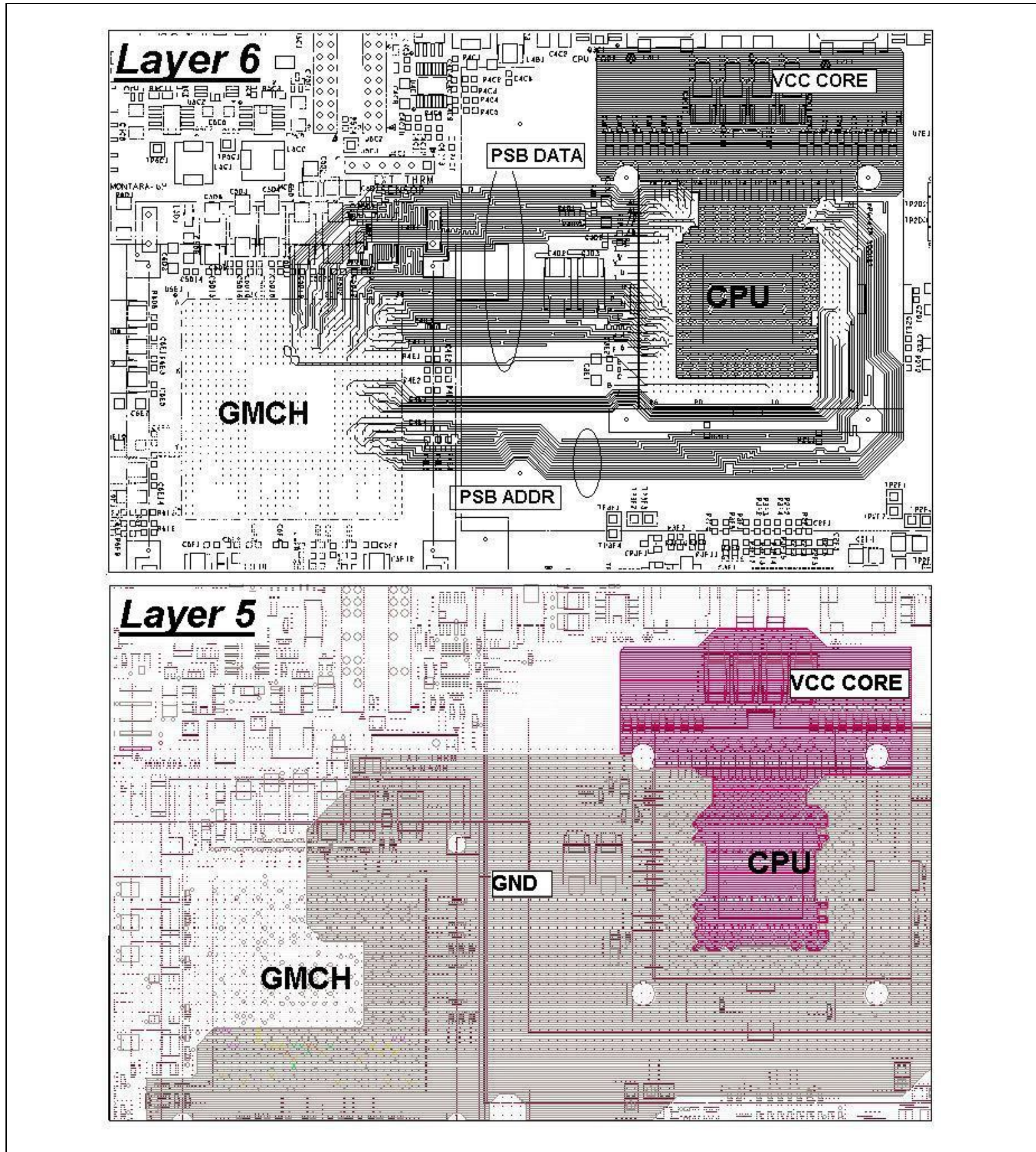
All source synchronous signals use an AGTL+ bus driver technology with on-die GTL termination resistors connected in a point-to-point, Zo = 55 Ω controlled impedance topology between the processor and the GMCH. No external termination is needed on these signals. Source synchronous FSB address signals operate at a double pumped rate of 200 MHz while the source synchronous FSB data signals operate at a quad pumped rate of 400 MHz. High-speed operation of the source synchronous signals requires careful attention to their routing considerations. The following guidelines should be strictly adhered to, to guarantee robust high frequency operation of these signals.

Source synchronous data and address signals and their associated strobes are partitioned into groups of signals. Flight time skew minimization within the same group of source synchronous signals is a key parameter that allows their high frequency (400 MHz) operation. All the source synchronous signals that belong to **the same group** should be routed on **the same internal layer** for the entire length of the bus. It is OK to split different groups of source synchronous signals between different motherboard layers as long as all the signals that belong to that group are kept on the same layer. Grouping of FSB source synchronous signals is summarized in Table 15 and Table 17. This practice results in a significant reduction of the flight time skew since the dielectric thickness, line width, and velocity of the signals will be uniform across a single layer of the stack-up.

The source synchronous signals should be routed as a strip-line on an internal layer with complete reference to ground planes both above and below the signal layer. Routing with references to split planes or power planes other than ground is **not** recommended. For the recommended stack-up example as shown in Figure 5, source synchronous FSB signals are routed on Layer 3 and Layer 6. Layer 2 and Layer 7 are solid grounds across the entire motherboard. However, this is not sufficient since significant coupling exists between signal layer, Layer 3 and power plane Layer 2 as well as signal layer, Layer 6 and power plane Layer 5. To guarantee complete ground referencing, Layer 4 and Layer 5 are converted to ground plane floods in the areas where the source synchronous FSB signals are routed. In addition all the ground plane areas are stitched with ground vias in the vicinity of the processor and the GMCH package outlines with the vias of the ground pins of the processor and the GMCH pin-map.

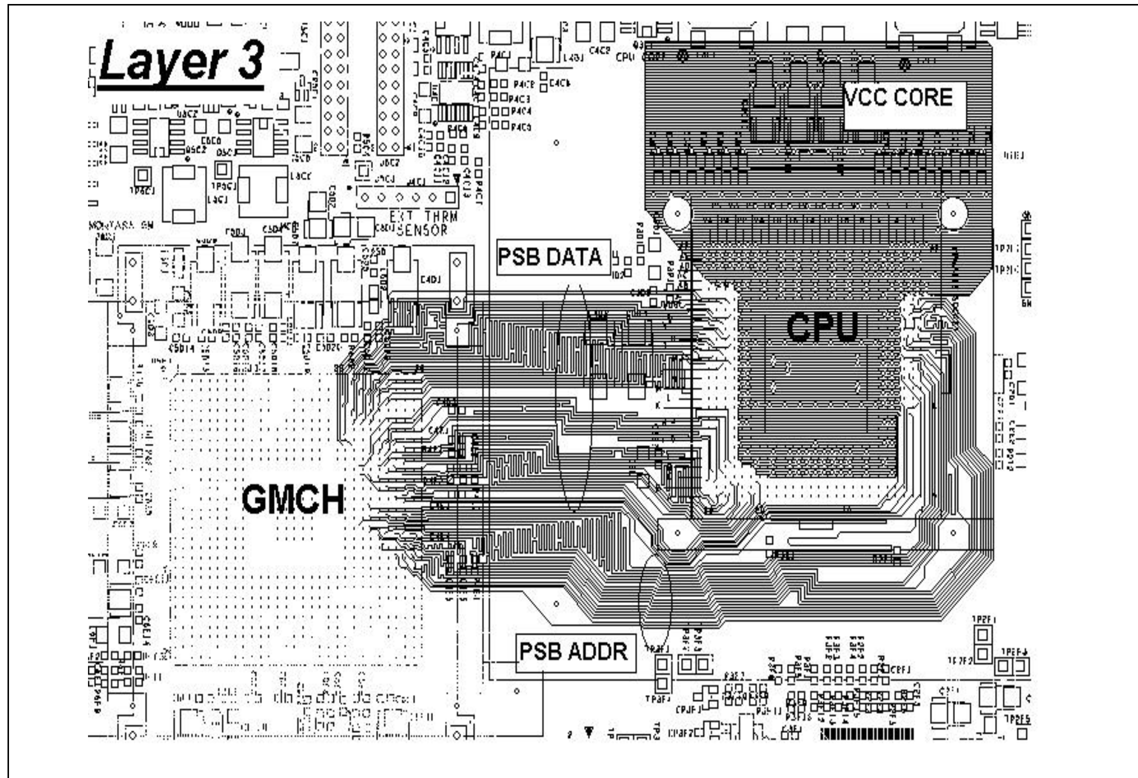
Figure 21 illustrates a motherboard layout of the recommended stack-up of the FSB source synchronous DATA and ADDRESS signals referencing ground planes on both Layer 7 and Layer 5. Note that in the socket cavity of the processor, Layer 5 and Layer 6 is used for VCC core power delivery. However, outside the socket cavity Layer 6 signals are routed on top of a solid Layer 7 ground plane and also Layer 5 is converted to a ground flood under the shadow of the FSB signals routing between the processor and the GMCH. Stitching of all the GND planes is provided by the ground vias in the pin-map of the processor and the GMCH.

Figure 21. Layer 6 FSB Source Synchronous Signals GND Referencing to Layer 5



In a similar way, Figure 22 illustrates a recommended layout and stack-up example of how another group of FSB source synchronous DATA and ADDRESS signals can reference ground planes on both Layer 2 and Layer 4. Note that in the socket cavity of the processor, Layer 3 is used for VCC core power delivery to reduce the I*R drop. However, outside of the socket cavity Layer 3 signals are routed below a solid Layer 2 ground plane and also Layer 4 is converted to a ground flood under the shadow of the FSB signals routing between the processor and the GMCH.

Figure 22. Layer 3 FSB Source Synchronous Signals



5.4.1. Source Synchronous Signal Length Matching Constraints

The routing guidelines presented in the following subsections define the recommended routing topologies, trace width and spacing geometries, and absolute minimum and maximum routed lengths for each signal group, which are recommended to achieve optimal SI and timing. In addition to the absolute length limits provided in the individual guideline tables, more restrictive length matching requirements called length-matching constraints. These additional requirements further restrict the minimum to maximum length range of each signal group with respect to strobe, within the overall boundaries defined in the guideline tables, as required to guarantee adequate timing margins. The amount of minimum to maximum length variance allowed for each group around the strobe reference length varies from signal group to signal group depending on the amount of timing variation, which can be tolerated.

5.4.2. Package Length Compensation

The Intel Celeron M processor package length **does not need** to be accounted for in the motherboard routing since the processor has the source synchronous signals and the strobes length matched within the group inside the package routing. However trace length matching of the **GMCH** package length **does need** to be accounted for in the motherboard routing since the package does not have the source synchronous signals and the strobes length matched within the group inside the package routing. See Table 19 for the processor and the GMCH package lengths. Skew minimization requires GMCH die-pad to processor pin (pad-to-pin) trace length matching of the FSB source synchronous signals that belong to the same group including the strobe signals of that group.

Package length compensation should not be confused with length matching. Length matching refers to constraints on the min and max length bounds of a signal group based on clock length, whereas package length compensation refers to the process of compensating for package length variance across a signal group. There is some overlap in that both affect the target length of an individual signal. Intel recommends that the initial route be completed based on the length matching formulas in conjunction with nominal package lengths and that package length compensation be performed as secondary operation.

5.4.3. Source Synchronous – Data Group

Robust operation of the 400-MHz, source synchronous data signals require tight skew control. For this reason, these signals are split into matched groups as outlined in Table 15. All the signals within the same group should be kept on the same layer of motherboard routing and should be routed to the same pad-to-pin length within ±100 mils of the associated strobes. Only the Intel Celeron M Processor has the package trace equalization for signals within each data and address group. The GMCH does not have the package trace equalization for signals within each data and address group. See Table 19 for the package lengths. Please refer to Section 4.9.3.1 for trace length and package compensation requirements. The two complementary strobe signals associated with each group should be length matched (pad-to-pin) to each other within ± 25 mils and tuned to the average length of the data signals (pad-to-pin) of their associated group. This will optimize setup/hold time margin.

Current simulation results provide routing guidelines using 3:1 spacing for the FSB source synchronous data and strobe signals. This implies a minimum of 12-mil spacing (i.e. 16-mil minimum pitch) for a 4-mil trace width. Practical cases of escape routing under the GMCH or the processor package outline and vicinity may not even allow the implementation of 2:1 trace spacing requirements. Although every attempt should be made to maximize the signal spacing in these areas, it is allowable to have 1:1 trace spacing underneath the GMCH and the processor package outlines and up to 200 – 300 mils outside the package outline. The benefits of additional spacing include increased signal quality and voltage margining. The trace routing and length matching requirements are as follows in Section 5.4.1 through Section 5.4.5. Note that if trace impedance can be controlled to within ± 10%, the FSB data signals can then be routed using 2:1 spacing guidelines. The strobes, however, must still be routed with 3:1 spacing.

Table 15. Processor FSB Data Source Synchronous Signal Trace Length Mismatch Mapping

Data Group	DINV signal for associated Data Group	Signal Matching	Data Strobes associated With the Group	Strobe Matching	Notes
D[15:0]#	DINV0#	± 100 mils	DSTBP0#, DSTBN0#	± 25 mils	1,2
D[31:16]#	DINV1#	± 100 mils	DSTBP1#, DSTBN1#	± 25 mils	1,2
D[47:32]#	DINV2#	± 100 mils	DSTBP2#, DSTBN2#	± 25 mils	1,2
D[63:48]#	DINV3#	± 100 mils	DSTBP3#, DSTBN3#	± 25 mils	1,2

NOTES:

1. Strobes of the same group should be trace length matched to each other within ±25 mil and to the average length of their associated Data signal group.
2. Note that all length matching formulas are based on GMCH die-pad to processor pin total length per byte lane. Package length table are provided for all signals in order to facilitate this pad to pin matching.

Table 16 lists the source synchronous data signal general routing requirements. Due to the 400-MHz, high frequency operation of the data signals should be limited to a pin-to-pin trace length minimum of 0.50 inches and maximum of 5.5 inches.

Table 16. FSB Source Synchronous Data Signal Routing Guidelines

Signal Names				Transmission Line Type	Total Trace Length		Nominal Impedance (Ω)	Spacing & Width (mils)
Data Group #1	Data Group #2	Data Group #3	Data Group #4		Min (inches)	Max (inches)		
D[15:0]#	D[31:16]#	D[47:32]#	D[63:48]#	Strip-line	0.5	5.5	55 ± 15%	3:1
DINV0#	DINV1#	DINV2#	DINV3#	Strip-line	0.5	5.5	55 ±15%	3:1
DSTBN[0]#	DSTBN[1]#	DSTBN[2]#	DSTBN[3]#	Strip-line	0.5	5.5	55 ± 15%	3:1
DSTBP[0]#	DSTBP[1]#	DSTBP[2]#	DSTBP[3]#	Strip-line	0.5	5.5	55 ±15%	3:1

NOTES:

1. These data signals can be routed with 2:1 spacing if using 55 ± 10% nominal impedance. However, spacing to associated strobes must still be kept at 3:1.

5.4.4. Source Synchronous – Address Group

Source synchronous address signals operate at 200 MHz. Thus, their routing requirements are very similar to the data signals. Refer to Sections 5.4 and 5.4.1 for further details. Table 17 details the partition of the address signals into matched length groups. Due to the lower operating frequency of the address signals, pad-to-pin length matching is relaxed to ± 200 mils. Each group is associated with only one strobe signal. To maximize setup/hold time margin, the address strobes should be trace length matched to the average trace length of the address signals of their associated group. In addition, each address signal should be trace length matched within ± 200 mils of its associated strobe signal.

Table 17. Processor FSB Address Source Synchronous Signal Trace Length Mismatch Mapping

CPU Signal Name	Signal Matching	Strobe Associated With the Group	Strobe to Assoc. Address Signal Matching	Notes
REQ[4:0]#, A[16:3]#	± 200 mils	ADSTB0#	± 200 mils	1,2,3
A[31:17]#	± 200 mils	ADSTB1#	± 200 mils	1,2,3

NOTES:

1. ADSTB[1:0]# should be should be trace length matched to the average length of their associated Address signals group
2. Each Address signal should be trace length matched to its associated Address Strobe within ± 200 mils.
3. Note that all length matching formulas are based on GMCH die-pad to processor pin total length per signal group. Package length table are provided for all signals in order to facilitate this pad to pin matching.

Table 18 lists the source synchronous address signals general routing requirements. They should be routed to a pin-to-pin length minimum of 0.50 inches and maximum of 6.5 inches. Due to the 200-MHz, high frequency operation of the address signals, the routing guidelines listed in Table 18 allows for 2:1 spacing for the address signals given a 55 Ω ± 15% characteristic trace impedance except for address strobe signals. But if space permits, 3:1 spacing is strongly advised for these signals.

Table 18. Processor FSB Source Synchronous Address Signal Routing Guidelines

Signal Names		Transmission Line Type	Total Trace Length		Nominal Impedance (Ω)	Width & Spacing (mils)
Address Group #1	Address Group #2		Min (inches)	Max (inches)		
A[16:3]#	A[31:17]#	Strip-line	0.50	6.5	55 ± 15%	4 & 8
REQ[4:0]#		Strip-line	0.50	6.5	55 ± 15%	4 & 8
ADSTB#[0]	ADSTB#[1]	Strip-line	0.50	6.5	55 ± 15%	4 & 12

5.4.5. Intel Celeron M Processor and Intel 852GM Chipset GMCH FSB Signal Package Lengths

Table 19 lists the preliminary package trace lengths of the Intel Celeron M Processor and the Intel 852GM chipset GMCH for the source synchronous data and address signals. The processor FSB package signals within the same group are **routed** to the same package trace length, but the GMCH package signals within the same group are **not routed** to the same package trace length. As a result of this package length compensation is required for GMCH. Refer to Section 5.4.1 for length matching constrains and Section 5.4.2 package length compensation for further details. The processor package traces are routed as micro-strip lines with a nominal characteristic impedance of 55 Ω ± 15%.

Table 19. Intel Celeron M Processor and GMCH Source Synchronous FSB Signal Package Lengths

Signal Group	CPU Signal Name	CPU Package Length (mils)	GMCH Signal Name	GMCH Package Length (mils)	Signal Group	CPU Signal Name	CPU Package Length (mils)	GMCH Signal Name	GMCH Package Length (mils)
Data Group 1	D15#	721	HD15#	554	Data Group 2	D31#	564	HD31#	914
	D14#	721	HD14#	393		D30#	564	HD30#	464
	D13#	721	HD13#	494		D29#	564	HD29#	691
	D12#	721	HD12#	620		D28#	564	HD28#	768
	D11#	721	HD11#	319		D27#	564	HD27#	453
	D10#	721	HD10#	504		D26#	564	HD26#	815
	D9#	721	HD9#	438		D25#	564	HD25#	837
	D8#	721	HD8#	458		D24#	564	HD24#	493
	D7#	721	HD7#	329		D23#	564	HD23#	766
	D6#	721	HD6#	518		D22#	564	HD22#	731
	D5#	721	HD5#	693		D21#	564	HD21#	522
	D4#	721	HD4#	600		D20#	564	HD20#	714
	D3#	721	HD3#	387		D19#	564	HD19#	412
	D2#	721	HD2#	438		D18#	564	HD18#	834
	D1#	721	HD1#	620		D17#	564	HD17#	634
	D0#	721	HD0#	329		D16#	564	HD16#	593
	DINV[0]#	721	DINV[0]#	514		DINV[1]#	564	DINV[1]#	628
	DSTBP[0]#	721	HDSTBP[0]#	662		DSTBP[1]#	564	HDSTBP[1]#	736
	DSTBN[0]#	721	HDSTBN[0]#	763		DSTBN[1]#	564	HDSTBN[1]#	787
Data Group 3	D47#	661	HD47#	654	Data Group 4	D63#	758	HD63#	579
	D46#	661	HD46#	647		D62#	758	HD62#	509
	D45#	661	HD45#	460		D61#	758	HD61#	431
	D44#	661	HD44#	563		D60#	758	HD60#	522
	D43#	661	HD43#	726		D59#	758	HD59#	490
	D42#	661	HD42#	828		D58#	758	HD58#	347
	D41#	661	HD41#	608		D57#	758	HD57#	649
	D40#	661	HD40#	358		D56#	758	HD56#	372
	D39#	661	HD39#	655		D55#	758	HD55#	541
	D38#	661	HD38#	619		D54#	758	HD54#	598
	D37#	661	HD37#	747		D53#	758	HD53#	469
	D36#	661	HD36#	633		D52#	758	HD52#	575
	D35#	661	HD35#	675		D51#	758	HD51#	326
	D34#	661	HD34#	683		D50#	758	HD50#	549
	D33#	661	HD33#	501		D49#	758	HD49#	511
	D32#	661	HD32#	664		D48#	758	HD48#	372
	DINV[2]#	661	DINV[2]#	784		DINV[3]#	758	DINV[3]#	431
	DSTBP[2]#	661	HDSTBP[2]#	502		DSTBP[3]#	758	HDSTBP[3]#	463

Signal Group	CPU Signal Name	CPU Package Length (mils)	GMCH Signal Name	GMCH Package Length (mils)	Signal Group	CPU Signal Name	CPU Package Length (mils)	GMCH Signal Name	GMCH Package Length (mils)
	DSTBN[2]#	661	HDSTBN[2]#	538		DSTBN[3]#	758	H DSTBN[3]#	505
Addr Group 1	REQ4#	616	HREQ4#	276	**Addr Group 2**	A31#	773	HA31#	617
	REQ3#	616	HREQ3#	383		A30#	773	HA30#	484
	REQ2#	616	HREQ2#	247		A29#	773	HA29#	558
	REQ1#	616	HREQ1#	378		A28#	773	HA28#	579
	REQ0#	616	HREQ0#	569		A27#	773	HA27#	631
	A16#	616	HA16#	491		A26#	773	HA26#	556
	A15#	616	HA15#	375		A25#	773	HA25#	535
	A14#	616	HA14#	562		A24#	773	HA24#	353
	A13#	616	HA13#	501		A23#	773	HA23#	382
	A12#	616	HA12#	522		A22#	773	HA22#	545
	A11#	616	HA11#	566		A21#	773	HA21#	429
	A10#	616	HA10#	560		A20#	773	HA20#	414
	A9#	616	HA9#	327		A19#	773	HA19#	284
	A8#	616	HA8#	333		A18#	773	HA18#	389
	A7#	616	HA7#	274		A17#	773	HA17#	457
	A6#	616	HA6#	523		ADSTB[1]#	773	HADSTB[1]#	504
	A5#	616	HA5#	551	**Host Clocks**	BCLK0	447	BCLK	1138
	A4#	616	HA4#	352		BCLK1	447	BCLK#	1145
	A3#	616	HA3#	468					
	ADSTB[0]#	616	HADSTB[0]#	419					

5.5. Asynchronous Signals

The following sections describe the topologies and layout recommendations for the Asynchronous Open Drain and CMOS signals found on the platform. All Open Drain signals listed in the following sections must be pulled-up to VCCP (1.05 V). If any of these Open Drain signals are pulled-up to a voltage higher than VCCP, the reliability and power consumption of the processor may be affected. Therefore, it is very important to follow the recommended pull-up voltage for these signals. All signals must meet the AC and DC specifications as documented in the *Intel® Celeron® M Processor Datasheet*.

Table 20. Asynchronous AGTL+ Nets

Signal Names	Description	Topology #	CPU IO Type	Output	Output Buffer Type	Input	Input Power Well
A20M#	Address 20 mask	2C	I	ICH4-M	CMOS	CPU	N/A
DPSLP#	Deep sleep	2B	I	ICH4-M	CMOS	CPU	N/A
FERR#	Floating point error	1B	O	CPU	AGTL+	ICH4-M	Main I/O (3.3 V)
IERR#	Internal error	1A	O	CPU	AGTL+	System Receiver	Vcc_Receiver
IGNNE#	Ignore next numeric error	2C	I	ICH4-M	CMOS	CPU	N/A
INIT#	Processor initialize	3	I	ICH4-M	CMOS	CPU, FWH	N/A, 3.3V
LINT0/INTR	Local interrupts	2C	I	ICH4-M	CMOS	CPU	N/A
LINT1/NMI	Local interrupts	2C	I	ICH4-M	CMOS	CPU	N/A
PROCHOT#	Thermal sensor	1C	O	CPU	AGTL+	System Receiver	Vcc_Receiver
PWRGOOD	System power good	2A	I	ICH4-M	OD CMOS	CPU	N/A
SLP#	Sleep	2C	I	ICH4-M	CMOS	CPU	N/A
SMI#	System management interrupt	2C	I	ICH4-M	CMOS	CPU	N/A
STPCLK#	Processor stop clock	2C	I	ICH4-M	CMOS	CPU	N/A
THRMTRIP#	Thermal sensor	1B	O	CPU	AGTL+	System Receiver	Vcc_Receiver

5.5.1. Topology 1A: Open Drain (OD) Signals Driven by the Processor – IERR#

The Topology 1A OD signal IERR# should adhere to the following routing and layout recommendations. Table 21 lists the recommended routing requirements for the IERR# signal of the processor. The routing guidelines allow the signal to be routed as either micro-strip or strip-lines using 55 Ω ± 15% characteristic trace impedance. Series resistor R1 is a dampening resistor for reducing overshoot/ undershoot reflections on the transmission line. The pull-up voltage for termination resistor Rtt is VCCP (1.05 V). Due to the dependencies on system design implementation, IERR# can be implemented in a number of ways to meet design goals. IERR# can be routed as a test point or to any optional system receiver.

Figure 23. Routing Illustration for Topology 1A

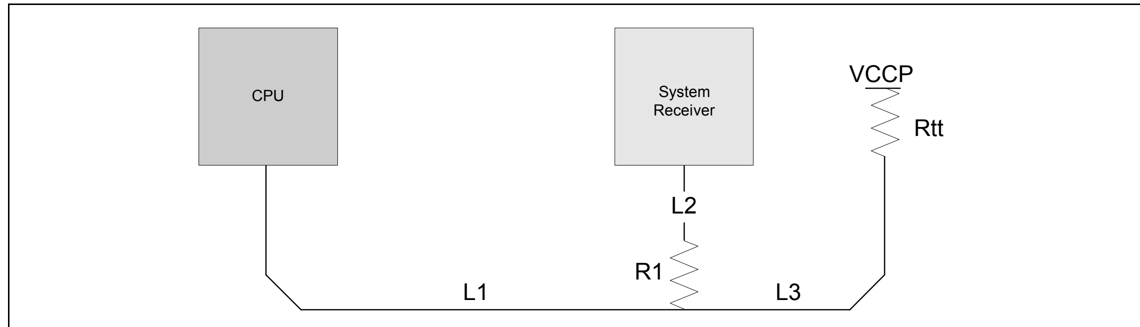


Table 21. Layout Recommendations for Topology 1A

L1	L2	L3	R1	Rtt	Transmission Line Type
0.5” – 12.0”	0” – 3.0”	0” – 3.0”	56 Ω ± 5%	56 Ω ± 5%	Micro-strip
0.5” – 12.0”	0” – 3.0”	0” – 3.0”	56 Ω ± 5%	56 Ω ± 5%	Strip-line

5.5.2. Topology 1B: Open Drain (OD) Signals Driven by the Processor – FERR# and THERMTRIP#

The Topology 1B OD signals FERR# and THERMTRIP# should adhere to the following routing and layout recommendations. Table 22 lists the recommended routing requirements for the FERR# and THERMTRIP# signals of the processor. The routing guidelines allow the signals to be routed as either micro-strips or strip-lines using 55 Ω ± 15% characteristic trace impedance. Series resistor R1 is a dampening resistor for reducing overshoot/undershoot reflections on the transmission line. The pull-up voltage for termination resistor Rtt is VCCP (1.05 V).

Intel recommends that the FERR# signal of the processor be routed to the FERR# signal of the ICH4-M. THERMTRIP# can be implemented in a number of ways to meet design goals. It can be routed to the ICH4-M or any optional system receiver. It is recommended that the THERMTRIP# signal of the processor be routed to the THRMTRIP# signal of the ICH4-M. The ICH4-M’s THRMTRIP# signal is a new signal to the I/O controller hub architecture that allows the ICH4-M to quickly put the whole system into a S5 state whenever the catastrophic thermal trip point has been reached.

If either FERR# or THERMTRIP# is routed to an optional system receiver rather than the ICH4-M and the interface voltage of the optional system receiver does not support a 1.05-V voltage swing, then a voltage translation circuit must be used. If the recommended voltage translation circuit described in Section 5.5.8 is used, the driver isolation resistor shown in Figure 30, Rs, should replace the series dampening resistor R1 in Topology 1B. Thus, it is important to note that R1 will no longer be required in such a topology.

Figure 24. Routing Illustration for Topology 1B

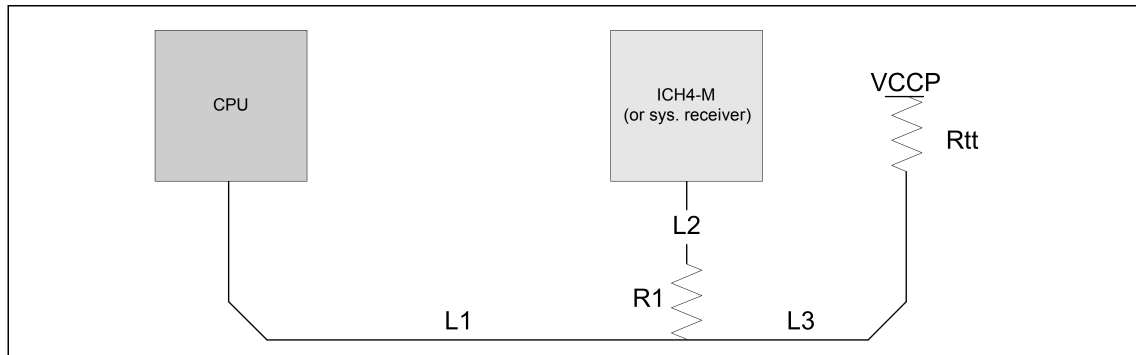


Table 22. Layout Recommendations for Topology 1B

L1	L2	L3	R1	Rtt	Transmission Line Type
0.5" – 12.0"	0" – 3.0"	0" – 3.0"	56 Ω ± 5%	56 Ω ± 5%	Micro-strip
0.5" – 12.0"	0" – 3.0"	0" – 3.0"	56 Ω ± 5%	56 Ω ± 5%	Strip-line

5.5.3. Topology 1C: Open Drain (OD) Signals Driven by the Processor – PROCHOT#

The Topology 1C OD signal PROCHOT# should adhere to the following routing and layout recommendations. Table 23 lists the recommended routing requirements for the PROCHOT# signal of the processor. The routing guidelines allow the signal to be routed as either a micro-strip or strip-line using 55 Ω ± 15% characteristic trace impedance. Figure 25 shows the recommended implementation for providing voltage translation between the processor's PROCHOT# signal and a system receiver that utilizes a 3.3-V interface voltage (shown as V_IO_RCVR). The receiver at the output of the voltage translation circuit can be any system receiver that can function properly with the PROCHOT# signal given the nature and usage model of this pin. PROCHOT# is capable of toggling hundreds of times per second to signal a hot temperature condition.

Series resistor Rs is a component of the voltage translation logic and serves as a driver isolation resistor. Rs is shown separated by distance L3 from the first bipolar junction transistor (BJT), Q1, to emphasize the placement of Rs with respect to Q1. The placement of Rs a distance L3 before the Q1 BJT is a specific implementation of the generalized voltage translator circuit shown in Figure 30. Rs should be placed at the beginning of the T-split from the PROCHOT# signal. The pull-up voltage for termination resistor Rtt is VCCP (1.05 V).

Figure 25. Routing Illustration for Topology 1C

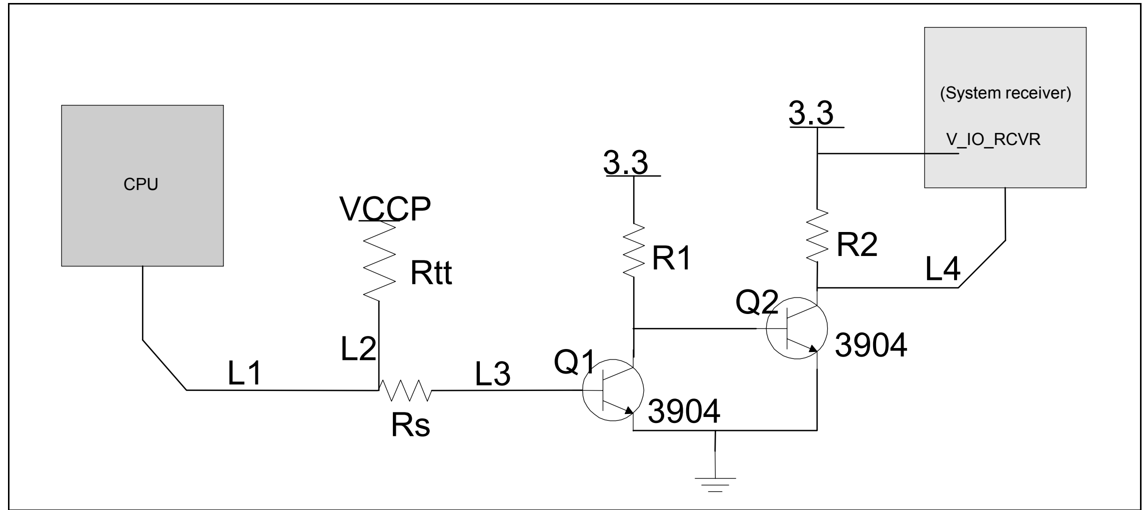


Table 23. Layout Recommendations for Topology 1C

L1	L2	L3	L4	Rs	R1	R2-	Rtt	Transmission Line Type
0.5" – 12.0"	0" – 3.0"	0" – 3.0"	0.5" – 12.0"	330 Ω ± 5%	1.3 kΩ ± 5%	330 Ω ± 5%	56 Ω ± 5%	Micro-strip
0.5" – 12.0"	0" – 3.0"	0" – 3.0"	0.5" – 12.0"	330 Ω ± 5%	1.3 kΩ ± 5%	330 Ω ± 5%	56 Ω ± 5%	Strip-line

5.5.4. Topology 2A: Open Drain (OD) Signals Driven by ICH4-M – PWRGOOD

The Topology 2A OD signal PWRGOOD, which is driven by the ICH4-M (CMOS signal input to processor) should adhere to the following routing and layout recommendations. Table 24 lists the recommended routing requirements for the PWRGOOD signal of the processor. The routing guidelines allow the signal to be routed as either micro-strip or strip-lines using 55 Ω ± 15% characteristic trace impedance. The pull-up voltage for termination resistor Rtt is VCCP (1.05 V).

Note: The ICH4-M's CPUPWRGD signal should be routed point-to-point to the processor's PWRGOOD signal. The routing from the processor's PWRGOOD pin should fork out to both to the termination resistor, Rtt, and the ICH4-M. Segments L1 and L2 from Table 24 should not T-split from a trace from the pin.

Figure 26. Routing Illustration for Topology 2A

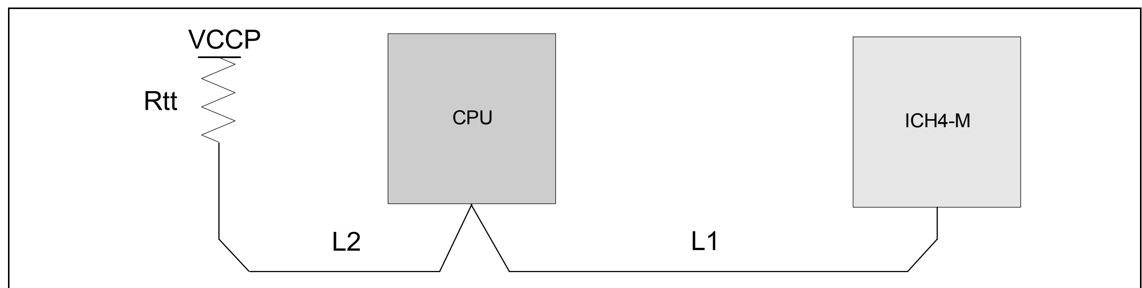


Table 24. Layout Recommendations for Topology 2A

L1	L2	Rtt	Transmission Line Type
0.5" – 12.0"	0" – 3.0"	330 Ω ± 5%	Micro-strip
0.5" – 12.0"	0" – 3.0"	330 Ω ±5%	Strip-line

5.5.5. Topology 2B: CMOS Signals Driven by ICH4-M – DPSLP#

The Topology 2B CMOS DPSLP# signal, which is driven by the ICH4-M (CMOS signal input to the processor), should adhere to the routing and layout recommendations illustrated in Figure 27. As listed in Figure 27, the L1 and L2 segments of the DPSLP# signal topology can be routed as either micro-strip or strip-lines using 55 Ω ± 15% characteristic trace impedance.

Note: The ICH4-M's DPSLP# signal should be routed point-to-point with the daisy chain topology shown. The routing of DPSLP# at the CPU should fork out to both the ICH4-M and the GMCH. Segments L1 and L2 from Figure 27 should not T-split from a trace from the pin.

Figure 27. Routing Illustration for Topology 2B

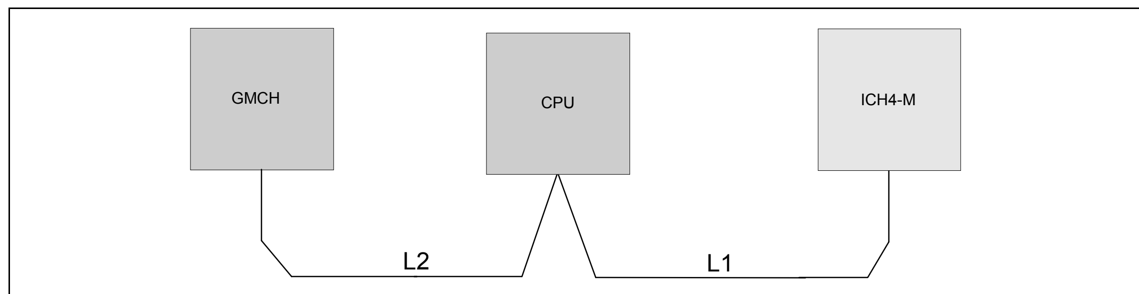


Table 25. Layout Recommendations for Topology 2B

L1	L2	Transmission Line Type
0.5" – 12.0"	0.5" – 6.5"	Micro-strip
0.5" – 12.0"	0.5" – 6.5"	Strip-line

5.5.6. Topology 2C: CMOS Signals Driven by ICH4-M – LINT0/INTR, LINT1/NMI, A20M#, IGNNE#, SLP#, SMI#, and STPCLK#

The Topology 2C CMOS LINT0/INTR, LINT1/NMI, A20M#, IGNNE#, SLP#, SMI#, and STPCLK# signals should implement a point-to-point connection between the ICH4-M and the processor. The routing guidelines allow both signals to be routed as either micro-strip or strip-lines using 55 Ω ± 15% characteristic trace impedance. No additional motherboard components are necessary for this topology.

Figure 28. Routing Illustration for Topology 2C

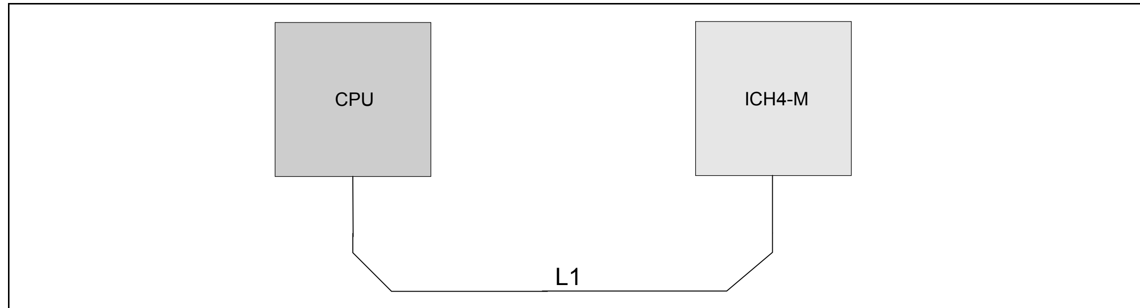


Table 26. Layout Recommendations for Topology 2C

L1	Transmission Line Type
0.5" – 12.0"	Micro-strip
0.5" – 12.0"	Strip-line

5.5.7. Topology 3: CMOS Signals Driven by ICH4-M to CPU and FWH – INIT#

The signal INIT# should adhere to the following routing and layout recommendations. Table 27 lists the recommended routing requirements for the INIT# signal of the ICH4-M. The routing guidelines allow both signals to be routed as either micro-strip or strip-lines using 55 Ω ± 15% characteristic trace impedance. Figure 29 shows the recommended implementation for providing voltage translation between the ICH4-M's INIT# voltage signaling level and any firmware hub (FWH) that utilizes a 3.3-V interface voltage (shown as a supply V_IO_FWH). See Section 5.5.8 for more details on the voltage translator circuit.

Series resistor Rs is a component of the voltage translator logic circuit and serves as a driver isolation resistor. Rs is shown separated by distance L3 from the first bipolar junction transistor (BJT), Q1, to emphasize the placement of Rs with respect to Q1. The placement of Rs a distance of L3 before the Q1 BJT is a specific implementation of the generalized voltage translator circuit shown in Figure 30. The routing recommendations of transmission line L3 in Figure 29 is listed in Table 27 and Rs should be placed at the beginning of the T-split of the trace from the ICH4-M's INIT# pin.

Figure 29. Routing Illustration for Topology 3

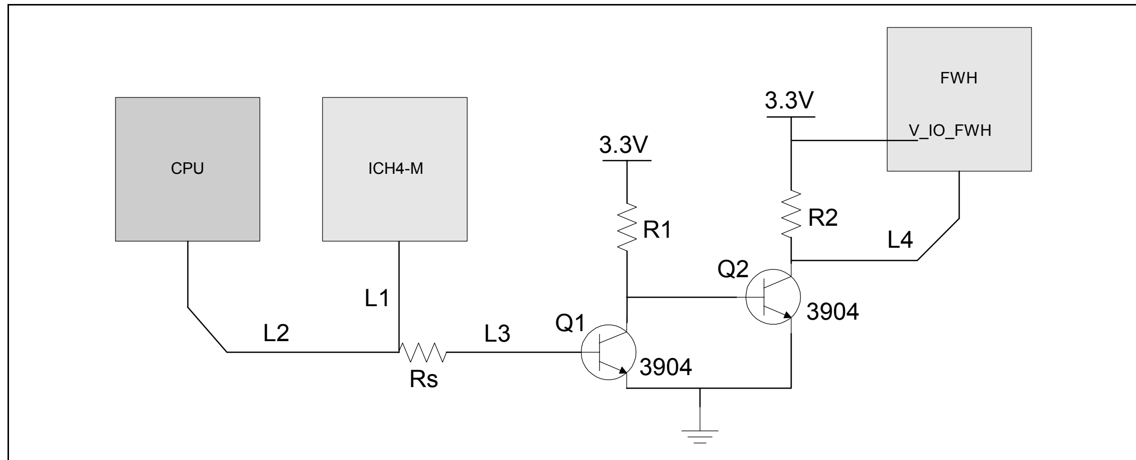


Table 27. Layout Recommendations for Topology 3

L1 + L2	L3	L4	Rs	R1	R2	Transmission Line Type
0.5" – 12.0"	0" – 3.0"	0.5" – 6.0"	330 Ω ± 5%	1.3 kΩ ± 5%	330 Ω ± 5%	Micro-strip
0.5" – 12.0"	0" – 3.0"	0.5" – 6.0"	330 Ω ± 5%	1.3 kΩ ± 5%	330 Ω ± 5%	Strip-line

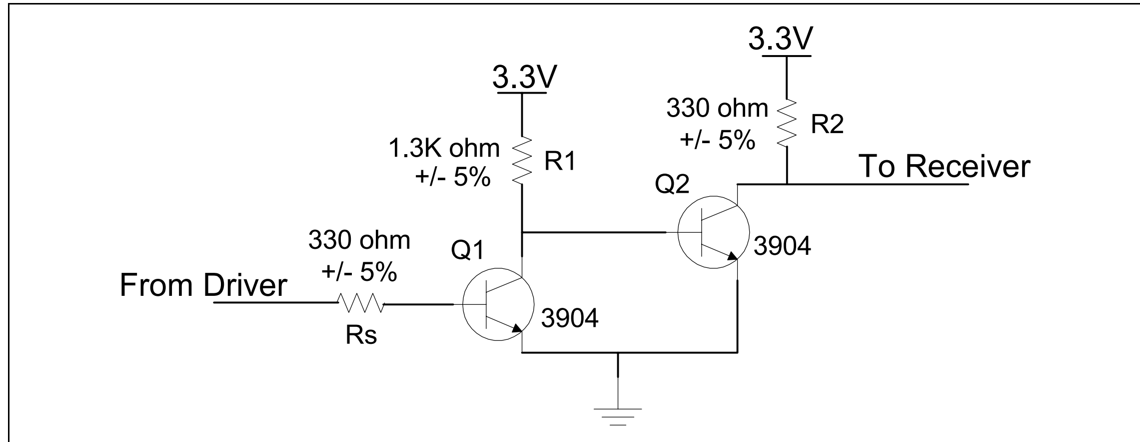
5.5.8. Voltage Translation Logic

A voltage translation circuit or component is required on any signals where the voltage signaling level between two components connected by a transmission line may cause unpredictable signal quality. The recommended voltage translation circuit for the platform is shown in Figure 30. The driver isolation resistor, Rs, is place at the beginning of a transmission line that connects to the first bipolar junction transistor, Q1. Though the circuit shown in Figure 30 was developed to work with signals that require translation from a 1.05 V to a 3.3 V voltage level, the same topology and component values, in general, can be adapted for use with other signals as well, provided the interface voltage of the receiver is also 3.3 V. Any component value changes or component placement requirements for other signals must be simulated in order to guarantee good signal quality and acceptable performance from the circuit.

In addition to providing voltage translation between driver and receiver devices, the recommended circuit also provides filtering for noise and electrical glitches. A larger first-stage collector resistor, R1, can be used on the collector of Q1, however, it will result in a slower response time to the output falling edge. In the case of the INIT# signal, resistors with value*s as close as possible to those listed in Figure 30 should be used without exception.

With the low 1.05-V signaling level of the Intel Celeron M Processor Front Side Bus, the voltage translation circuit provides ample isolation of any transients or signal reflections at the input of transistor Q1 from reaching the output of transistor Q2. Based on simulation results, the voltage translation circuit can effectively isolate transients as large as 200 mV and that last as long as 60 ns.

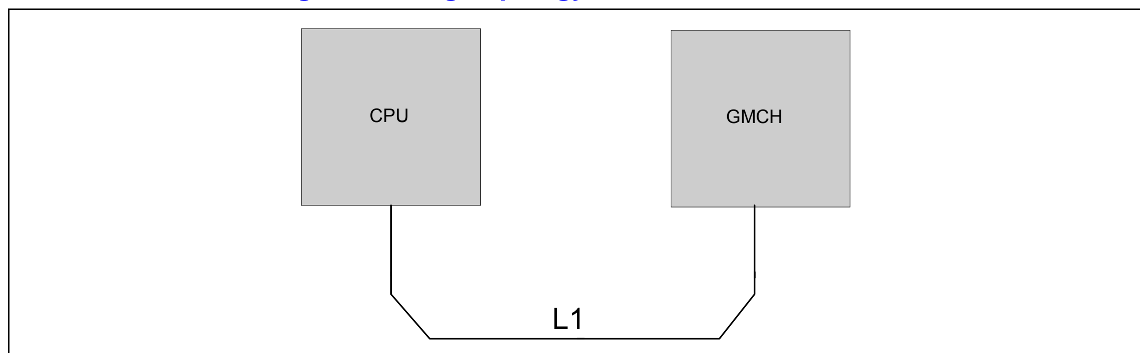
Figure 30. Voltage Translation Circuit



5.6. Processor RESET# Signal

The RESET# signal is a common clock signal driven by the GMCH CPURST# pin. In a production system where no ITP700FLEX debug port is implemented, a simple point-to-point connection between the CPURST# pin of the GMCH and processor RESET# pin is recommended (see Figure 31). On-die termination of the AGTL+ buffers on both the processor and the GMCH provide proper signal quality for this connection. This is the same case as for the other common clock signals listed Section 5.3. Length L1 of this interconnect should be limited to minimum of 1 inch and maximum of 6.5 inches.

Figure 31. Processor RESET# Signal Routing Topology with NO ITP700FLEX Connector



For a system that implements an ITP700FLEX debug port a more elaborate topology is required in order to guarantee proper signal quality at both the processor signal pad and the ITP700FLEX input receiver. In this case the topology illustrated in Figure 32 should be implemented. The CPURST# signal from the GMCH should fork out (do not route one trace from GMCH pin and then T-split) towards the processor's RESET# pin as well as towards the Rtt and Rs resistive termination network placed next to the ITP700FLEX debug port connector. Rtt (54.9 Ω + 1%) pulls-up to the VCCP voltage and is placed at the end of the L2 line that is limited to a 12-inch maximum length. Rs (22.6 Ω +/- 1%) should be placed right next to Rtt to minimize the routing between them in the vicinity of the ITP700FLEX connector to limit the L3 length to less than 0.5 inches. ITP700FLEX operation requires the matching of L2 + L3 - L1 length to the length of the BPM[4:0]# signals length within ± 250 mils. See Table 28 for routing length summary and termination resistor values.

Currently 1% tolerance resistors are recommended for Rs and Rtt. The use of 5% tolerant resistors for these resistors and whether it could provide adequate signal quality performance is under investigation.

Figure 32. Processor RESET# Signal Routing Topology with ITP700FLEX Connector

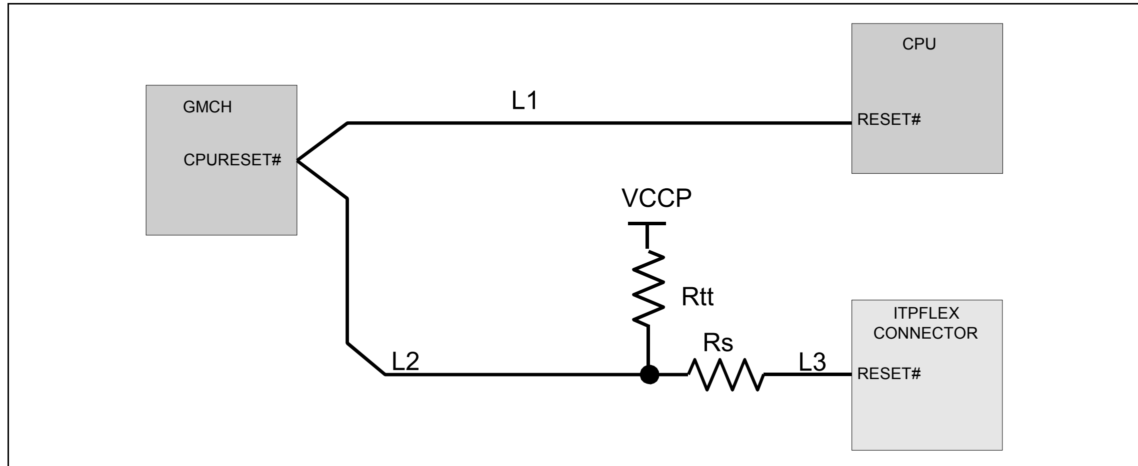


Table 28. Processor RESET# Signal Routing Guidelines with ITP700FLEX Connector

L1	L2 + L3	L3	Rs	Rtt
1.0" – 6.0"	6.0" max	0.5" max	Rs = 22.6 Ω ± 1%	Rtt = 220 Ω ± 5%

5.6.1. Processor RESET# Routing Example

Figure 33 illustrates a board routing example for the RESET# signal with an ITP700FLEX debug port implemented. It illustrates how the CPURST# pin of GMCH forks out into two branches on Layer 6 of the motherboard. One branch is routed directly to the processor RESET# pin amongst the rest of the common clock signals. Another branch routes below the address signals and vias down to the secondary side that route to the Rs and Rtt resistors. These resistors are placed in the vicinity of the ITP700FLEX debug port.

Note: The placement of Rs and Rtt next to each other is to minimize the routing between Rs and Rtt as well as the minimal routing between Rs and the ITP700FLEX connector. Also, since a transition between Layer 6 and the secondary side occurs, a GND stitching via is added to guarantee continuous ground reference of the secondary side routing of the RESET# signal to ITP700FLEX connector.

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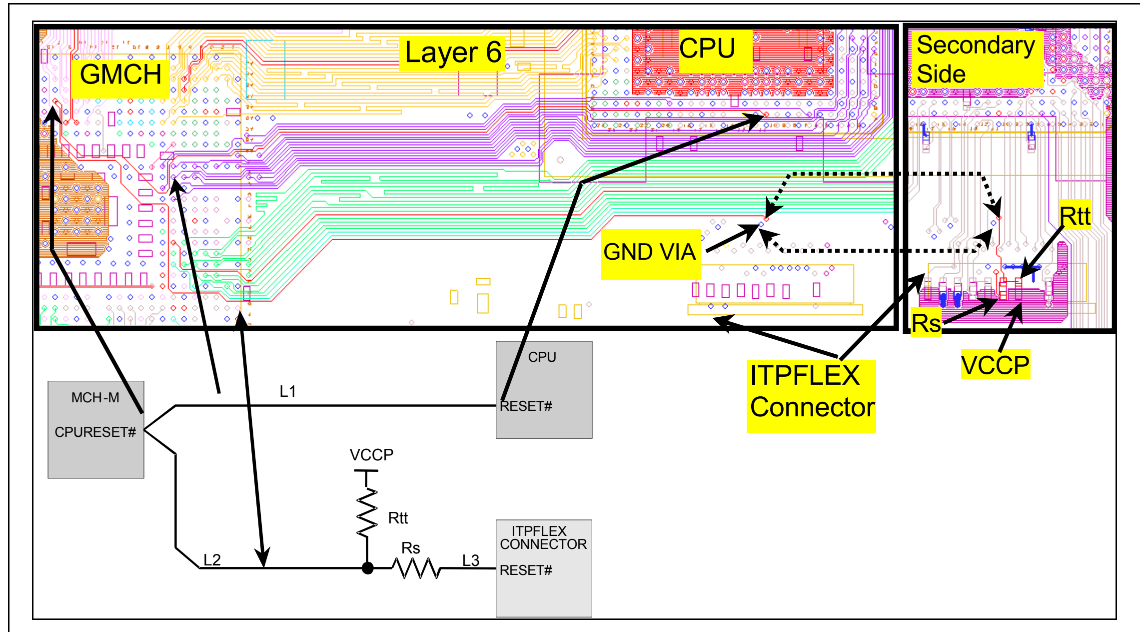
Figure 33. Processor RESET# Signal Routing Example with ITP700FLEX Debug Port

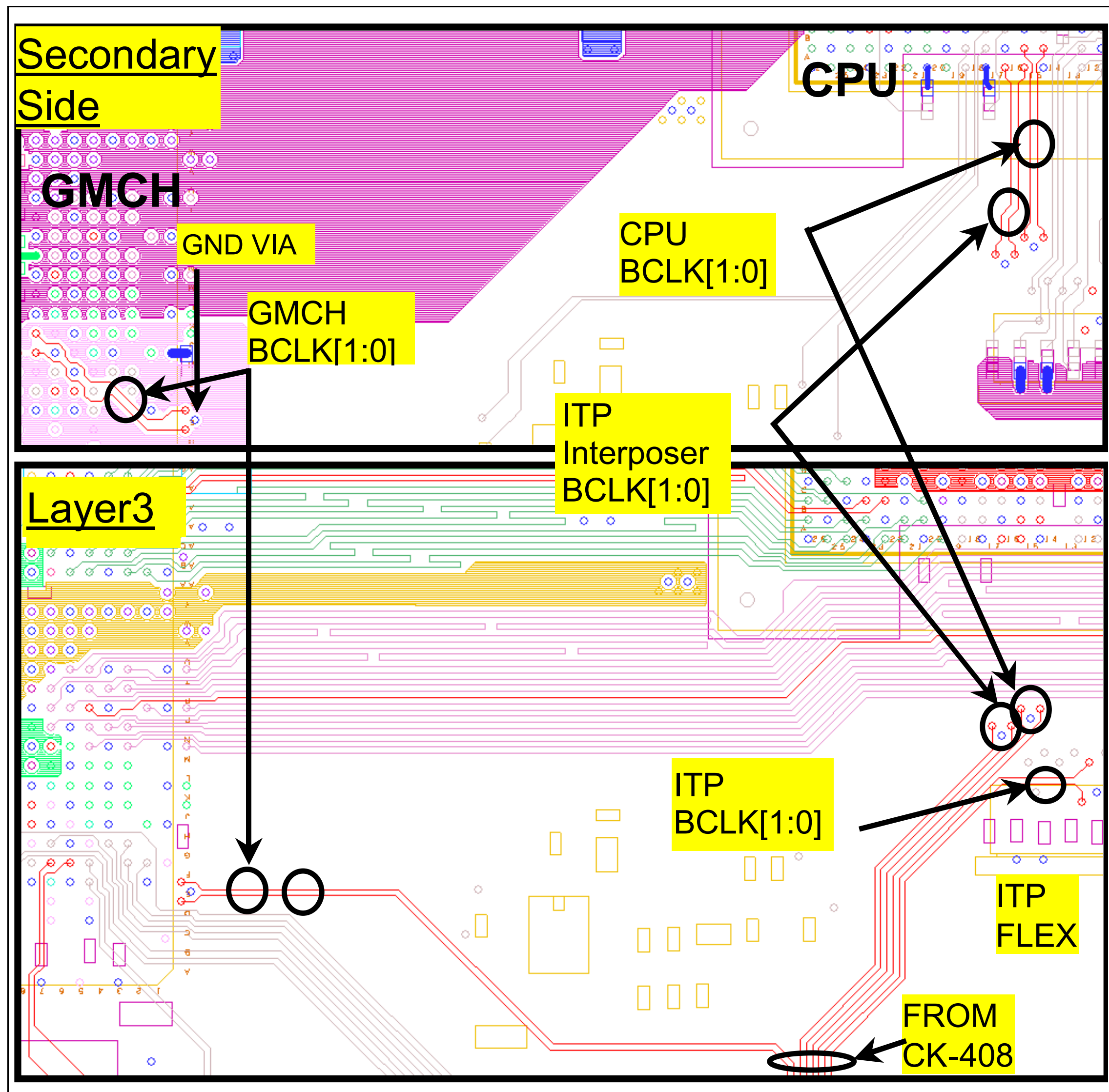


5.7. Processor and GMCH Host Clock Signals

Figure 34 illustrates processor and GMCH host clock signal routing. Both the processor and the GMCH's BCLK[1:0] signals are initially routed from the CK-408 clock generator on Layer 3.In the recommended routing example (Figure 34) secondary side layer routing of BCLK[1:0] is 507 mils long. To meet length-matching requirements between the processor and GMCH's BCLK[1:0] signals, a similar transition from Layer 3 to the secondary side layer is done next to the GMCH package outline. Routing of the GMCH's BCLK[1:0] signals on the secondary side is also trace tuned to 507 mils. BCLK[1:0] layer transition vias are accompanied by GND stitching vias. For similar reasons, routing for the ITP interposer's BCLK[1:0] signals also transition from Layer 3 to the secondary side layer and have 507-mil long traces on this layer. Throughout the routing length on Layer 3, BCLK[1:0] signals should reference a solid GND plane on Layer 2 and Layer 4 as shown in Figure 22.

If a system supports either the on-board ITP700FLEX connector or ITP interposer only, then differential host clock routing to either the ITP700FLEX connector or CPU socket (but not both) is required.

Figure 34. Processor and GMCH Host Clock Layout Routing Example



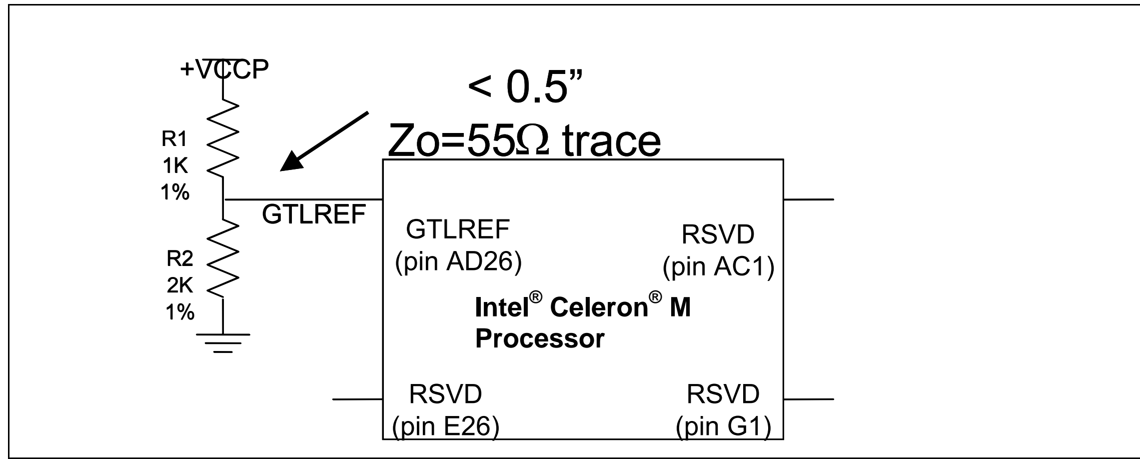
5.8. Processor GTLREF Layout and Routing Recommendations

There is one AGTL+ reference voltage pin on the Intel Celeron M Processor, GTLREF, which is used to set the reference voltage level for the AGTL+ signals (GTLREF). The reference voltage must be supplied to the GTLREF pin. The voltage level that needs to be supplied to GTLREF must be equal to 2/3 * VCCP ± 2%. The GMCH also requires a reference voltage (MCH_GTLREF) to be supplied to its HVREF[4:0] pins. The GTLREF voltage divider for both the processor and GMCH cannot be shared. Thus, both the processor and GMCH must have their own locally generated GTLREF networks. Figure 35 shows the recommended topology for generating GTLREF for the processor using a R1 = 1 kΩ ± 1% and R2 = 2 kΩ ± 1% resistive divider.

Since the input buffer trip point is set by the 2/3*VCCP on GTLREF and to allow tracking of VCCP voltage fluctuations, **no** decoupling should be placed on the GTLREF pin. The node between R1 and R2 (GTLREF) should be connected to the GTLREF pin of the processor with Zo = 55 Ω trace shorter than 0.5 inches. Space any other switching signals away from GTLREF with a minimum separation of 25 mils. Do not allow signal lines to use the GTLREF routing as part of their return path (i.e. do not allow the GTLREF routing to create splits or discontinuities in the reference planes of the FSB signals).

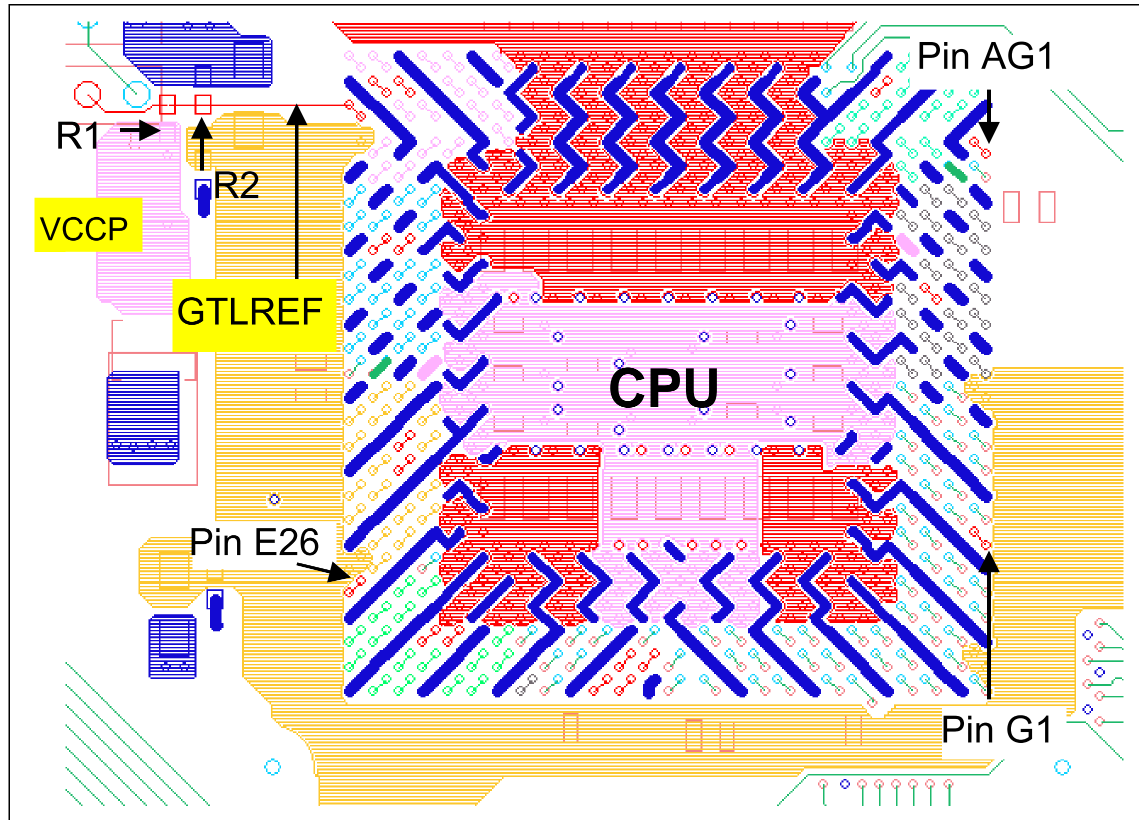
RSVD signal pins E26, G1, and AC1 are to be left unconnected on Intel® Celeron® M processor based systems.

Figure 35. Processor GTLREF Voltage Divider Network



A recommended layout of GTLREF for the processor is shown in Figure 36. To avoid interaction with FSB routing and power delivery, GTLREF's R1 and R2 components are placed next to each other on the primary side of the motherboard and connected with a Zo = 55 Ω to the GTLREF pin on the processor. The BGA ball lands on the primary side for the RSVD signal pins E26, G1, and AC1 are shown for illustrative purposes and are not routed.

Figure 36. Processor GTLREF Motherboard Layout



5.9. AGTL+ I/O Buffer Compensation

The Intel Celeron M Processor has 4 pins, COMP[3:0], and the GMCH has 2 pins, HRCOMP[1:0], that require compensation resistors to adjust the AGTL+ I/O buffer characteristics to specific board and operating environment characteristics. Also, the GMCH requires two special reference voltage generation circuits to pins HSWNG[1:0] for the same purpose described above. Refer to the *Intel® Celeron® M Processor Datasheet* and *Intel® 852GM Chipset GMCH datasheet* for details on resistive compensation.

5.9.1. Processor AGTL+ I/O Buffer Compensation

For the Intel Celeron M Processor, the COMP[2] and COMP[0] pins (see Figure 37) must each be pulled-down to ground with 27.4 Ω ± 1% resistors and should be connected to the processor with a Zo = 27.4 Ω trace that is less than 0.5 inches from the processor pins. The COMP[3] and COMP[1] pins (see Figure 38) must each be pulled-down to ground with 54.9 Ω ± 1% resistors and should be connected to the processor with a Zo = 55 Ω trace that is less than 0.5 inches from the processor pins. COMP[3:0] traces should be at least 25 mils (> 50 mils preferred) away from any other toggling signal.

Figure 37. Processor COMP[2] & COMP[0] Resistive Compensation

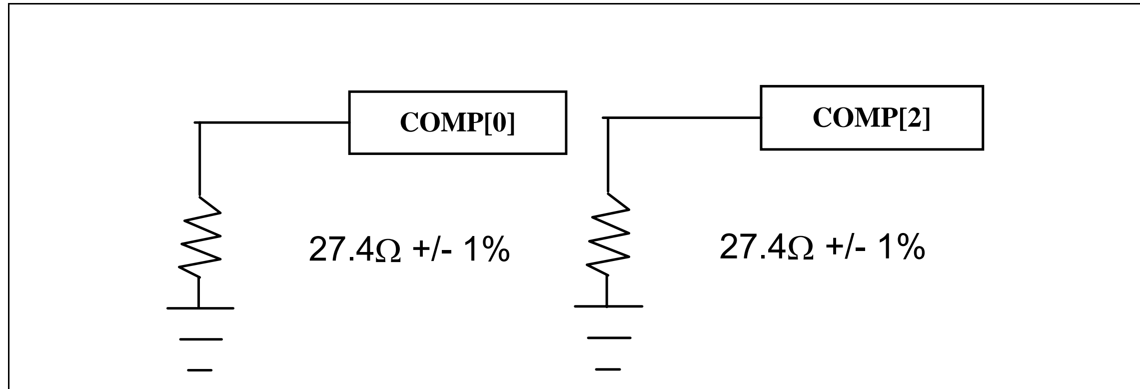
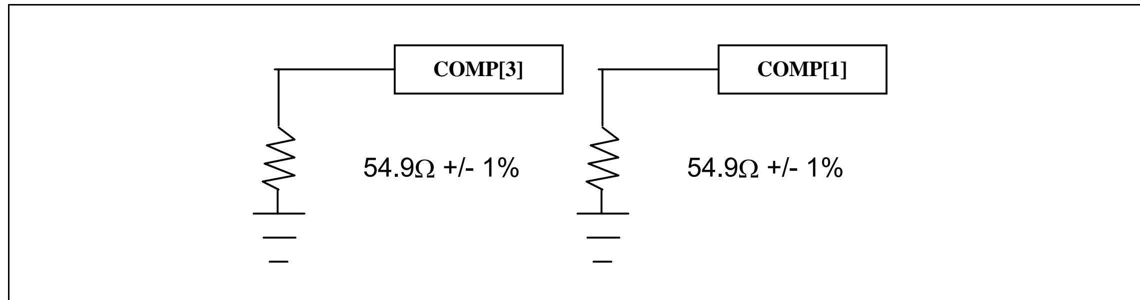


Figure 38. Processor COMP[3] & COMP[1] Resistive Compensation



The recommended layout of the processor COMP[3:0] resistors is illustrated in Figure 39. To avoid interaction with FSB routing on internal layers and VCCA power delivery on the primary side, Layer 1, COMP[1:0] resistors are placed on the secondary side. Ground connections to the COMP[1:0] resistors use a small ground flood on the secondary side layer and connect only with a single GND via to stitch the GND planes. The compact layout as shown in Figure 39 should be used to avoid excessive "perforation" of the V_{CCP} plane power delivery. Figure 39 illustrates how a 27.4 Ω resistor connects with an ~18-mil wide (Zo = 27.4 Ω) trace to COMP0. Necking down to 14 mils is allowed for a short length to pass in between the dog bones. The 54.9-Ω resistor connects with a regular 5-mil wide (Zo = 55 Ω) trace to COMP1. Placement of COMP[1:0] on the primary side is possible as well. An alternative placement implementation is shown in Figure 40.

To minimize motherboard space usage and produce a robust connection, the COMP[3:2] resistors are also placed on the secondary side (Figure 39, right side). A 27.4-Ω resistor connects with an 18-mil wide (Zo = 27.4 Ω) and 260-mil long trace to COMP2. Necking down to 14 mils is allowed for a short length to pass in between the dog bones. Notice that the COMP2 (Figure 39, left side) dog bone trace connection on the primary side is also widened to 14 mils to meet the Zo = 27.4-Ω characteristic impedance target. The right side of Figure 39 also illustrates how the 54.9 Ω ± 1% resistor connects with a regular 5-mil wide (Zo = 55Ω) and 100-mil long trace to COMP3. The ground connection of COMP[3:2] is done with a small flood plane on the secondary side that connects to the GND vias of pins AA1 and Y2 of the processor pin-map. This is done to avoid via interaction with the FSB routing on Layer 3 and Layer 6.

For COMP2 and COMP0, it is extremely important that 18-mil wide dog bone connections on the primary side and 18-mil wide traces on the secondary sides be used to connect the signals to compensation resistors on the secondary side. The use of 18-mil wide dog bones and traces is used to achieve the Zo = 27.4-Ω target to ensure proper operation of the FSB. See Figure 41 for more details.

Figure 39. Processor COMP[3:0] Resistor Layout

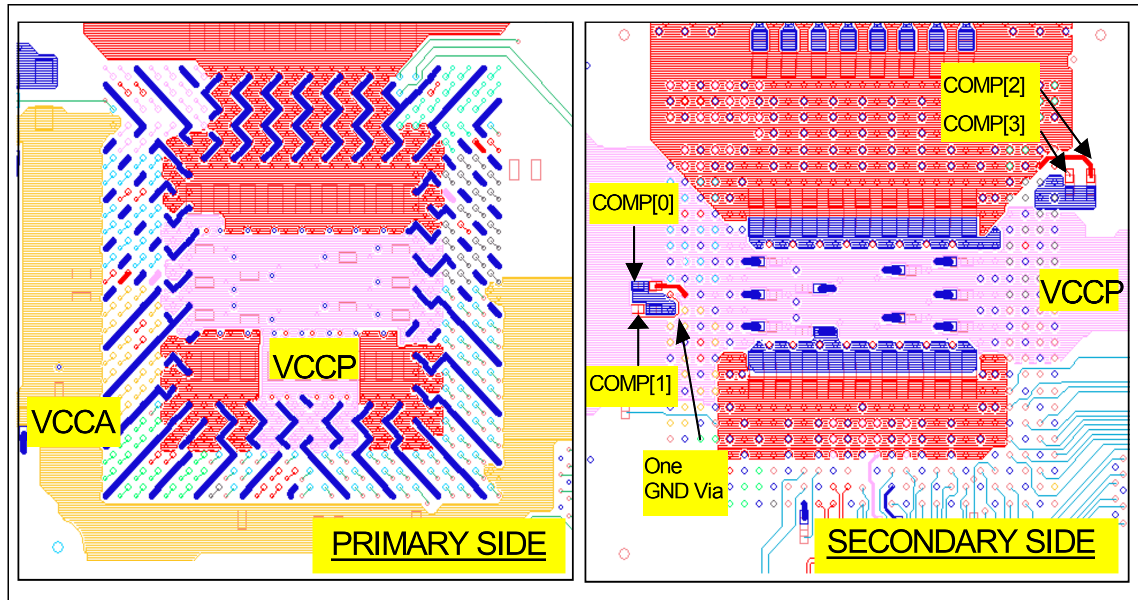


Figure 40. Processor COMP[1:0] Resistor Alternative Primary Side Layout

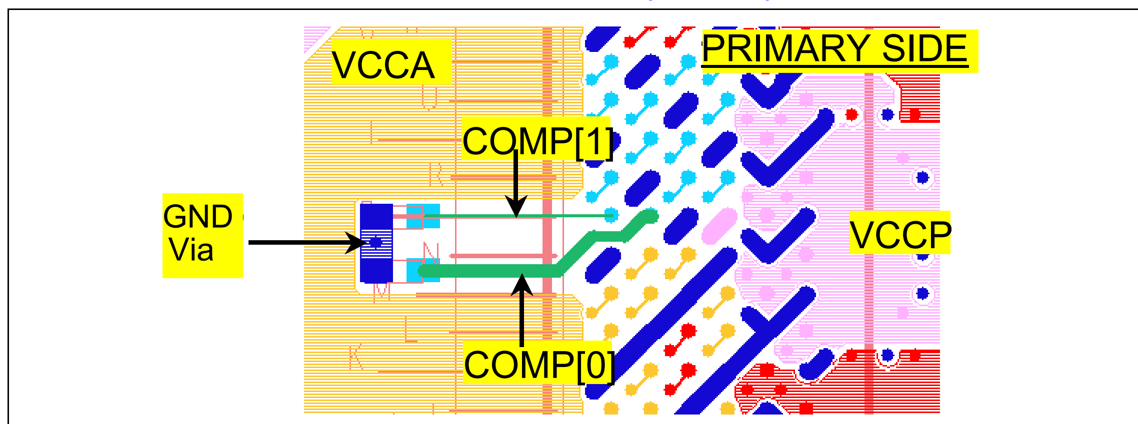
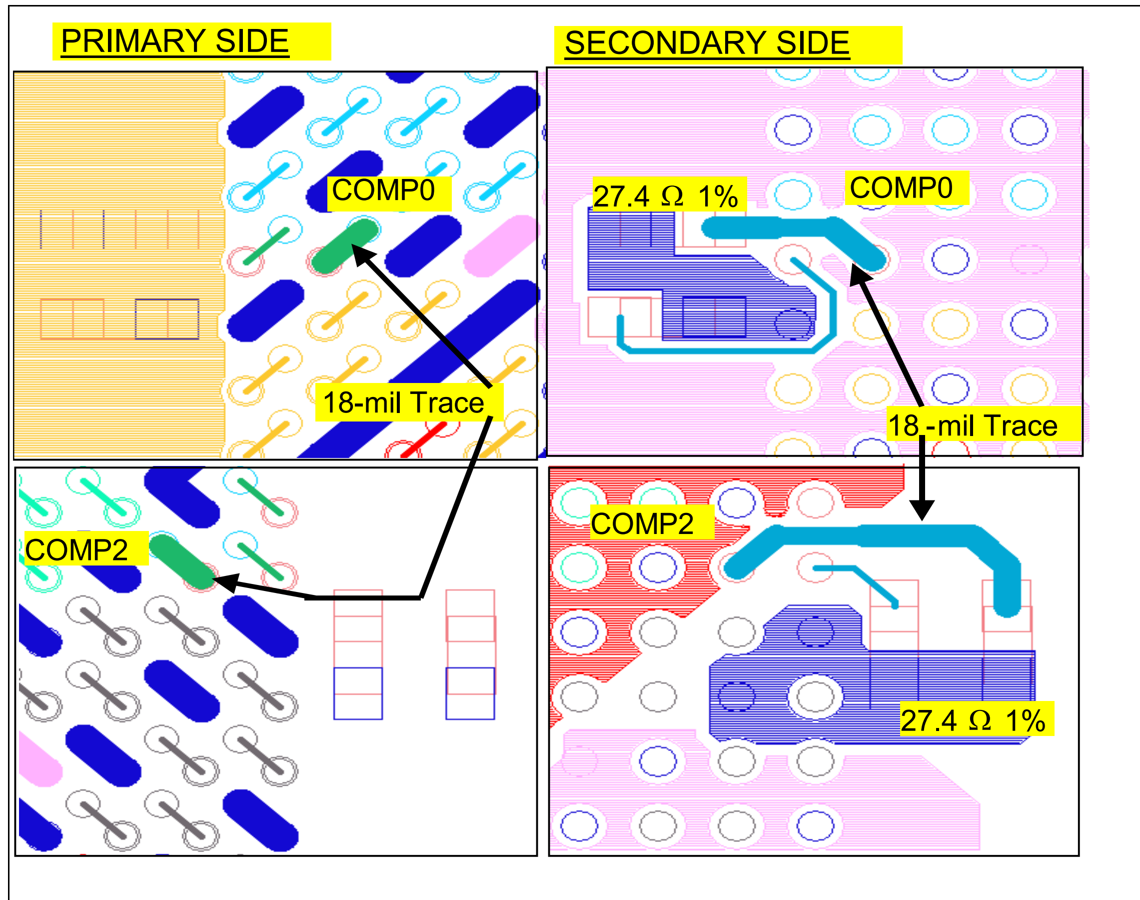


Figure 41. COMP2 & COMP0 27.4-Ω Traces



5.10. Intel Celeron M Processor Front Side Bus Strapping and Debug Port

The Intel Celeron M Processor and GMCH both have pins that require termination for proper component operation.

1. For the processor, a stuffing option should be provided for the TEST[3:1] pin to allow a 1 kΩ ± 5% pull-down to ground for testing purposes. For proper processor operation, the resistor should not be stuffed. Resistors for the stuffing option on these pins should be placed within 2.0 inches of the processor. For normal operation, these resistors should not be stuffed.
2. The processor's ITP signals, TDI, TMS, TRST, and TCK should assume default logic values even if the ITP debug port is not used. The TDO signal may be left open or no connect in this case. The table below summarizes the default strapping resistors for these signals. These resistors should be connected to the processor within 2.0 inches from their respective pins. It is important to note that Table 29 is applicable only when neither the onboard ITP nor ITP interposer are planned to be used. Intel does not recommend use of the ITP interposer debug port if there is a dependence only on the motherboard termination resistors. The signals below should be isolated from the motherboard via specific termination resistors on the ITP interposer itself per interposer debug port recommendations.

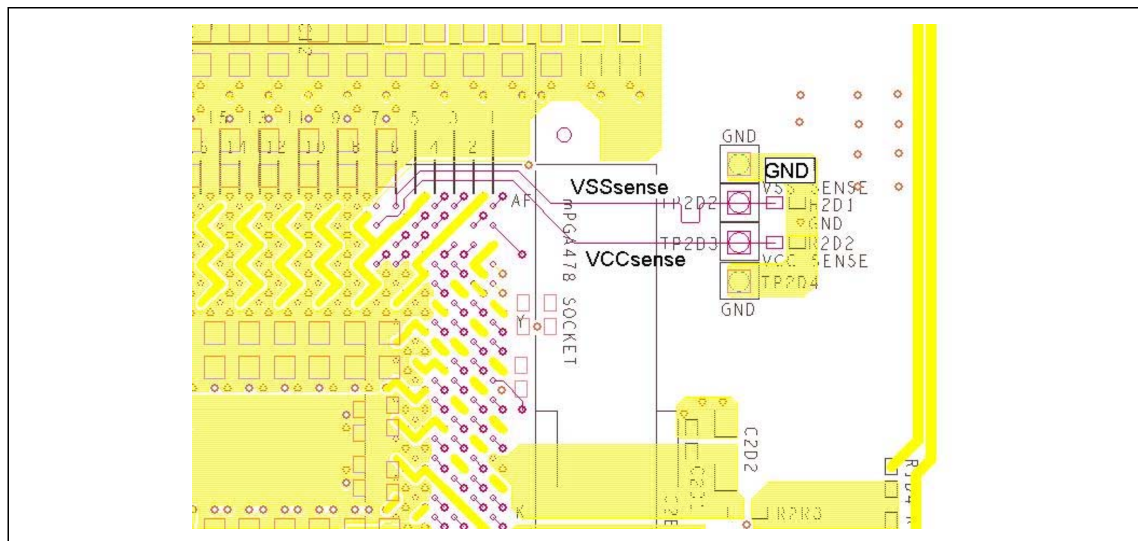
Table 29. ITP Signal Default Strapping When ITP Debug Port Not Used

Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 Ω ± 5%	VCCP	Within 2.0" of the CPU
TMS	39 Ω ± 5%	VCCP	Within 2.0" of the CPU
TRST#	680 Ω ± 5%	GND	Within 2.0" of the CPU
TCK	27 Ω ± 5%	GND	Within 2.0" of the CPU
TDO	Open	NC	N/A

5.11. Processor $V_{CCSENSE}$/$V_{SSSENSE}$ Design Recommendations

The VCCSENSE and VSSSENSE signals of the Intel Celeron M Processor provide isolated, low impedance connections to the processor's core power (VCC) and ground (VSS). These pins can be used to sense or measure power (VCC) or ground (VSS) near the silicon with little noise. To make them available for measurement purposes, it is recommended that VCCSENSE and VSSSENSE both be routed with a Zo = 55 Ω ± 15% trace of equal length. Use 3:1 spacing between the routing for the two signals and all other signals should be a minimum of 25 mils (preferably 50 mils) from VCCSENSE and VSSSENSE routing. Terminate each line with an optional (default is No Stuff) 54.9 Ω ± 1% resistor. Also, a ground via spaced 100 mils away from each of the test point vias for VCCSENSE and VSSSENSE should be added. A third ground via should also be placed in between them to allow for a differential probe ground. See Figure 42 for the recommended layout example.

Figure 42. $V_{CCSENSE}$/$V_{SSSENSE}$ Routing Example



6. Processor Power Delivery Requirements

Please contact your Intel Field Representative for more information on the electrical requirements for the DC-to-DC Voltage Regulator for the Mobile Pentium 4 Processor-M featuring Intel® SpeedStep® technology.

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7. System Memory Design Guidelines (DDR-SDRAM)

The Intel 852GM GMCH chipset Double Data Rate (DDR) SDRAM system memory interface consists of SSTL-2 compatible signals. These SSTL-2 compatible signals have been divided into several signal groups: Data, Control, Command, CPC, Clock, and Feedback signals. Table 30 summarizes the different signal grouping. Refer to the *Intel® 852GM GMCH Chipset Datasheet* for details on the signals listed.

Table 30. Intel 852GM GMCH Chipset DDR Signal Groups

Group	Signal Name	Description
Clocks	SCK[4,3,1,0]	DDR-SDRAM Differential Clocks - (2 per SO-DIMM)
	SCK#[4,3,1,0]	DDR-SDRAM Inverted Differential Clocks - (2 per SO-DIMM)
Data	SDQ[63:0]	Data Bus
	SDQS[7:0]	Data Strobes
	SDM[7:0]	Data Mask
Control	SCKE[3:0]	Clock Enable - (One per Device Row)
	SCS#[3:0]	Chip Select - (One per Device Row)
Command	SMA[12:6,3,0]	Memory Address Bus
	SBA[1:0]	Bank Select
	SRAS#	Row Address Select
	SCAS#	Column Address Select
	SWE#	Write Enable
CPC	SMA[5,4,2,1]	Command per Clock (SO-DIMM0)
	SMAB[5,4,2,1]	Command per Clock (SO-DIMM1)
Feedback	RCVENOUT#	Receive Enable Output (no external connection)
	RCVENIN#	Receive Enable Input (no external connection)

7.1. Length Matching and Length Formulas

The routing guidelines presented in the following subsections define the recommended routing topologies, trace width and spacing geometries, and absolute minimum and maximum routed lengths for each signal group, which are recommended to achieve optimal SI and timing. In addition to the absolute length limits provided in the individual guideline tables, more restrictive length matching formulas are also provided which further restrict the minimum to maximum length range of each signal group with respect to clock, within the overall boundaries defined in the guideline tables, as required to guarantee adequate timing margins. These secondary constraints are referred to as length matching constraints and the formulas used are referred to as length matching formulas.

All signal groups, except feedback signals, are length matched to the DDR clocks. The clocks on a given SO-DIMM are matched to within ± 25 mils of the target length. A different clock target length may be used for each SO-DIMM. The difference in clock target lengths between SO-DIMM0 and SO-DIMM1 should not exceed 1 inch. A simple summary of the length matching formulas for each signal group is provided in Table 31.

Table 31. Length Matching Formulas

Signal Group	Minimum Length	Maximum Length
Control to Clock	Clock –1.0”	Clock + 0.5”
Command to Clock	Clock – 1.0”	Clock + 2.0”
CPC to Clock	Clock – 1.0”	Clock + 0.5”
Strobe to Clock	Clock – 1.0”	Clock + 0.5”
Data to Strobe	Strobe – 25 mils	Strobe + 25 mils

NOTE: All length matching formulas are based on GMCH die-pad to SO-DIMM pin total length.

Package length tables are provided for all signals in order to facilitate this pad-to-pin matching. The clock lengths to SO-DIMM1 may be up to 1.0 inch longer than the clock lengths to SO-DIMM0. Length formulas should be applied to each SO-DIMM slot separately. The full geometry and routing guidelines along with the exact length matching formulas and associated diagrams are provided in the individual signal group guidelines sections.

7.2. Package Length Compensation

As mentioned in Section 7.1, all length matching is done GMCH die-pad to SO-DIMM pin. The reason for this is to compensate for the package length variation across each signal group. The GMCH does not equalize package lengths internally as some previous GMCH components have, and therefore, the Intel 852GM GMCH requires length matching.

Package length compensation should not be confused with length matching as discussed in the previous section. Length matching refers to constraints on the min and max length bounds of a signal group based on clock length, whereas package length compensation refers to the process of adjusting out package length variance across a signal group. There is of course some overlap in that both affect the target length of an individual signal. Intel recommends that the initial route be completed based on the length matching formulas in conjunction with nominal package lengths and that package length compensation is performed as secondary operation.

7.3. Topologies and Routing Guidelines

The Intel 852GM GMCH chipset's Double Data Rate (DDR) SDRAM system memory interface implements the low swing, high-speed, terminated SSTL_2 topology. This section contains information related to the recommended interconnect topologies and routing guidelines for each of the signal groups that comprise the DDR interface. When implemented as defined, these guidelines will provide a robust DDR solution on an Intel 852GM GMCH chipset based design.

7.3.1. Clock Signals – SCK[4,3,1,0], SCK#[4,3,1,0]

The clock signal group includes the differential clock pairs SCK/SCK#[4,3,1,0]. The GMCH generates and drives these differential clock signals required by the DDR interface; therefore, no external clock driver is required for the DDR interface. The GMCH only supports unbuffered DDR SO-DIMMs; three differential clock pairs are routed to each SO-DIMM connector. Table 32 summarizes the clock signal mapping.

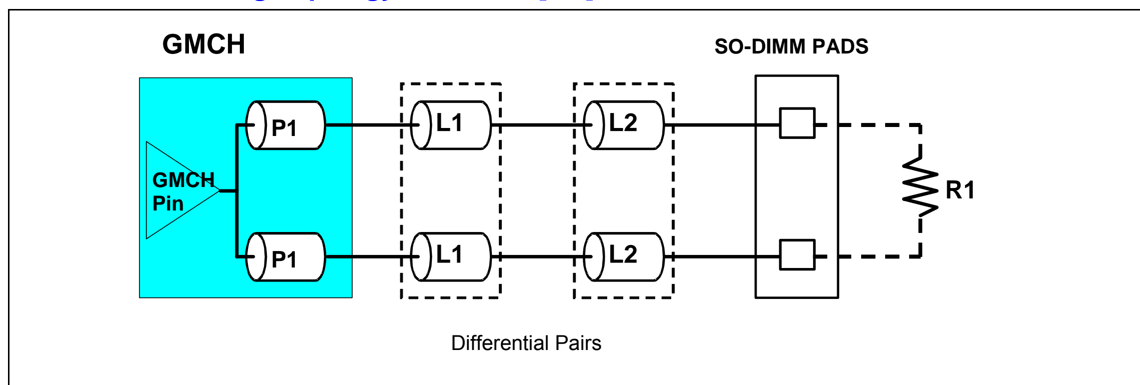
Table 32. Clock Signal Mapping

Signal	Relative To
SCK/SCK#[1:0]	SO-DIMM0
SCK/SCK#[4:3]	SO-DIMM1

7.3.2. Clock Topology Diagram

The Intel 852GM GMCH provides six differential clock output pairs, or three clock pairs per SO-DIMM socket. The motherboard clock routing topology is shown below for reference. Refer to the routing guidelines in Table 2 on the follow page for detailed length and spacing rules for each segment. The clock signals should be routed as closely coupled differential pairs over the entire length. Spacing to other DDR signals should not be less than 20 mils. Isolation spacing to non-DDR signals should be 25 mils.

Figure 43. DDR Clock Routing Topology SCK/SCK#[5:0]



The clock signals should be routed as closely coupled differential pairs over the entire length. Spacing to other DDR signals should not be less than 20 mils. Isolation spacing to non-DDR signals should be 25 mils.

7.3.3. DDR Clock Routing Guidelines

Table 33. Clock Signal Group Routing Guidelines

Parameter	Definition
Signal Group	SCK[4,3,1,0] and SCK#[4,3,1,0]
Topology	Differential Pair Point to Point
Reference Plane	Ground Referenced
Single Ended Trace Impedance (Zo)	42 ohms ± 15%
Differential Mode Impedance (Zdiff)	70 ohms ± 15%
Nominal Trace Width (see exceptions for breakout region below)	Inner Layers: 7 mils Outer Layers: 8 mils (pin escapes only)
Nominal Pair Spacing (edge to edge) (see exceptions for breakout region below)	Inner Layers: 4 mils Outer Layers: 5 mils (pin escapes only)
Minimum Pair to Pair Spacing (see exceptions for breakout region below)	20 mils
Minimum Serpentine Spacing	20 mils
Minimum Spacing to Other DDR Signals (see exceptions for breakout region below)	20 mils
Minimum Isolation Spacing to non-DDR Signals	25 mils
Maximum Via Count	2 (per side)
Package Length Range – P1	1000 mils ± 350 mils (See clock package length Table 34 for exact lengths.)
Trace Length Limits – L1	Max = 300 mils (breakout segment)
Total MB Length Limits – L1 + L2	Min = 0.5” Max = 5.0”
Total Length – P1 + L1 + L2	Total length target is determined by placement (see Figure 43) Total length for SO-DIMM0 group = X0 (see Figure 44) Total length for SO-DIMM1 group = X1 (see Figure 44)
SCLK to SCLK# Length Matching	Match total length to ±10 mils (see Section 7.3.3.1)
Clock to Clock Length Matching (Total Length)	Match all SO-DIMM0 clocks to X0 ± 25 mils (see Figure 44) Match all SO-DIMM1 clocks to X1 ± 25 mils (see Figure 44)
Breakout Exceptions (Reduced geometries for GMCH breakout region)	Inner Layers: 4 mil trace, 4 mil pair space allowed Outer Layers: 5 mil trace, 5 mil pair space allowed Pair to pair spacing of 5 mils allowed Spacing to other DDR signals of 5 mils allowed Maximum breakout length is 0.3”

NOTES:

1. Pad-to-Pin length tuning is utilized on clocks in order to achieve minimal variance. Package lengths range between approximately 600 mils and 1400 mils. Exact package lengths for each clock signal are provided at the end of this Section. Overall target length should be established based on placement and routing flow. The resulting motherboard segment lengths must fall within the ranges specified.
2. The DDR clocks should be routed on internal layers, except for pin escapes. It is recommended that pin escape vias be located directly adjacent to the ball pads on all clocks. Surface layer routing should be minimized.

3. Exceptions to the trace width and spacing geometries are allowed in the breakout region in order to fan-out the interconnect pattern. Reduced spacing should be avoided as much as possible.

7.3.3.1. Clock Length Matching Requirements

The GMCH chipset provides three differential clock pair for each SO-DIMM. A differential clock pair is made up of a SCK signal and its complement signal SCK#. Refer to Section 7.1 for more details on length matching requirements.

The differential pairs for one SO-DIMM are:

SCK[0] / SCK#[0]
SCK[1] / SCK#[1]

The differential pairs for the second SO-DIMM are:

SCK[3] / SCK#[3]
SCK[4] / SCK#[4]

The two sets of differential clocks must be length tuned on the motherboard such that any pair to pair package length variation is tuned out. The three pairs associated with SO-DIMM0 are tuned to a fixed overall length, including package, and the three pairs associated with SO-DIMM1 are tuned to a fixed overall length.

The two traces associated with each clock pair are length matched within the package, however some additional compensation may be required on the motherboard in order to achieve the ± 10 mil length tolerance within the pair.

Between clock pairs the package length varies substantially. Therefore, the motherboard length of each clock pair must be length adjusted to tune out package variance. The total length including package should be matched to within ± 25 mils of each other, as shown in the Figure 44 on the following page. This may result in a clock length variance of as much as 700 mils on the motherboard.

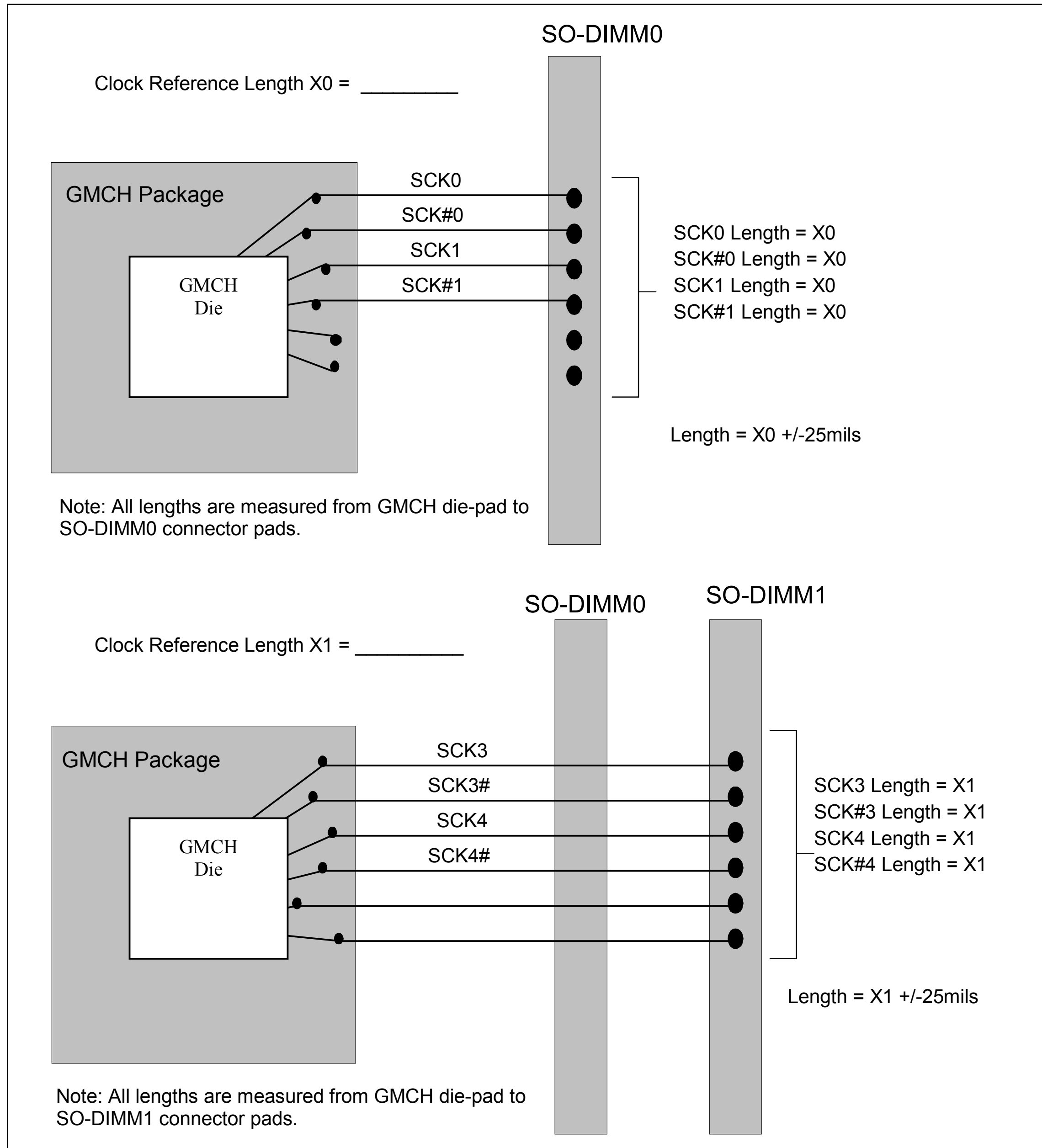
The first step in determining the routing lengths for clocks and all other clock relative signal groups is to establish the target length for each SO-DIMM clock group. These target lengths are shown as X0 and X1, in Figure 44. These are the lengths to which all clocks within the corresponding group will be matched, and the reference length values used to calculate the length ranges for the other signal groups.

7.3.3.2. Clock Reference Lengths

The clock reference length for each SO-DIMM clock group is determined by first determining the longest total clock length required to complete the clock routing. A table of clock package lengths is provided in Table 34 to assist in this calculation. Once the longest total length is determined for each clock group, this becomes a lower bound for the associated clock reference length. At this point it is helpful to have completed a test route of the SDQ/SDQS bus such that final clock reference lengths can be defined with consideration of the impact on SDQ/SDQS bus routability. Some iteration may be required.

Once the reference lengths X0 & X1 are defined then the next step is to tune each clock pairs's motherboard trace segment lengths as required such that the overall length of each clock equals the associated clock reference length plus or minus the 25-mil tolerance. Again, the reference length for the two sets of clocks should be offset by the nominal routing length between SO-DIMM connectors.

Figure 44. DDR Clock Trace Length Matching Diagram



7.3.3.3. Clock Package Length Table

The package length data in the table below should be used to tune the motherboard length of each SCLK/SCLK# clock pair between the GMCH and the associated SO-DIMM socket. Intel recommends that die-pad to SO-DIMM pin length be tuned to within ± 25 mils in order to optimize timing margins on the interface.

Table 34. DDR Clock Package Lengths

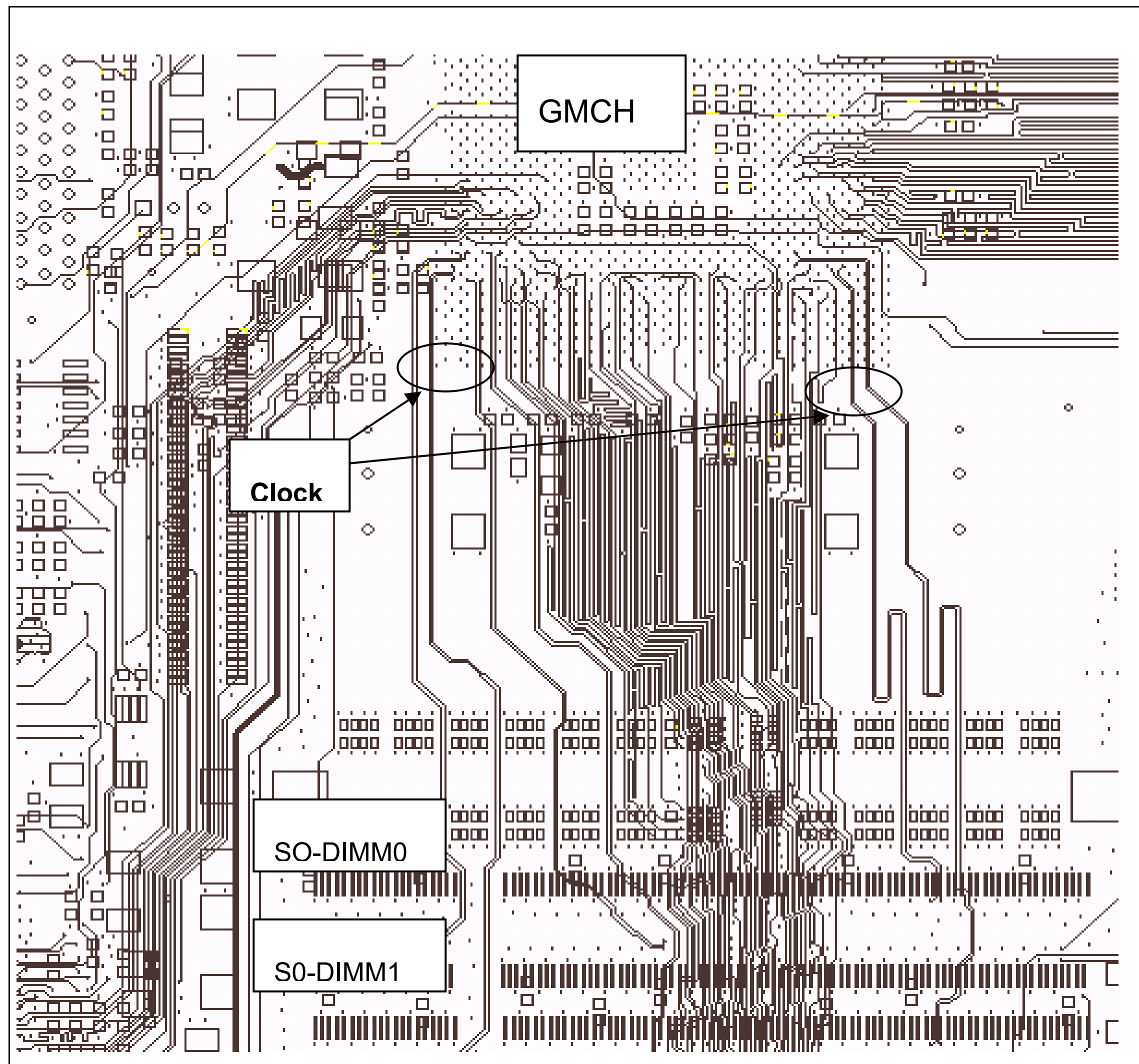
Signal	Pin Number	Package Length (mils)
SCLK_0	AB2	1177
SCLK#_0	AA2	1169
SCLK_1	AC26	840
SCLK#_1	AB25	838
SCLK_2	AC3	1129
SCLK#_2	AD4	1107
SCLK_3	AC2	1299
SCLK#_3	AD2	1305
SCLK_4	AB23	643
SCLK#_4	AB24	656
SCLK_5	AA3	1128
SCLK#_5	AB4	1146

Package length compensation can be performed on each individual clock output thereby matching total length on SCK/SCK# exactly, or alternatively the average package length can be used for both outputs of a pair and length tuning done with respect to the motherboard portion only.

7.3.3.4. Clock Routing Example

Figure 45 is an example of a board routing for the clock signal group.

Figure 45. Clock Signal Routing Example



7.3.3.4.1. Clock Routing Updates for “DDP Stacked” Memory Device Support

Simulation results show that the current DDR layout and routing guidelines for Intel 852GM chipset-based platforms can support “DDP stacked” SO-DIMM memory modules.

7.3.4. Data Signals – SDQ[64:0], SDM[7:0], SDQS[7:0]

The GMCH data signals are source synchronous signals that include a 64-bit wide data bus, a set of 8 data mask bits, and a set of 8 data strobe signals. There is an associated data strobe and data mask bit for each of the 8-bit data byte groups, making for a total of nine – 10-bit byte lanes. This section summarizes the SDQ/SDM to SDQS routing guidelines and length matching recommendations.

The data signals include SDQ[64:0], SDM[7:0], and SDQS[7:0].

- The data signals should transition from an external layer to an internal signal layer under the GMCH.
- Keep to the same internal layer until transitioning back to an external layer at the series resistor.
- After the series resistor, the signal should transition from the external layer to the same internal layer and route to SO-DIMM0.
- At SO-DIMM0, the signal should transition to an external layer and connect to the appropriate pad of the connector.
- After the SO-DIMM0 transition, continue to route the signal on the same internal layer to SO-DIMM1.
- Transition back out to an external layer and connect to the appropriate pad of SO-DIMM1.
- Connection to the termination resistor should be via the same internal layer with a transition back to the external layer near the resistor. External trace lengths should be minimized.

To facilitate routing, swapping of the byte lanes is allowed for SDQ[63:0] only. Bit swapping within the byte lane is also allowed for SDQ[63:0] only. It is suggested that the parallel termination be placed on both sides of SO-DIMM1 to simplify routing and minimize trace lengths. All internal and external signals should be ground referenced to keep the path of the return current continuous.

Resistor packs are acceptable for the series (Rs) and parallel (Rt) data and strobe termination resistors, but data and strobe signals can't be placed within the same R pack as the command or control signals. The table and diagrams below depict the recommended topology and layout routing guidelines for the DDR-SDRAM data signals.

Intel recommends that the full data bus SDQ[64:0], mask bus SDM[7:0], and strobe signals SDQS[7:0] be routed on the same internal signal layer. It is required that the SDQ byte group and the associated SDM and SDQS signals within a byte lane be routed on the same internal layer.

The total length of SDQ, SDM, and SDQS traces between the GMCH and the SO-DIMMs must be within the range defined in the overall guidelines, and is also constrained by a length range boundary based on SCK/SCK# clock length, and a SDQ/SDM to SDQS length matching requirement within each byte lane. Note also that all length matching must be done inclusive of package length. A table of SDQ, SDM, and SDQS package lengths is provided at the end of this Section to facilitate this process.

There are two levels of matching implemented on the data bus signals.

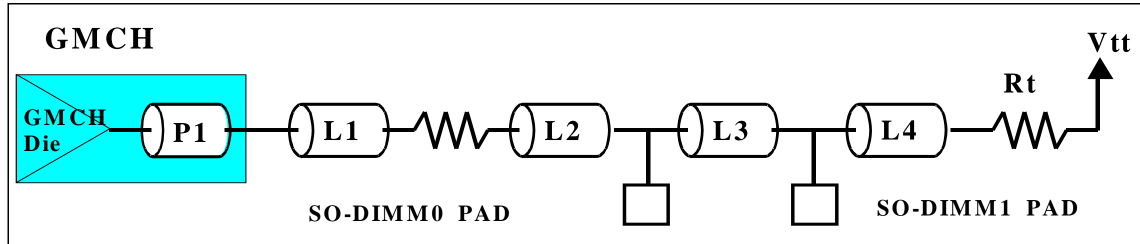
- The first is the length range constraint on the SDQS signals based on clock reference length.
- The second is SDQ/SDM to SDQS length matching within a byte lane.

The length of the SDQS signal for each byte lane must fall within a range determined by the clock reference length, as defined in the SDQS to SCK/SCK length matching section. The actual length of SDQS for each byte lane may fall anywhere within this range based on placement and routing flow.

Once the SDQS length for a byte lane is established, the SDQ, SDM, and SDQS signals within the byte lane must be length matched to each other, inclusive of package length, as described in the SDQ to SDQS length matching section.

7.3.4.1. Data Bus Topology

Figure 46. Data Signal Routing Topology



The data signals should be routed using a 2 to 1 trace spacing to trace width ratio for signals within the DDR group, except clocks and strobes. There should be a minimum of 20 mils of spacing to non-DDR related signals. Data signals should be routed on inner layers with minimized external trace lengths.

Table 35. Data Signal Group Routing Guidelines

Parameter	Definition
Signal Group	SDQ[64:0], SDQS[7:0], SDM[7:0]
Motherboard Topology	Daisy Chain with Parallel Termination
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Zo)	55 Ω ± 15%
Nominal Trace Width	Inner layers: 4 mils Outer layers: 5 mils
Minimum Spacing to Trace Width Ratio	SDQ/SDM: 2 to 1 (e.g. 8 mil space to 4 mil trace) SDQS: 3 to 1 (e.g. 12 mil space to 4 mil space)
Minimum Isolation Spacing to non-DDR Signals	20 mils
Package Length P1	700 mils ± 300 mils (See package length Table 37 for exact lengths.)
Trace Length L1 – GMCH Signal Ball to Series Termination Resistor Pad	Min = 0.5” Max = 3.75”
Trace Length L2 – Series Termination Resistor Pad to First SO-DIMM Pad	Max = 0.75”
Trace Length L3 – First SO-DIMM Pad to Last SO-DIMM Pad	Min = 0.25” Max = 1.0”
Trace Length L4 – Last SO-DIMM Pad to Parallel Termination Resistor Pad	Max = 1.0”
Length Matching Requirements	SDQS to SCK/SCK# See length matching Section 7.3.4.2 SDQ/SDM to SDQS, to ± 25mils, within each byte lane See length matching Section 7.3.4.3 and Figure 4

NOTES:

1. Power distribution vias from Rt to Vtt are not included in this count.
2. The overall minimum and maximum length to the SO-DIMM must comply with clock length matching requirements.
3. It is possible to route using 4 vias if trace segments L2 and L4 are routed on the same external layer as the associated SO-DIMM, for example if L2 is on the same layer as SO-DIMM0.

7.3.4.2. SDQS to Clock Length Matching Requirements

The first step in length matching is to determine the SDQS length range based on the SCK/SCK# reference length defined previously. The total length of the SDQS strobe signals, including package length, between the GMCH die-pad and the SO-DIMMs must fall within the range defined in the formulas below. See the clock Section for the definition of the clock reference length. Refer to Figure 46 for the definition of the various trace segments. The length tuning requirements are also depicted in Figure 47. Refer to Section 7.1 for more details on length matching and length formula requirements.

Length range formula for SO-DIMM0:

X_0 = SCK/SCLK#[1:0] total reference length, including package length. See clock Section 7.3.1.

Y_0 = SDQS[7:0] total length = GMCH package + L1 + L2, as shown in Figure 47,

where: $(X_0 - 1.0") \leq Y_0 \leq (X_0 + 0.5")$

Length range formula for SO-DIMM1:

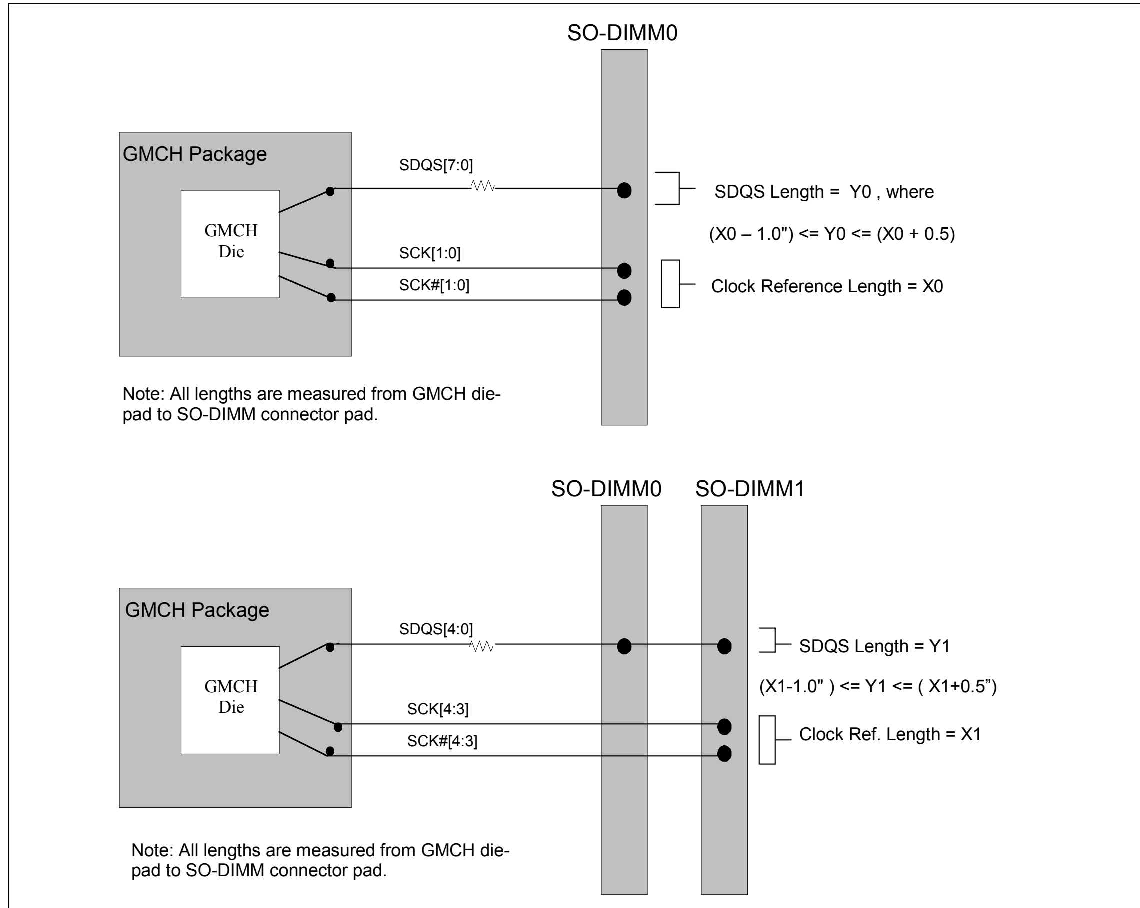
X_1 = SCK/SCK#[4:3] total reference length, including package length. See clock Section 7.3.1

Y_1 = SDQS[7:0] total length = GMCH package + L1 + L2 + L3, as shown Figure 47,

where: $(X_1 - 1.0") \leq Y_1 \leq (X_1 + 0.5")$

Length matching is only performed from the GMCH to the SO-DIMMs and does not involve the length of L4, which can vary over its entire range. Intel recommends that routing segment length L3 between SO-DIMM0 to SO-DIMM1 be held fairly constant and equal to the offset between clock reference lengths X0 and X1. This will produce the most straightforward length matching scenario. Note that a nominal SDQS package length of 750 mils can be used to estimate MB lengths prior to performing package length compensation. Refer to Section 7.2 for more details on package length compensation.

Figure 47. SDQS to Clock Trace Length Matching Diagram



7.3.4.3. Data to Strobe Length Matching Requirements

The data bit signals, SDQ[64:0] are grouped by byte lanes and associated with a data mask signal SDM[7:0], and a data strobe, SDQS[7:0].

- The data and mask signals must be length matched to their associated strobe within ± 25 mils, including package.
- For SO-DIMM0 this length matching includes the motherboard trace length to the pads of the SO-DIMM0 connector (L1 + L2) plus package length.
- For SO-DIMM1, the motherboard trace length to the pads of the SO-DIMM1 connector (L1 + L2 + L3) plus package length.

Refer to Section 7.2 for more details on package length compensation.

Length range formula for SDQ and SDM,

X = SDQS total length, including package length, as defined previously

Y = SDQ, SDM total length, including package length, within same byte lane as show in Figure 48,

where: $(X – 25 \text{ mils}) \leq Y \leq (X + 25 \text{ mils})$

Length matching is not required from the SO-DIMM1 to the parallel termination resistors. Figure 48 on the following page depicts the length matching requirements between the SDQ, SDM, and SDQS signals within a byte lane. Byte lane mapping is defined in Table 36 below.

7.3.4.4. SDQ to SDQS Mapping

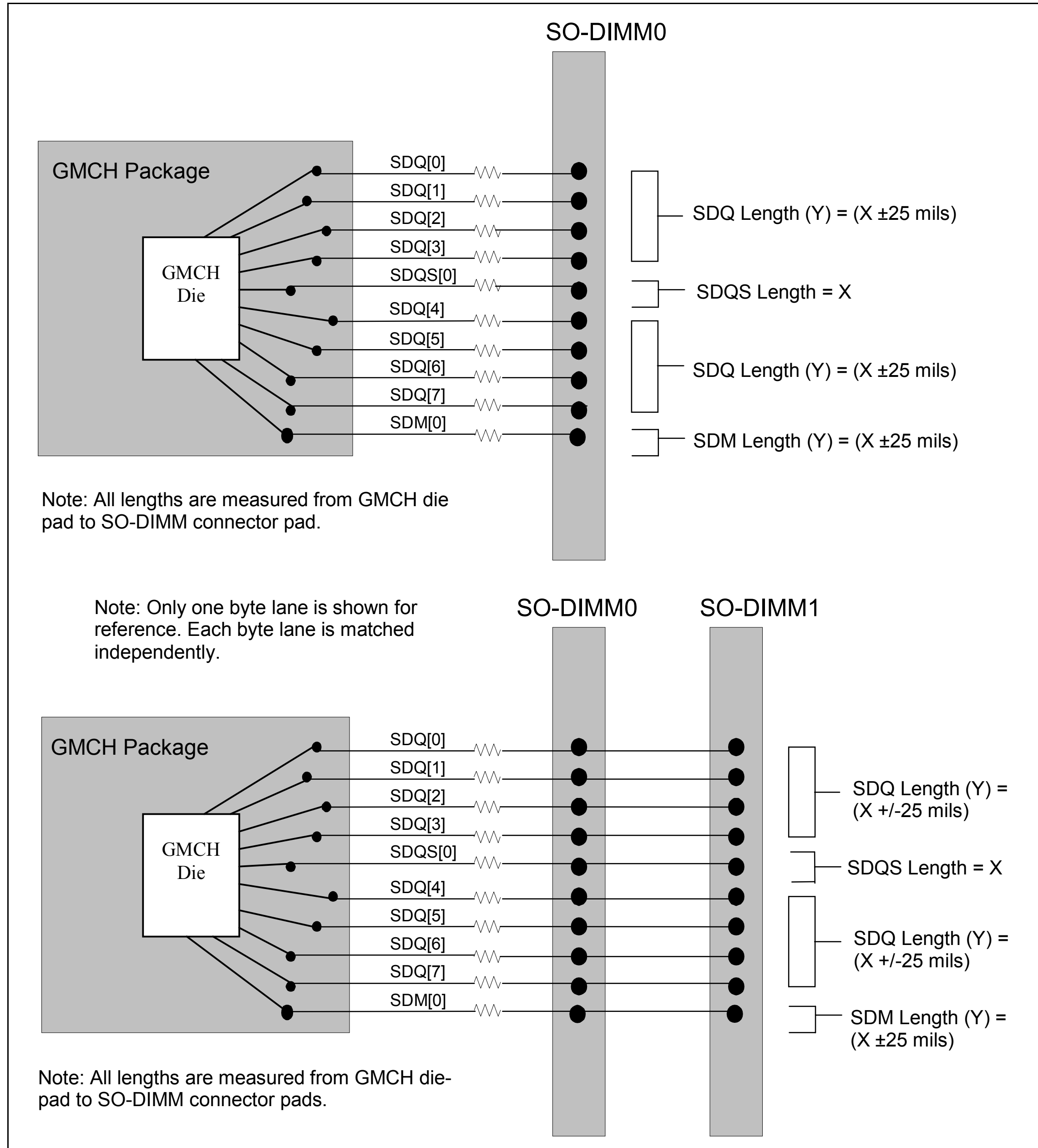
Table 36 below defines the mapping between the nine byte lanes, nine mask bits, and the nine SDQS signals, as required to do the required length matching.

The following signals are should not be routed out SDQ[71:64], SDM[8], and SDQS[8] as these signals are not supported in the Intel 852GM chipset.

Table 36. SDQ/SDM to SDQS Mapping

Signal	Mask	Relative To
SDQ[7:0]	SDM[0]	SDQS[0]
SDQ[15:8]	SDM[1]	SDQS[1]
SDQ[23:16]	SDM[2]	SDQS[2]
SDQ[31:24]	SDM[3]	SDQS[3]
SDQ[39:32]	SDM[4]	SDQS[4]
SDQ[56:40]	SDM[5]	SDQS[5]
SDQ[55:48]	SDM[6]	SDQS[6]
SDQ[63:56]	SDM[7]	SDQS[7]

Figure 48. SDQ/SDM to SDQS Trace Length Matching Diagram



7.3.4.5. SDQ/SDQS Signal Package Lengths

The package length data in Table 37 below should be used to tune the length of each SDQ, SDM, and SDQS motherboard trace as required to achieve the overall length matching requirements defined in the prior sections.

Table 37. DDR SDQ/SDM/SDQS Package Lengths

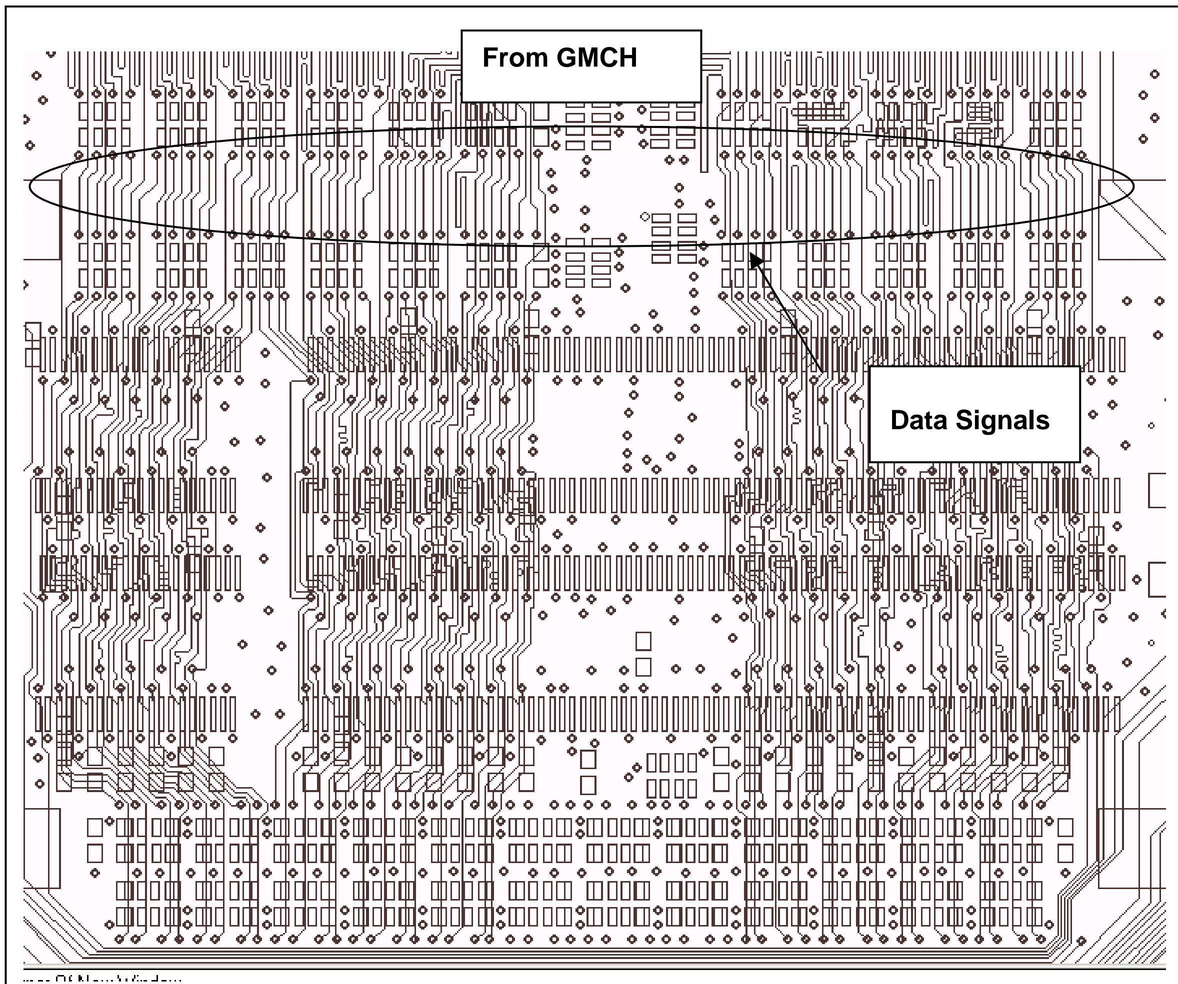
Signal	Pin Number	Pkg Length (mils)	Signal	Pin Number	Pkg Length (mils)
SDQ_00	AF2	785	SDQ_32	AH16	766
SDQ_01	AE3	751	SDQ_33	AG17	558
SDQ_02	AF4	690	SDQ_34	AF19	510
SDQ_03	AH2	903	SDQ_35	AE20	579
SDQ_04	AD3	682	SDQ_36	AD18	408
SDQ_05	AE2	739	SDQ_37	AE18	458
SDQ_06	AG4	741	SDQ_38	AH18	658
SDQ_07	AH3	845	SDQ_39	AG19	596
SDQ_08	AD6	607	SDQ_40	AH20	677
SDQ_09	AG5	756	SDQ_41	AG20	730
SDQ_10	AG7	685	SDQ_42	AF22	562
SDQ_11	AE8	558	SDQ_43	AH22	702
SDQ_12	AF5	734	SDQ_44	AF20	563
SDQ_13	AH4	825	SDQ_45	AH19	644
SDQ_14	AF7	644	SDQ_46	AH21	716
SDQ_15	AH6	912	SDQ_47	AG22	783
SDQ_16	AF8	622	SDQ_48	AE23	592
SDQ_17	AG8	624	SDQ_49	AH23	752
SDQ_18	AH9	676	SDQ_50	AE24	666
SDQ_19	AG10	634	SDQ_51	AH25	817
SDQ_20	AH7	710	SDQ_52	AG23	639
SDQ_21	AD9	508	SDQ_53	AF23	667
SDQ_22	AF10	569	SDQ_54	AF25	707
SDQ_23	AE11	469	SDQ_55	AG25	783
SDQ_24	AH10	648	SDQ_56	AH26	834
SDQ_25	AH11	622	SDQ_57	AE26	701
SDQ_26	AG13	572	SDQ_58	AG28	808

Signal	Pin Number	Pkg Length (mils)	Signal	Pin Number	Pkg Length (mils)
SDQ_27	AF14	655	SDQ_59	AF28	756
SDQ_28	AG11	599	SDQ_60	AG26	782
SDQ_29	AD12	460	SDQ_61	AF26	748
SDQ_30	AF13	536	SDQ_62	AE27	673
SDQ_31	AH13	642	SDQ_63	AD27	608
SDM_0	AE5	838	SDQS_0	AG2	925
SDM_1	AE6	693	SDQS_1	AH5	838
SDM_2	AE9	538	SDQS_2	AH8	756
SDM_3	AH12	606	SDQS_3	AE12	466
SDM_4	AD19	492	SDQS_4	AH17	678
SDM_5	AD21	470	SDQS_5	AE21	487
SDM_6	AD24	557	SDQS_6	AH24	770
SDM_7	AH28	917	SDQS_7	AH27	858

7.3.4.6. DDR Data Routing Example

Figure 49 is an example of a board routing for the Data signal group. The majority of the Data signal route is on an internal layer, both external layers can be used for parallel termination R-pack placement.

Figure 49. Data Signals Group Routing Example



7.3.5. Control Signals – SCKE[3:0], SCS#[3:0]

The Intel 852GM GMCH chipset control signals, SCKE[3:0] and SCS#[3:0], are clocked into the DDR SDRAM devices using clock signals SCK/SCK#[5:0]. The GMCH drives the control and clock signals together, with the clocks crossing in the valid control window. The GMCH provides one chip select (CS) and one clock enable (CKE) signal per SO-DIMM physical device row. Two chip select and two clock enable signals will be routed to each SO-DIMM. Refer to Table 38 for the CKE and CS# signal to SO-DIMM mapping.

Table 38. Control Signal to SO-DIMM Mapping

Signal	Relative To	SO-DIMM Pin
SCS#[0]	SO-DIMM0	AD23
SCS#[1]	SO-DIMM0	AD26
SCS#[2]	SO-DIMM1	AC22
SCS#[3]	SO-DIMM1	AC25
SCKE[0]	SO-DIMM0	AC7
SCKE[1]	SO-DIMM0	AB7
SCKE[2]	SO-DIMM1	AC9
SCKE[3]	SO-DIMM1	AC10

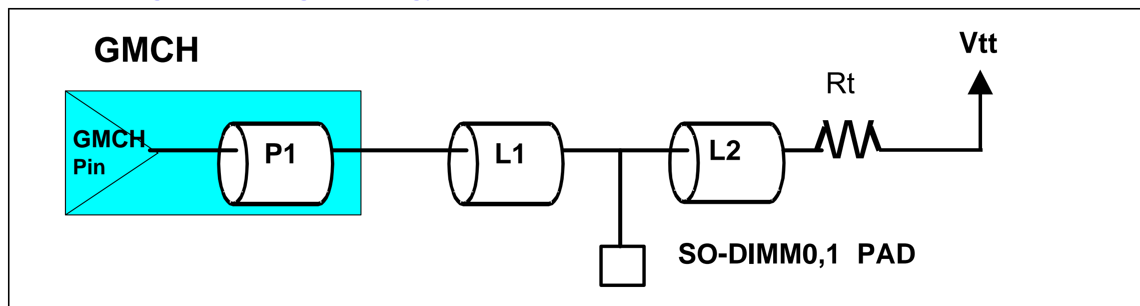
The control signal routing should transition from an external layer to an internal signal layer under the GMCH. Keep to the same internal layer until transitioning back out to an external layer to connect to the appropriate pad of the SO-DIMM connector and the parallel termination resistor. If the layout requires additional routing before the termination resistor, return to the same internal layer and transition back out to an external layer immediately prior to parallel termination resistor.

External trace lengths should be minimized. Intel suggests that the parallel termination be placed on both sides of the board to simplify routing and minimize trace lengths. All internal and external signals should be ground reference to keep the path of return current continuous. Intel suggests that all control signals be routed on the same internal layer.

Resistor packs are acceptable for the parallel (Rt) control termination resistors, but control signals can't be placed within the same R pack as the data or command signals. Figure 50 and Table 39 below depicts the recommended topology and layout routing guidelines for the DDR-SDRAM control signals.

7.3.5.1. Control Signal Topology

Figure 50. Control Signal Routing Topology



The control signals should be routed using 2 to 1 trace spacing to trace width ratio for signals within the DDR group, except clocks and strobes. There should be a minimum of 20-mils of spacing to non-DDR related signals. Control signals should be routed on inner layers with minimized external trace lengths.

7.3.5.2. Control Signal Routing Guidelines

Table 39. Control Signal Routing Guidelines

Parameter	Routing Guidelines
Signal Group	SCKE[3:0], SCS#[3:0]
Motherboard Topology	Point-to-Point with Parallel Termination
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Zo)	55 Ω ±15%
Nominal Trace Width	Inner layers: 4 mils Outer layers: 5 mils
Minimum Spacing to Trace Width Ratio	2 to 1 (e.g. 8 mil space to 4 mil trace)
Minimum Isolation Spacing to non-DDR Signals	20 mils
Package Length P1	500 mils ± 250 mils (See Table 40 for exact package lengths.)
Trace Length L1 – GMCH Control Signal Ball to SO-DIMM Pad	Min = 0.5 inches Max = 5.5 inches
Trace Length L2 – SO-DIMM Pad to Parallel Termination Resistor Pad	Max = 2.0 inches
Parallel Termination Resistor (Rt)	56 Ω ± 5%
Maximum Recommended Motherboard Via Count Per Signal	6
Length Matching Requirements	CTRL to SCK/SCK# [5:0] See length matching Section 7.3.5.3 and Figure 51.

NOTES:
1. Recommended resistor values and trace lengths may change in a later revision of the design guide.
2. Power distribution vias from Rt to Vtt are not included in this count.
3. It is possible to route using 2 vias if one via is shared that connects to the SO-DIMM pad and parallel termination resistor.
4. The overall maximum and minimum length to the SO-DIMM must comply with clock length matching requirements.

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7.3.5.3. Control to Clock Length Matching Requirements

The length of the control signals, between the GMCH die pad and the SO-DIMM must fall within the range defined below, with respect to the associated clock reference length. Refer to Figure 50 for a definition of the various trace segments that make up this path. The length of trace from the SO-DIMM to the termination resistor need not be length matched. The length matching requirements are also depicted in Figure 51. Refer to Section 7.1 for more details on length matching requirements.

Length range formula for SO-DIMM0:

X_0 = SCK/SCLK#[1:0] total reference length, including package length. See clock Section 7.3.1.

Y_0 = SCS#[1:0] & SCKE[1:0] total length = GMCH package length + L1, as shown in Figure 50,

where: $(X_0 - 1.0") \le Y_0 \le (X_0 + 0.5")$

Length range formula for SO-DIMM1:

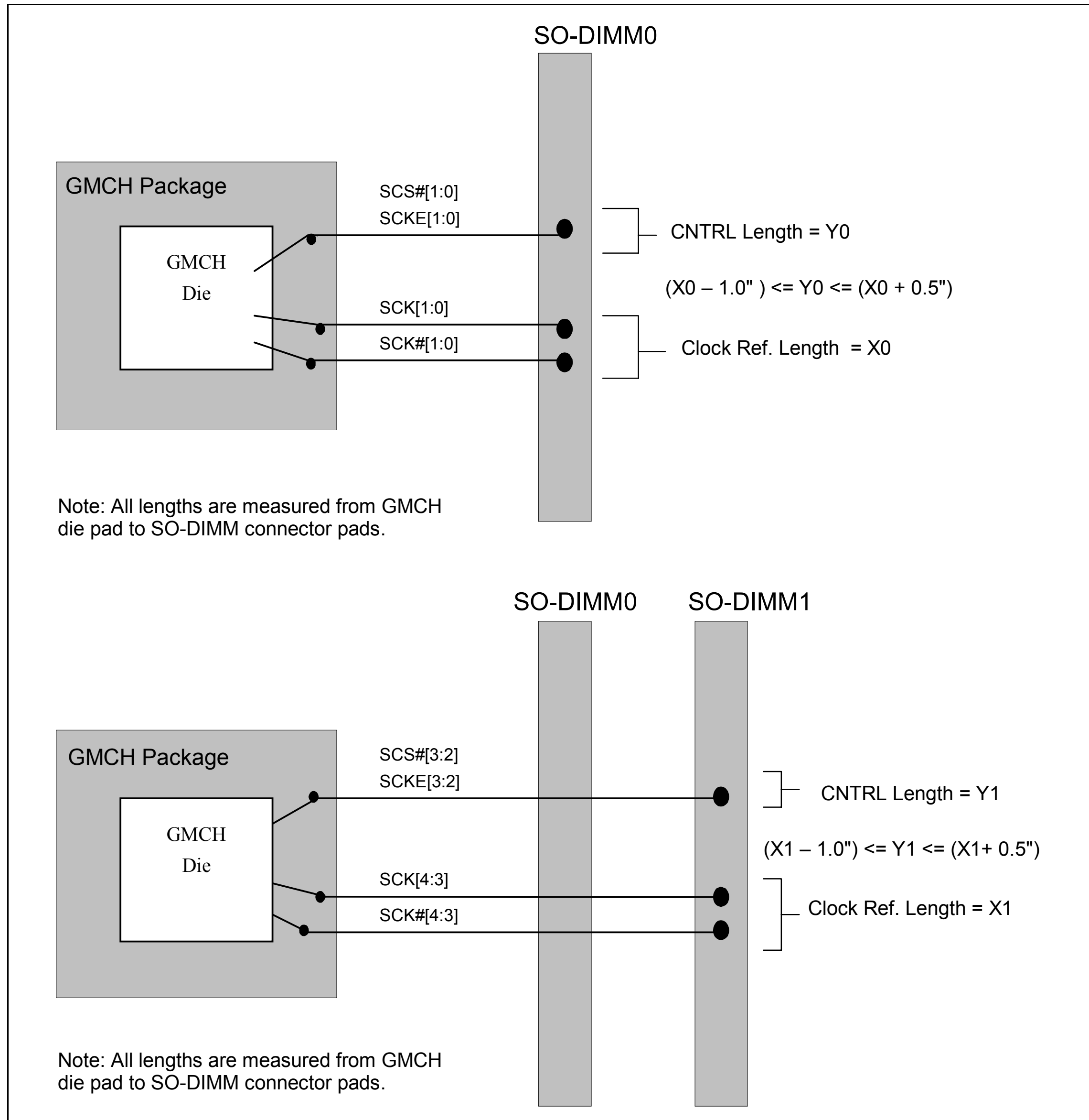
X_1 = SCK/SCLK#[4:3] total reference length, including package length. See clock Section 7.3.1.

Y_1 = SCS#[3:2] & SCKE[3:2] total length = GMCH package length + L1, as shown in Figure 50,

where: $(X_1 - 1.0") \le Y_1 \le (X_1 + 0.5")$

No length matching is required from the SO-DIMM to the termination resistor. Figure 51 on the following page depicts the length matching requirements between the control signals and clock. A nominal CS/CKE package length of 500 mils can be used to estimate baseline MB lengths. Refer to Section 7.2 for more details on package length compensation.

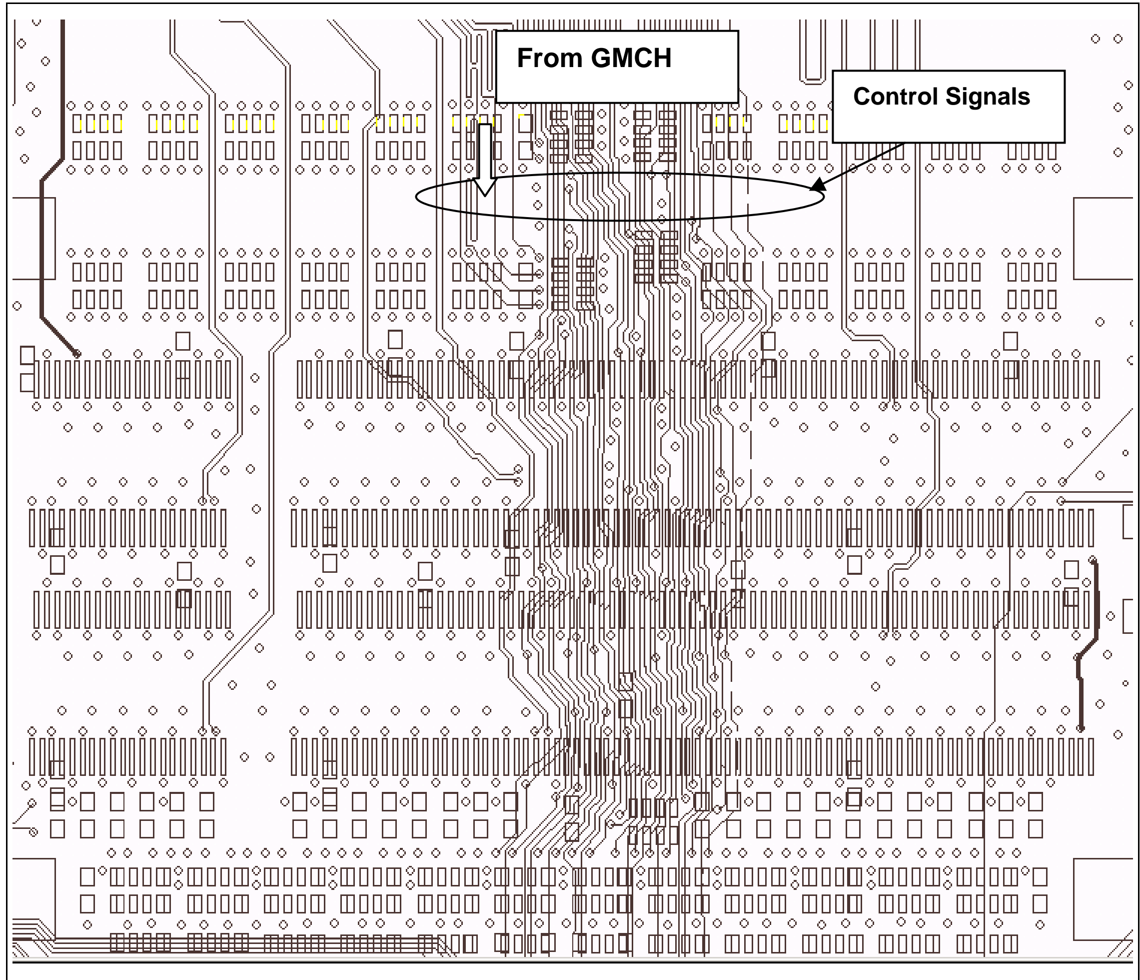
Figure 51. Control Signal to Clock Trace Length Matching Diagram



7.3.5.4. DDR Control Routing Example

Figure 52 is an example of a board routing for the Control signal group.

Figure 52. Control Signals Group Routing Example



7.3.5.5. Control Group Package Length Table

The package length data in Table 40 below should be used to match the overall length of each command signal to its associated clock reference length. Note that due to the relatively small variance in package length and adequate timing margins it is acceptable to use a fixed 500-mil nominal package length for all control signals, thereby reducing the complexity of the motherboard length calculations.

Table 40. Control Group Package Lengths

Signal	Pin Number	Package Length (mils)
SCS#[0]	AD23	502
SCS#[1]	AD26	659
SCS#[2]	AC22	544
SCS#[3]	AC25	612
SCKE[0]	AC7	443
SCKE[1]	AB7	389
SCKE[2]	AC9	386
SCKE[3]	AC10	376

7.3.6. Command Signals – SMA[12:6,3,0], SBA[1:0], SRAS#, SCAS#, SWE#

The Intel 852GM GMCH chipset command signals, SMA[12:0], SBA[1:0], SRAS#, SCAS#, and SWE# clocked into the DDR SDRAMs using the clock signals SCK/SCK#[5:0]. The GMCH drives the command and clock signals together, with the clocks crossing in the valid command window. There are two supported topologies for the command signal group, Topology 1, which is a daisy chain topology, and Topology 2, which implements a T routing topology. Both topologies place a series resistor between the two SO-DIMMs to dampen the SO-DIMM to SO-DIMM resonance. Topology 2 is the topology that best allows for placement of the SO-DIMMs back to back in the butterfly configuration, thus minimizing the SO-DIMM footprint area.

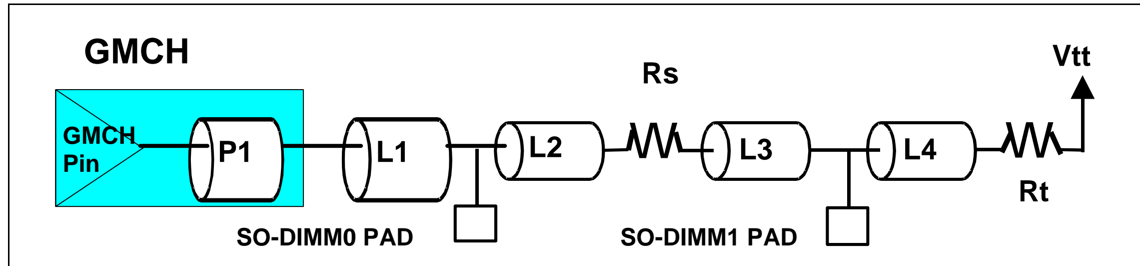
7.3.6.1. Command Topology 1

The command signal routing should transition from an external layer to an internal signal layer under the GMCH. Keep to the same internal layer until transitioning back to an external layer immediately prior to connecting the SO-DIMM0 connector pad. At the via transition for SO-DIMM0, continue the signal route on the same internal layer to the series termination resistor (Rs), connected to SO-DIMM1. At this resistor the signal should transition to an external layer immediately prior to the pad of Rs. After the series resistor, Rs, continue the signal route on the external layer landing on the appropriate connector pad of SO-DIMM1. After SO-DIMM1, transition to the same internal layer or stay on the external layer and route the signal to Rt.

Intel suggests that the parallel termination (Rt) be placed on both sides of the board to simplify routing and minimize trace lengths. All internal and external signals should be ground referenced to keep the path of the return current continuous.

Resistor packs are acceptable for the series and parallel command termination resistors but command signals can not be placed within the same R-packs as data, strobe, or control signals. Figure 53 and Table 41 below depict the recommended topology and layout routing guidelines for the DDR-SDRAM command signals routing to SO-DIMM0 and SO-DIMM1.

Figure 53. Command Routing for Topology 1



The command signals should be routed using a 2 to 1 trace spacing to trace width ratio for signals within the DDR group, except clocks and strobes. There should be a minimum of 20 mils spacing to non-DDR related signals. Command signals should be routed on inner layers with minimized external traces.

7.3.6.2. Command Topology 1 Routing Guidelines

Table 41. Command Topology 1 Routing Guidelines

Parameter	Routing Guidelines
Signal Group	SMA[12:6,3,0], SBA[1:0], SRAS#, SCAS#, SWE#
Motherboard Topology	Daisy Chain with Parallel Termination
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Zo)	55 Ω ± 15%
Nominal Trace Width	Inner layers: 4 mils Outer layers: 5 mils
Minimum Spacing to Trace Width Ratio	2 to 1 (e.g. 8 mil space to 4 mil trace)
Minimum Isolation Spacing to non-DDR Signals	20 mils
Package Length P1	500 mils ± 250 mils (See Table 44 for exact package lengths.)
Trace Length L1 – GMCH Command Signal Ball to First SO-DIMM Pad	Min = 0.5 inch Max = 4.0 inches
Trace Length L2 – First SO-DIMM Pad to Series Resistor Pad	Max = 1.5 inches
Trace Length L3 – Series Resistor Pad to Second SO-DIMM Pad	Max = 1.5 inches
Trace Length L2 + L3 – Total SO-DIMM to SO-DIMM spacing	Max = 3.0 inches
Trace Length L4 – Second SO-DIMM Pad to Parallel Resistor Pad	Max = 1.0 inches
Series Termination Resistor (Rs)	10 Ω ± 5%
Parallel Termination Resistor (Rt)	56 Ω ± 5%
Maximum Recommended Motherboard Via Count Per Signal	6
Length Matching Requirements	CMD to SCK/SCK# [5:0] See length matching Section 7.3.6.3 and Figure 54 for details.

NOTES:
1. Recommended resistor values and trace lengths may change in a later revision of the design guide.
2. Power distribution vias from Rt to Vtt are not included in this count.
3. The overall maximum and minimum length to the SO-DIMM must comply with clock length matching requirements.
4. It is possible to route using four vias if one via is shared that connects to the SO-DIMM1 pad and parallel termination resistor.

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7.3.6.3. Command Topology 1 Length Matching Requirements

The routing length of the command signals, between the GMCH die pad and the SO-DIMM must be within the range defined below, with respect to the associated clock reference length. Refer to Figure 53 for a definition of the various motherboard trace segments. The length of trace from the SO-DIMM to the termination resistor need not be length matched. The length matching requirements are also depicted in Figure 54. Refer to Section 7.1 for more details on length matching requirements.

Length range formula for SO-DIMM0:

X0 = SCK/SCLK#[2:0] total reference length, including package length. See clock Section 7.3.1.

Y0 = CMD signal total length = GMCH package + L1, as shown in Figure 53,

where: $(X_0 - 1.0") \le Y_0 \le (X_0 + 2.0")$

Length range formula for SO-DIMM1:

X1 = SCK/SCLK#[5:3] total reference length, including package length. See clock Section 7.3.1.

Y1 = CMD signal total length = GMCH package + L1 + L2 + L3, as shown in Figure 53,

where: $(X_1 - 1.0") \le Y_1 \le (X_1 + 2.0")$

No length matching is required from SO-DIMM1 to the termination resistor. Figure 54 on the following page depicts the length matching requirements between the command signals and clock. A nominal CMD package length of 500 mils can be used to estimate baseline MB lengths. Refer to Section 7.2 for more details on package length compensation.

Figure 54. Topology 1 Command Signal to Clock Trace Length Matching Diagram

SO-DIMM0

GMCH Package

GMCH
Die

SMAA[12:6,3,0]
SBA[1:0],
RAS#, CAS#,
WE#

CMD Length = Y0

(X0 – 1.0") <= Y0 <= (X0 + 2.0")

SCK[2:0]

SCK#[2:0]

Clock Reference Length = X0

Note: All lengths are measured from GMCH die pad to SO-DIMM connector pad.

SO-DIMM0

SO-DIMM1

GMCH Package

GMCH
Die

SMAA[12:6,3,0]
SBA[1:0],
RAS#, CAS#,
WE#

CMD Length = Y1

(X1 –1.0") <= Y1 <= (X1 +2.0")

SCK[5:3]

SCK#[5:3]

Clock Ref Length = X1

Note: All lengths are measured from GMCH die pad to SO-DIMM connector pad.

7.3.6.4. Command Topology 2

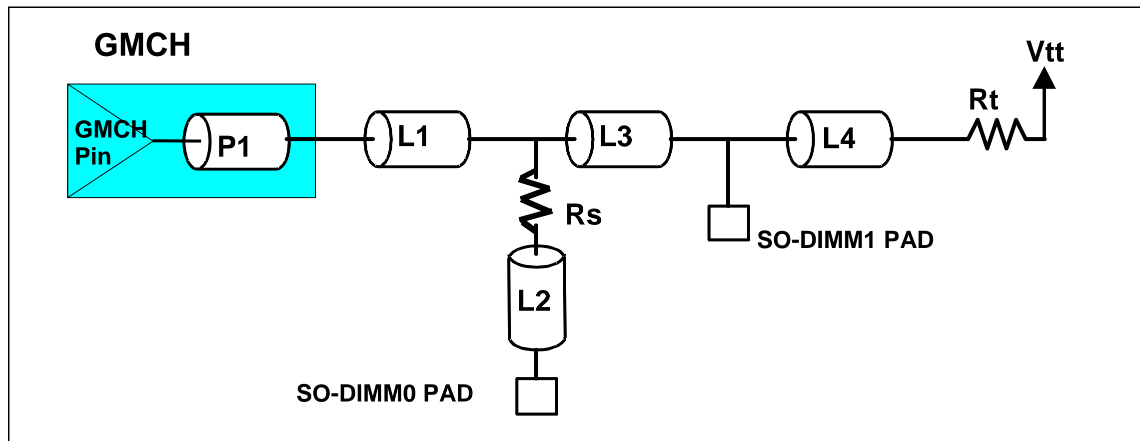
The command signal routing should transition from an external layer to an internal signal layer under the GMCH. Keep to the same internal layer until transitioning back to an external layer at the series resistor Rs. At this point there is a T in the topology. One leg of the T will route through Rs and either transition back to the same internal layer or stay external and landing on the appropriate connector pad of SO-DIMM0. If it was necessary to return to the internal layer the signal should return to the external layer immediately prior to landing on the appropriate connector pad of SO-DIMM0. The other leg of the T will continue on the same internal layer and return to the external layer immediately prior to landing on the appropriate connector pad of SO-DIMM1. If possible stay on the external layer and connect to the parallel termination resistor or if the parallel termination resistor is on the opposite side of the board from the SO-DIMM1 connector then share the via and route to the parallel termination resistor. If sharing the via or using the opposite side of the board is not possible, continue on the same internal layer and route to the external layer immediately prior to the termination resistor.

External trace lengths should be minimized. It is suggested that the parallel termination be placed on both sides of the board to simplify routing and minimize trace lengths. All internal and external signals should be ground referenced to keep the path of the return current continuous. It is recommended that command signal group be routed on same internal layer.

Intel suggests that the parallel termination (Rt) be placed on both sides of the board to simplify routing and minimize trace lengths. All internal and external signals should be ground referenced to keep the path of the return current continuous.

Resistor packs are acceptable for the series and parallel command termination resistors but command signals can not be placed within the same R-packs as data, strobe or control signals. Figure 55 and Table 42 below depict the recommended topology and layout routing guidelines for the DDR-SDRAM command signals routing to SO-DIMM0 and SO-DIMM1.

Figure 55. Command Routing Topology 2



The command signals should be routed using a 2 to 1 trace spacing to trace width ratio for signals within the DDR group, except clocks and strobes. There should be a minimum of 20 mils of spacing to non-DDR related signals. Command signals should be routed on inner layers with minimized external trace lengths.

7.3.6.5. Command Topology 2 Routing Guidelines

Table 42. Command Topology 2 Routing Guidelines

Parameter	Routing Guidelines
Signal Group	SMA[12:6,3,0], SBA[1:0], SRAS#, SCAS#, SWE#
Motherboard Topology	Branched T with Parallel Termination
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Zo)	55 Ω ± 15%
Nominal Trace Width	Inner layers: 4 mils Outer layers: 5 mils
Minimum Spacing to Trace Width Ratio	2 to 1 (e.g. 8 mil space to 4 mil trace)
Minimum Isolation Spacing to non-DDR Signals	20 mils
Package Length P1	500 mils ± 250 mils (See Table 44 for exact package length.)
Trace Length L1 – GMCH Command Signal Ball to Series Resistor Pad	Min = 0.5 inches Max = 4.0 inches
Trace Length L2 – Series Resistor Pad to First SO-DIMM Pad	Max = 1.0 inches
Trace Length L3 – Series Resistor Pad to Second SO-DIMM Pad	Max = 2.0 inches
Trace Length L2 + L3 – Total SO-DIMM to SO-DIMM spacing	Max = 3.0 inches
Trace Length L4 – Second SO-DIMM Pad to Parallel Resistor Pad	Max = 1.0 inches
Series Termination Resistor (Rs)	10 Ω ± 5%
Parallel Termination Resistor (Rt)	56 Ω ± 5%
Maximum Recommended Motherboard Via Count Per Signal	6
Length Matching Requirements	CMD to SCK/SCK# [5:0] See length matching Section 7.3.6.6 and Figure 56 for details.

NOTES:
1. Recommended resistor values and trace lengths may change in a later revision of the design guide.
2. Power distribution vias from Rt to Vtt are not included in this count.
3. The overall maximum and minimum length to the SO-DIMM must comply with clock length matching requirements.
4. It is possible to route using three vias if one via is shared that connects to the SO-DIMM0 pad and series termination resistor, if a via is shared that connects L1 to series termination and if one via is shared that connects to the SO-DIMM1 pad and parallel termination resistor.

7.3.6.6. Command Topology 2 Length Matching Requirements

The routed length of the command signals, between the GMCH package ball and the SO-DIMM must be within the range defined below, with respect to the associated clock reference length. Refer to Figure 55 for a definition of the various motherboard trace segments. The length of trace from the SO-DIMM to the termination resistor need not be length matched. The length matching requirements are also depicted in Figure 56. Refer to Section 7.1 for more details on length matching requirements.

Length range formula for SO-DIMM0:

$\mathbf{X_0}$ = SCK/SCLK#[2:0] total reference length, including package length. See clock Section 7.3.1.

$\mathbf{Y_0}$ = CMD signal total length = GMCH package + L1 + L2, as shown in Figure 55,

where: $(X_0 - 1.0") \leq Y_0 \leq (X_0 + 2.0")$

Length range formula for SO-DIMM1:

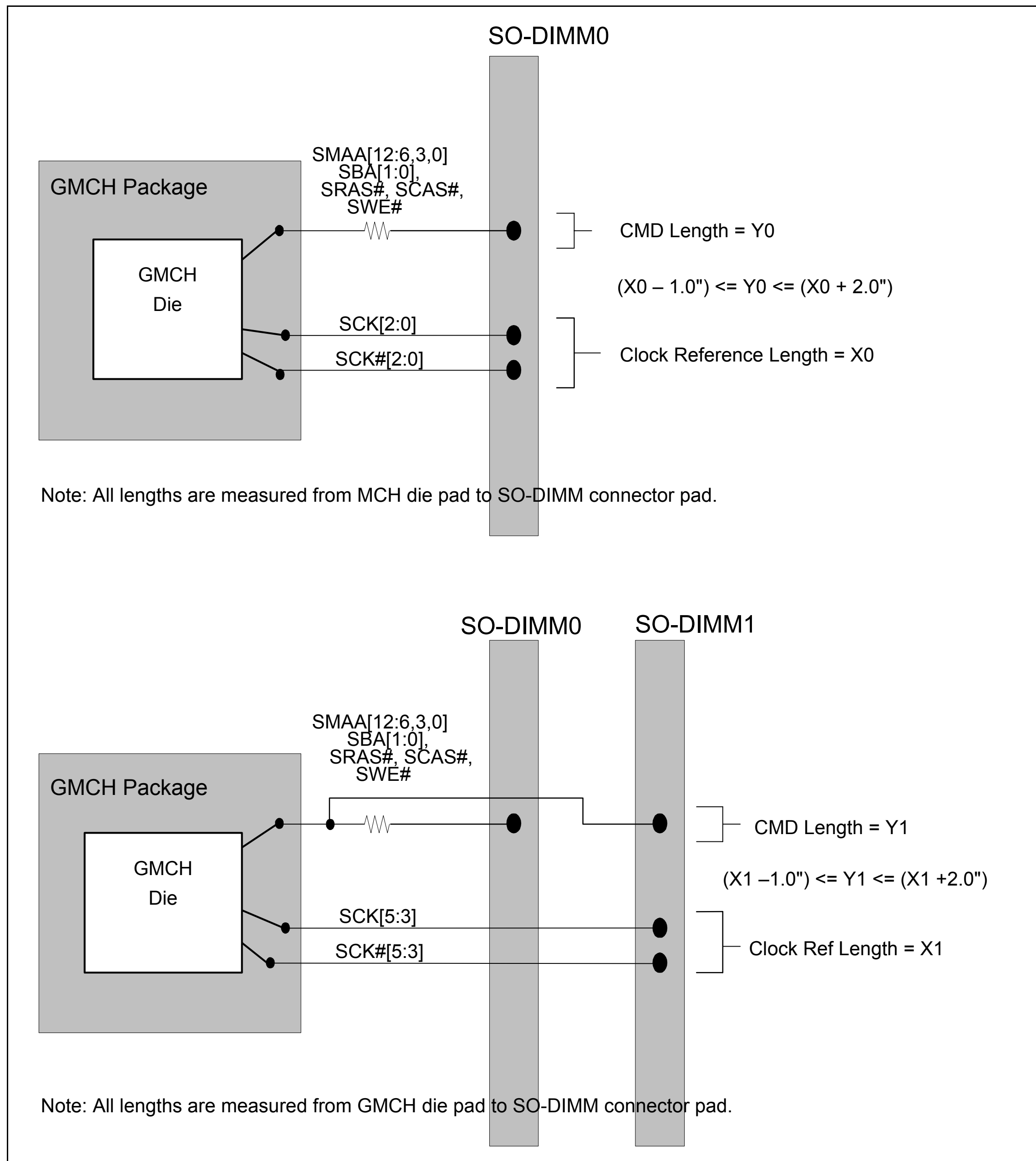
$\mathbf{X_2}$ = SCK/SCLK#[5:3] total reference length, including package length. See clock Section 7.3.1.

$\mathbf{Y_2}$ = CMD signal total length = GMCH package length + L1 + L3, as shown in Figure 55,

where: $(X_1 - 1.0") \leq Y_1 \leq (X_1 + 2.0")$

No length matching is required from SO-DIMM1 to the termination resistor. Figure 56 on the following page depicts the length matching requirements between the command signals and clock. A nominal CMD package length of 500 mils can be used to estimate baseline MB lengths. Refer to Section 7.2 for more details on package length compensation.

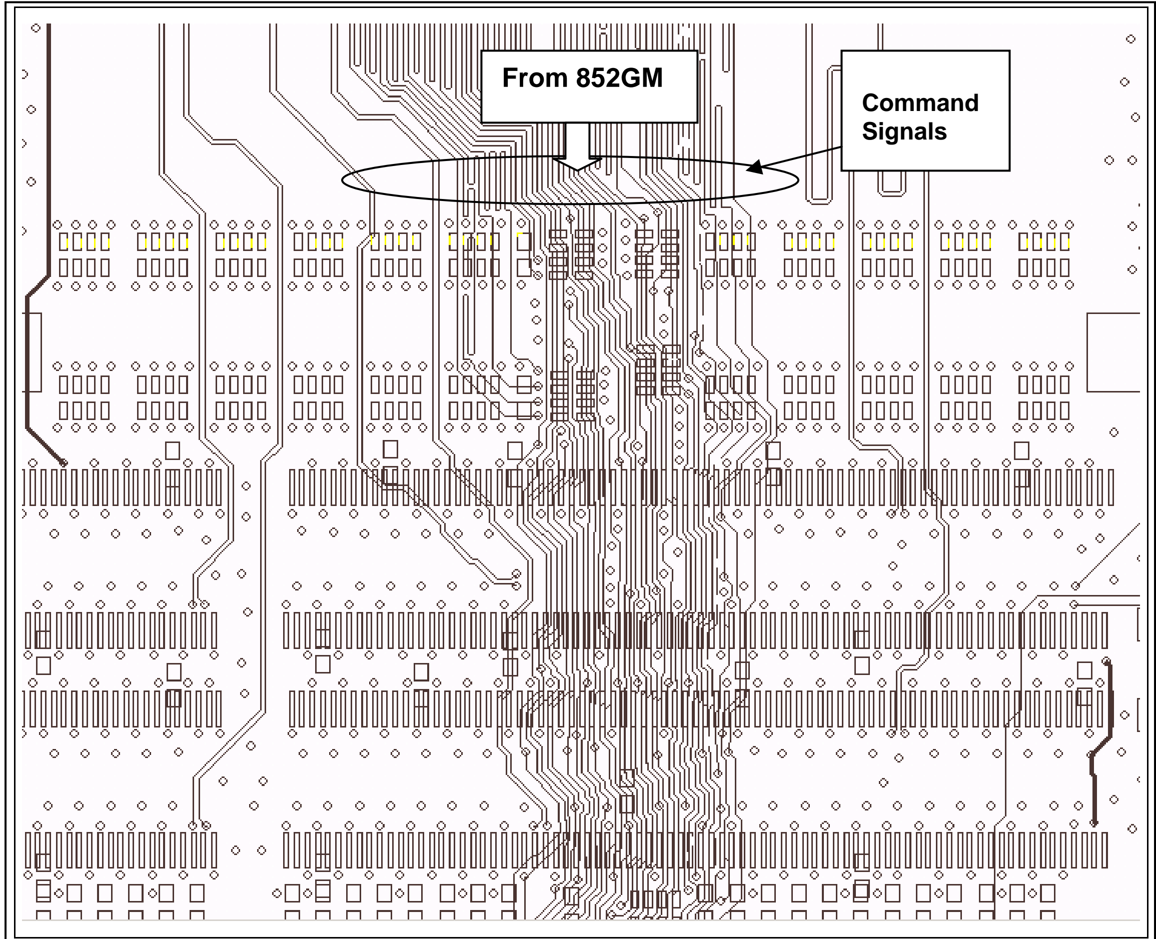
Figure 56. Topology 2 Command Signal to Clock Trace Length Matching Diagram



7.3.6.7. Command Topology 2 Routing Example

Figure 57 is an example of a board routing for the Command signal group.

Figure 57. Example of Command Signal Group



7.3.6.8. Command Topology 3

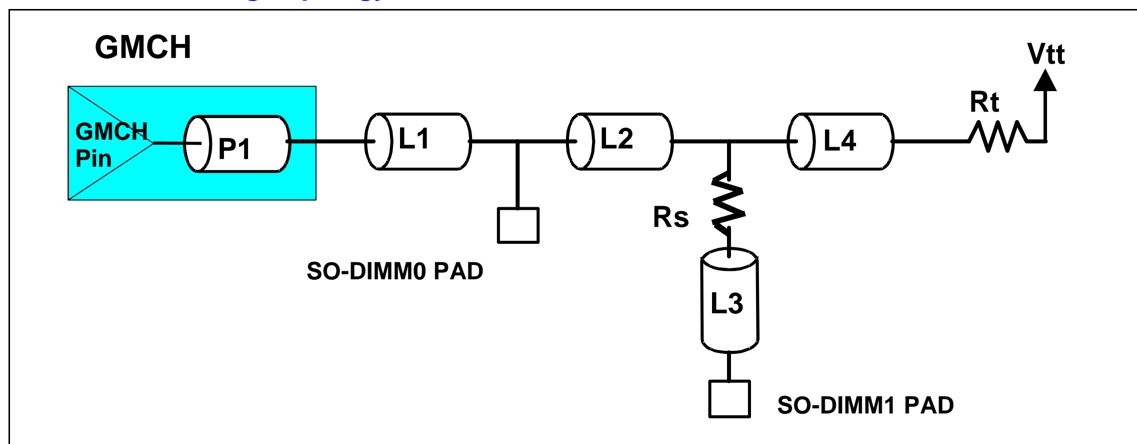
This topology is recommended when the SO-DIMMS are too close together for the series resistor to be placed between connectors. In this topology the series resistors are placed behind the second SO-DIMM.

External trace lengths should be minimized. It is suggested that the parallel termination be placed on both sides of the board to simplify routing and minimize trace lengths. All internal and external signals should be ground referenced to keep the path of the return current continuous. Intel recommends that command signal group be routed on same internal layer.

Intel suggests that the parallel termination (Rt) be placed on both sides of the board to simplify routing and minimize trace lengths. All internal and external signals should be ground referenced to keep the path of the return current continuous.

Resistor packs are acceptable for the series and parallel command termination resistors but command signals can't be placed within the same R-packs as data, strobe or control signals. The diagrams and tables below depict the recommended topology and layout routing guidelines for the DDR-SDRAM command signals routing to SO-DIMM0 and SO-DIMM1.

Figure 58. Command Routing Topology 3



The command signals should be routed using a 2 to 1 trace spacing to trace width ratio for signals within the DDR group, except clocks and strobes. There should be a minimum of 20 mils of spacing to non-DDR related signals. Command signals should be routed on inner layers with minimized external trace lengths.

7.3.6.9. Command Topology 3 Routing Guidelines

Table 43. Command Topology 3 Routing Guidelines

Parameter	Routing Guidelines
Signal Group	SMA[12:6,3,0], SBA[1:0], SRAS#, SCAS#, SWE#
Motherboard Topology	Branched T with Parallel Termination
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Zo)	55Ω ± 15%
Nominal Trace Width	Inner layers: 4 mils Outer layers: 5 mils
Minimum Spacing to Trace Width Ratio	2 to 1 (e.g. 8 mil space to 4 mil trace)
Minimum Isolation Spacing to non-DDR Signals	20 mils
Package Length P1	500 mils ± 250 mils (See Table 44 for exact package lengths.)
Trace Length L1 – GMCH Command Signal Ball to First SO-DIMM Pad	Min = 0.5 inches Max = 4.0 inches
Trace Length L2 – First SO-DIMM Pad to Series Resistor Pad	Max = 2.0 inches
Trace Length L3 – Series Resistor Pad to Second SO-DIMM Pad	Max = 1.0 inches
Trace Length L2 + L3 – Total SO-DIMM to SO-DIMM spacing	Max = 3.0 inches
Trace Length L4 – Series Resistor Pad to Parallel Resistor Pad	Max = 1.0 inches
Series Termination Resistor (Rs)	10 Ω ± 5%
Parallel Termination Resistor (Rt)	56 Ω ± 5%
Maximum Recommended Motherboard Via Count Per Signal	6
Length Matching Requirements	CMD to SCK/SCK# [5:0] See length matching Section 7.3.6.10 and Figure 59 for details.

NOTES:

1. Recommended resistor values and trace lengths may change in a later revision of the design guide.
2. Power distribution vias from Rt to Vtt are not included in this count.
3. The overall maximum and minimum length to the SO-DIMM must comply with clock length matching requirements.
4. It is possible to route using three vias if one via is shared that connects to the SO-DIMM0 pad and series termination resistor, if a via is shared that connects L1 to series termination and if one via is shared that connects to the SO-DIMM1 pad and parallel termination resistor.

7.3.6.10. Command Topology 3 Length Matching Requirements

The routed length of the command signals, between the GMCH package ball and the SO-DIMM must be within the range defined below, with respect to the associated clock reference length. Refer to Figure 55 for a definition of the various motherboard trace segments. The length of trace from the SO-DIMM to the termination resistor need not be length matched. The length matching requirements are also depicted in Figure 56. Refer to Section 7.1 for more details on length matching requirements.

Length range formula for SO-DIMM0:

$\mathbf{X_0}$ = SCK/SCLK#[2:0] total reference length, including package length. See clock Section 7.3.1.

$\mathbf{Y_0}$ = CMD signal total length = GMCH package + L1, as shown in Figure 55,

where: $(X_0 – 1.0”) \le Y_0 \le (X_0 + 2.0”)$

Length range formula for SO-DIMM1:

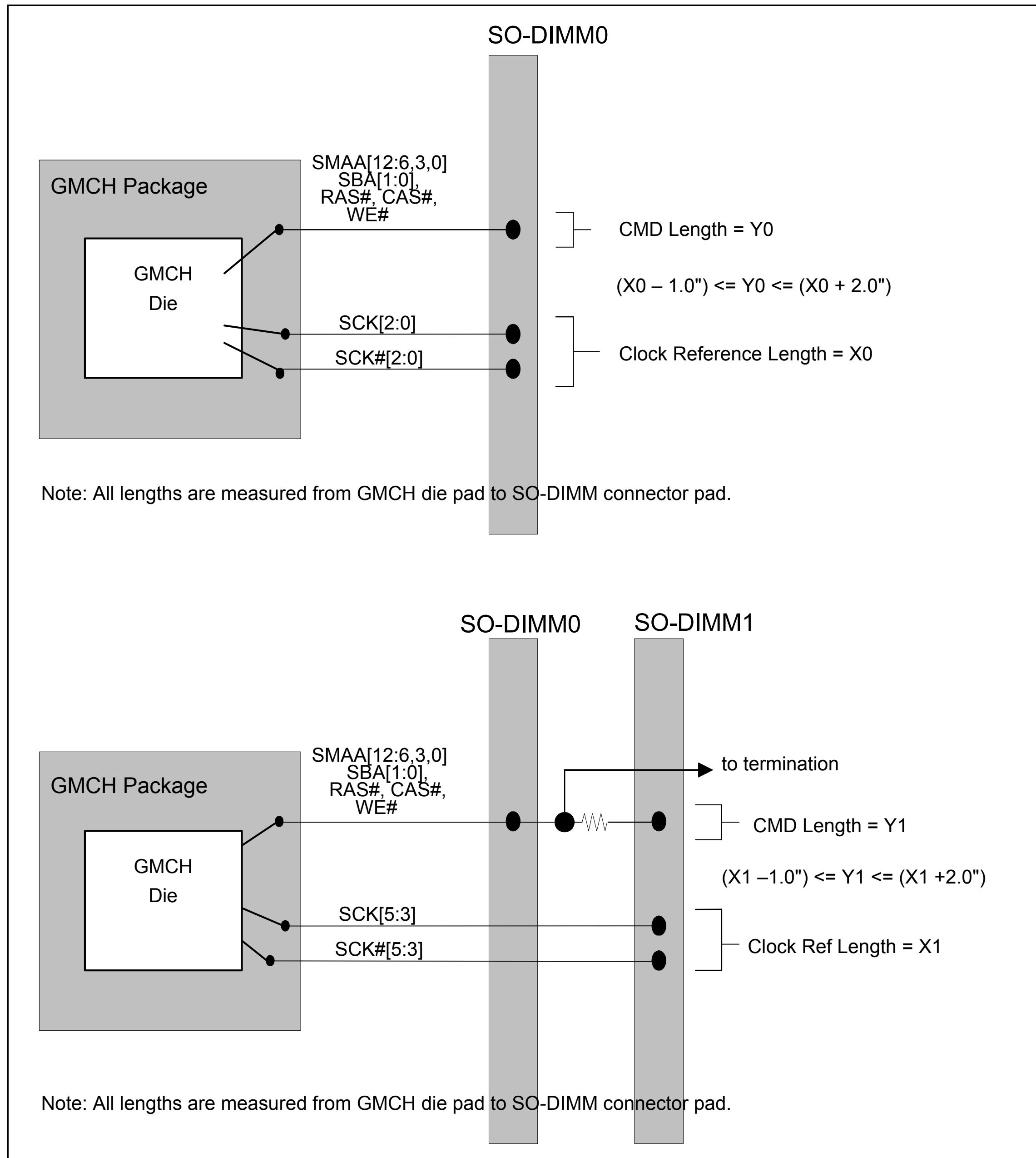
$\mathbf{X_2}$ = SCK/SCLK#[5:3] total reference length, including package length. See clock Section 7.3.1.

$\mathbf{Y_2}$ = CMD signal total length = GMCH package length + L1 + L2 +L3, as shown in Figure 55,

where: $(X_1 – 1.0”) \le Y_1 \le (X_1 + 2.0”)$

No length matching is required from SO-DIMM1 to the termination resistor. Figure 56 on the following page depicts the length matching requirements between the command signals and clock. A nominal CMD package length of 500 mils can be used to estimate baseline MB lengths. Refer to Section 7.2 for more details on package length compensation.

Figure 59. Topology 3 Command Signal to Clock Trace Length Matching Diagram



7.3.6.11. Command Group Package Length Table

The package length data in Table 44 below should be used to match the overall length of each command signal to its associated clock reference length.

Table 44. Command Group Package Lengths

Signal	Pin Number	Pkg Length (mils)
SMA[0]	AC18	420
SMA[3]	AD17	472
SMA[6]	AD8	591
SMA[7]	AD7	596
SMA[8]	AC6	630
SMA[9]	AC5	681
SMA[10]	AC19	377
SMA[11]	AD5	683
SMA[12]	AB5	609
SBA[0]	AD22	592
SBA[1]	AD20	435
SCAS#	AC24	562
SRAS#	AC21	499
SWE#	AD25	751

7.3.7. CPC Signals – SMA[5,4,2,1], SMAB[5,4,2,1]

The Intel 852GM GMCH chipset control signals, SCKE[3:0] and SCS#[3:0], are common clocked signals. They are "clocked" into the DDR SDRAM devices using clock signals SCK/SCK#[5:0]. The GMCH drives the CPC and clock signals together, with the clocks crossing in the valid control window. The GMCH provides one set of CPC signals per SO-DIMM slot.

Refer to Table 38 for the CKE and CS# signal to SO-DIMM mapping.

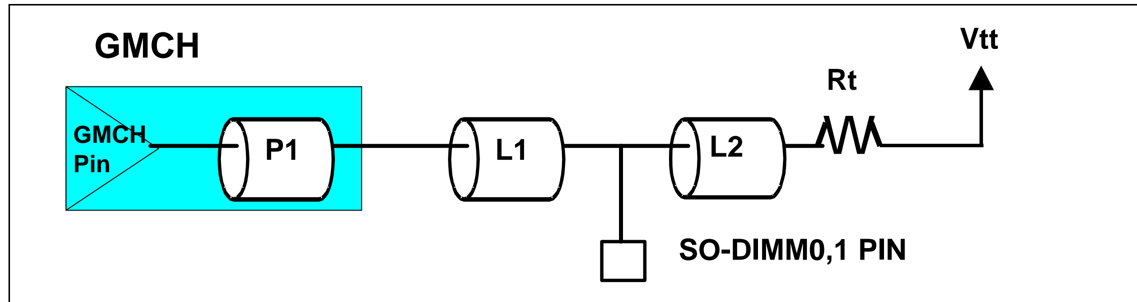
Table 45. CPC Signal to SO-DIMM Mapping

Signal	Relative To	SO-DIMM Pin
SMA[1]	SO-DIMM0	AD14
SMA[2]	SO-DIMM0	AD13
SMA[4]	SO-DIMM0	AD11
SMA[5]	SO-DIMM0	AC13
SMAB[1]	SO-DIMM1	AD16
SMAB[2]	SO-DIMM1	AC12
SMAB[4]	SO-DIMM1	AF11
SMAB[5]	SO-DIMM1	AD10

- The CPC signal routing should transition from an external layer to an internal signal layer under the GMCH.
- Keep to the same internal layer until transitioning back out to an external layer to connect to the appropriate pad of the SO-DIMM connector and the parallel termination resistor.
- If the layout requires additional routing before the termination resistor, return to the same internal layer and transition back out to an external layer immediately prior to parallel termination resistor.
- External trace lengths should be minimized. Intel suggests that the parallel termination be placed on both sides of the board to simplify routing and minimize trace lengths.
- All internal and external signals should be ground reference to keep the path of return current continuous. Intel suggests that all control signals be routed on the same internal layer.
- Resistor packs are acceptable for the parallel (Rt) control termination resistors, but control signals can't be placed within the same R pack as the data or command signals. Figure 60 and Table 46 below depict the recommended topology and layout routing guidelines for the DDR-SDRAM control signals.

7.3.7.1. CPC Signal Topology

Figure 60. Command per Clock Signal Routing Topology



The CPC signals should be routed using 2 to 1 trace space to width ratio for signals within the DDR group, except clocks and strobes. There should be a minimum of 20-mils of spacing to non-DDR related signals. CPC signals should be routed on inner layers with minimized external trace lengths.

7.3.7.2. CPC Signal Routing Guidelines

Table 46. CPC Signal Routing Guidelines

Parameter	Routing Guidelines
Signal Group	SMA[5,4,2,1], SMAB[5,4,2,1]
Motherboard Topology	Point-to-Point with Parallel Termination
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Zo)	55 Ω ±15%
Nominal Trace Width	Inner layers: 4 mils Outer layers: 5 mils
Minimum Spacing to Trace Width Ratio	2 to 1 (e.g. 8 mil space to 4 mil trace)
Minimum Isolation Spacing to non-DDR Signals	20 mils
Package Length P1	500 mils ± 250 mils (See Table 47 for exact package lengths.)
Trace Length L1 – GMCH Control Signal Ball to SO-DIMM Pad	Min = 0.5 inches Max = 5.5 inches
Trace Length L2 – SO-DIMM Pad to Parallel Termination Resistor Pad	Max = 2.0 inches
Parallel Termination Resistor (Rt)	56 Ω ± 5%
Maximum Recommended Motherboard Via Count Per Signal	3
Length Matching Requirements	CPC to SCK/SCK# [4,3,1,0] See length matching Section 7.3.7.3 and Figure 61 for details.

NOTES:
1. Recommended resistor values and trace lengths may change in a later revision of the design guide.
2. Power distribution vias from Rt to Vtt are not included in this count.

3. It is possible to route using 2 vias if one via is shared that connects to the SO-DIMM pad and parallel termination resistor.
4. The overall maximum and minimum length to the SO-DIMM must comply with clock length matching requirements.

7.3.7.3. CPC to Clock Length Matching Requirements

The total length of the CPC signals, between the GMCH die pad and the SO-DIMM must fall within the range defined below, with respect to the associated clock reference length. Refer to Figure 60 for a definition of the various trace segments. The length the trace from the SO-DIMM to the termination resistor need not be length matched. The length matching requirements are also depicted in Figure 61. Refer to Section 7.1 for more details on length matching requirements. A table of CPC signal package length is provided in Section 7.3.7.4.

Length range formula for SO-DIMM0:

X_0 = SCK/SCLK#[1:0] total reference length, including package length. See clock 7.3.1

Y_0 = SMA[5,4,2,1] total length = GMCH package + L1, as shown in Figure 60,

where: $(X_0 – 1.0”) \le Y_0 \le (X_0 + 0.5”)$

Length range formula for SO-DIMM1:

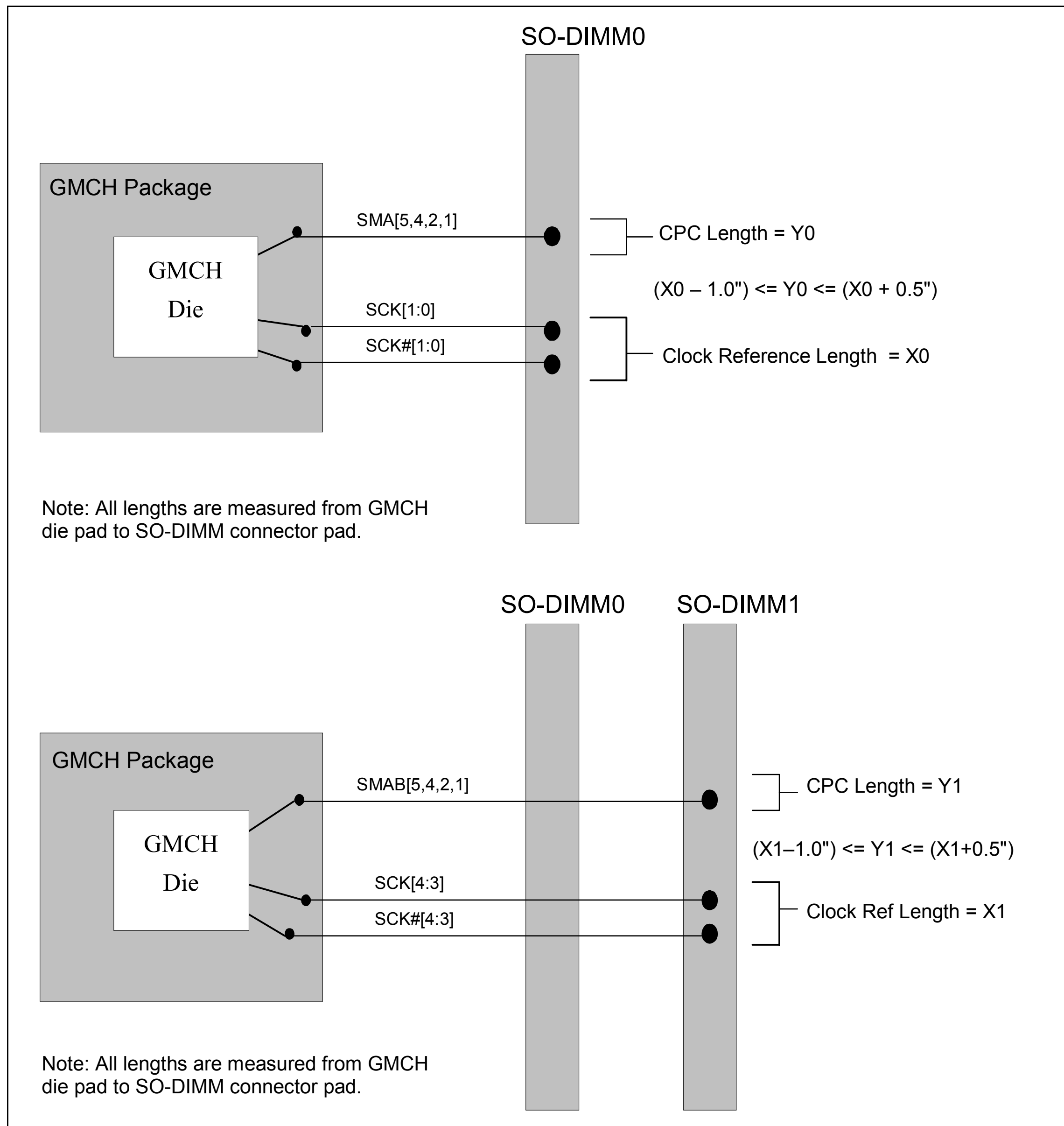
X_1 = SCK/SCLK#[4:3] total reference length, including package length. See clock 7.3.1.

Y_1 = SMAB[5,4,2,1] total length = GMCH package + L1, as shown in Figure 60,

where: $(X_1 – 1.0”) \le Y_1 \le (X_1 + 0.5”)$

No length matching is required from SO-DIMM1 to the termination resistor. Figure 61 on the following page depicts the length matching requirements between the CPC signals and clock. A nominal CPC package length of 500 mils can be used to estimate baseline MB lengths. Refer to Section 7.2 for more details on package length compensation.

Figure 61. CPC Signals to Clock Length Matching Diagram



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7.3.7.4. CPC Group Package Length Table

The package length data in the table below should be used to match the overall length of each CPC signal to its associated clock reference length.

Table 47. CPC Group Package Lengths

Signal	Pin Number	Pkg Length (mils)
SMA[1]	AD14	398
SMA[2]	AD13	443
SMA[4]	AD11	430
SMA[5]	AC13	346
SMAB[1]	AD16	427
SMAB[2]	AC12	395
SMAB[4]	AF11	716
SMAB[5]	AD10	631

7.3.8. Feedback – RCVENOUT#, RCVENIN#

The Intel 852GM GMCH provides a feedback signal called "receive enable" (RCVEN#), which is used to measure timing for the read data.

In the Intel 852GM GMCH implementation of the GMCH the RCVENOUT# signal is shunted directly to RCVENIN# inside the package in order to reduce timing variance. With this change it is no longer necessary to provide an external connection. However, it is recommended that both signals be transitioned to the bottom side with vias located adjacent to the package ball in order to facilitate probing.

7.4. System Memory Compensation

See Section 12.5.3.3 for details.

7.5. SMVREF Generation

See Section 12.5.3.2 for details.

7.6. DDR Power Delivery

See Section 12.5 for details.

7.7. External Thermal Sensor Based Throttling (ETS#)

The Intel 852GM chipset GMCH's ETS# input pin is an active low input that can be used with an external thermal sensor to monitor the temperature of the DDR SO-DIMMs for a possible thermal condition. Assertion of ETS# will result in the limiting of DRAM bandwidth on the DDR memory interface to reduce the temperature in the vicinity of the system memory.

By default, the functionality and input buffer associated with ETS# are disabled. Also, the GMCH can be programmed to send an SERR, SCI, or SMI message to the ICH4-M upon the assertion of this signal. External thermal sensors that are suitable for the purpose described above would need to have a small form factor and be able to accurately monitor the ambient temperature in the vicinity of the DDR system memory.

Intel is currently in the process of enabling this feature on the Intel 852GM GMCH and is actively engaging with thermal sensor vendors to ensure compatibility and suitability of vendors' products with the ETS# pin. This includes electrical design guidelines for the ETS# pin and usage/placement guidelines of the thermal sensors for maximum effectiveness. Current third party vendor product offerings that may be suitable for the ETS# pin application include ambient temperature thermal sensors and remote diode thermal sensors. Also, thermal sensors that implement an open-drain output for signaling a thermal event would provide the most flexibility from an electrical and for layout design perspective.

The design guidelines for ETS# and external thermal sensor placement below are considered preliminary and subject to change in future revisions of this design guide. Please contact your local FAE for any updates.

7.7.1. ETS# Usage Model

The thermal sensors targeted for this application with the GMCH's ETS# are planned to be capable of measuring the ambient temperature only and should be able to assert ETS# if the preprogrammed thermal limits/conditions are met or exceeded. Because many variables within a mobile system can affect the temperature measured at any given point in a system, the expected usage and effectiveness of ETS# is also very focused. Because of factors such as thermal sensor placement, airflow within a mobile chassis, adjacent components, thermal sensor sensitivity, and thermal sensor response time, ETS# can effectively be used for controlling skin temperatures. However, ETS# should not be used for measuring or controlling the Tj or Tcase parameters of DDR-SDRAM devices since due to the location of the thermal sensor it cannot respond quickly enough to dynamic changes in DRAM power.

7.7.2. ETS# Design Guidelines

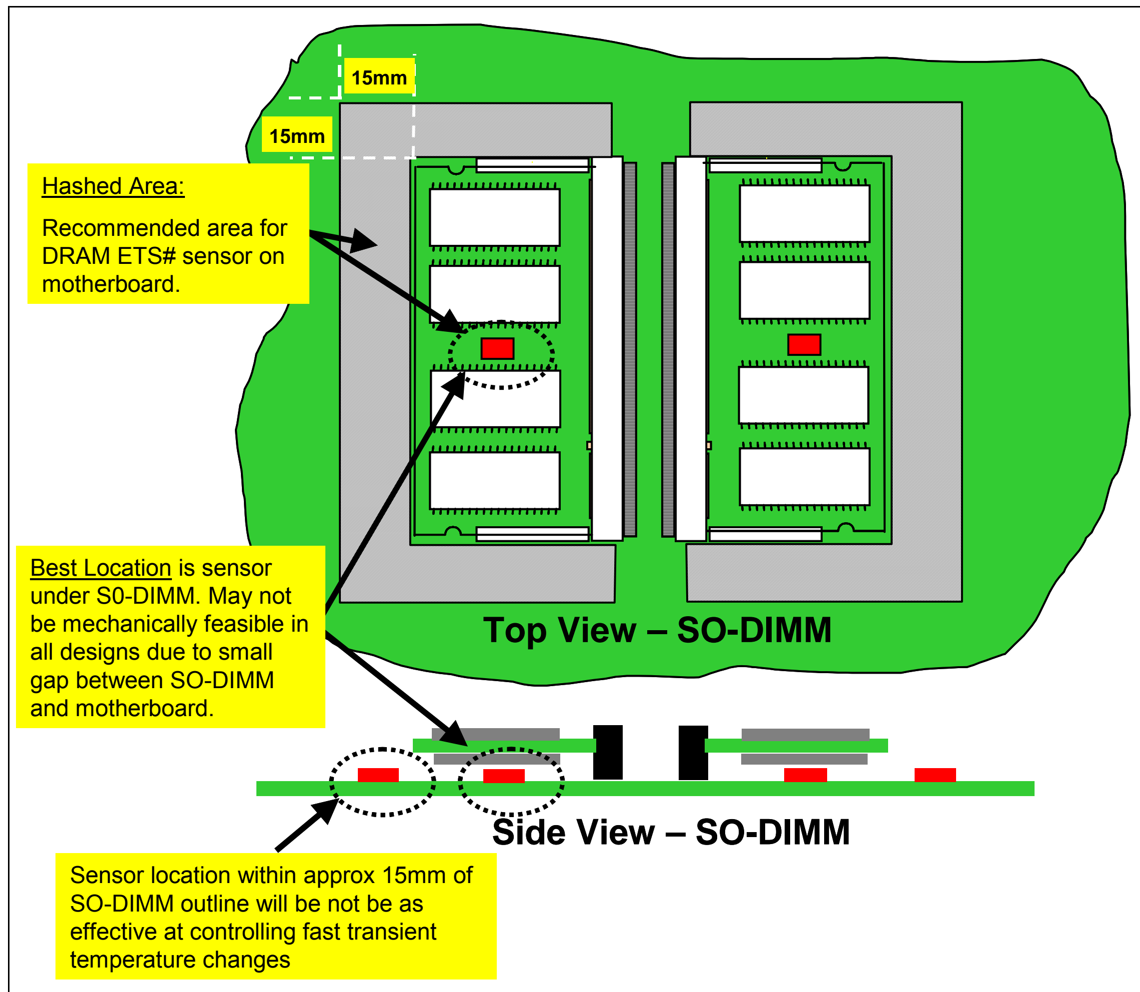
ETS#, as implemented in the GMCH, is an active low signal and does **not** have an integrated pull-up to maintain a logic 1. As a result of this, a placeholder for an external 8.2 kΩ to 10 kΩ pull-up resistor should be provided near the ETS# pin. Electrical details on output characteristics of suitable thermal sensors for use with the GMCH are currently not finalized. The currently recommended pull-up voltage for this external pull-up should be 3.3 V. The thermal sensor should implement an open drain type output buffer to drive ETS#. A system is expected to have one thermal sensor per SO-DIMM connector on the motherboard. As a result, routing guidelines for the output of these thermal sensors to the ETS# pin will also be important.

7.7.3. Thermal Sensor Placement Guidelines

The many factors that can affect the accuracy of ambient temperature measurements by thermal sensors make the placement of them a very critical and especially challenging task. Ideally, one thermal sensor should be placed near each SO-DIMM in a system. The thermal sensor should be located in an area where the effects of airflow and effects of conduction from adjacent components are minimized. This allows for the best correlation of thermal sensor temperature to chassis or notebook surface temperature. See Figure 62 for details.

Assuming airflow is negligible within a system, the optimal placement of the thermal sensor is on the surface of the motherboard directly beneath the shadow of an SO-DIMM module centered longitudinally and laterally in relation to the outline of the SO-DIMM. The thermal sensor should have a form factor small enough to allow it to fit beneath double-sided memory modules (i.e. modules with memory devices on both sides of a module). If placement within the outline of an SO-DIMM is not possible, then the next best option is to locate it within approximately 15 mm (0.6 inches) of the outline/SO-DIMM shadow. Again, this assumes negligible effects from airflow.

Figure 62. DDR Memory Thermal Sensor Placement



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8. Integrated Graphics Display Port

The GMCH contains four display ports: an analog CRT port, a dedicated LVDS port, and one 12-bit Digital Video Out (DVO) port. Section 8.1 will discuss the CRT and RAMDAC routing requirements. Section 8.2 will discuss the dedicated LVDS port. Section 8.3 will discuss DVOC design guideline. Section 8.4 provides recommendations for the GPIO signal group.

8.1. Analog RGB/CRT Guidelines

8.1.1. RAMDAC/Display Interface

The GMCH integrated graphics/chipset design interfaces to an analog display via a RAMDAC. The RAMDAC is a subsection of the graphics controller display engine and consists of three identical 8-bit digital-to-analog converter (DAC) channels, one for the display's red, green, and blue electron guns.

Each RGB output is doubly terminated with a 75-Ω resistance: One 75-Ω resistance is connected from the DAC output to the board ground, and the other termination resistance exists within the display. The equivalent DC resistance at the output of each DAC is 37.5 Ω. The current output from each DAC flows into this equivalent resistive load to produce a video voltage, without the need for external buffering. There is also an LC pi-filter on each channel that is used to reduce high-frequency noise and to reduce EMI. In order to maximize the performance, the filter impedance, cable impedance, and load impedance should be matched.

Since the DAC runs at speeds up to 350 MHz, special attention should be paid to signal integrity and EMI. RGB routing, component placement, component selection, cable and load impedance (monitor) all play a large role in the analog display's quality and robustness. This holds true for all resolutions, but especially for those at 1600x1200 resolutions or higher.

8.1.2. Reference Resistor (REFSET)

A reference resistor, Rset, is used to set the reference current for the DAC. This resistor is an external resistor with a 1% tolerance that is placed on the circuit board. A reference resistor can be selected from a range between 124 Ω to 137 Ω (1%). The Intel Customer Reference Board uses the value 127 Ω (1%). Based on board design, DAC RGB outputs may be measured when the display is completely white. If the RGB voltage value is between 665 mV to 770 mV, then the video level is within VESA specification and the resistor value that was chosen will be optimal for board design. See Figure 65 for the recommended Rset placement.

A reference voltage is generated on the GMCH from a bandgap voltage reference circuit. The bandgap reference voltage level is approximately 1.2 V and this voltage is divided by four to generate the reference voltage. The VESA video standard defines the LSB current for each DAC channel. The RAMDAC reference current is designed on-die to be equal to 32LSB.

8.1.3. RAMDAC Board Design Guidelines

In order for the RAMDAC to successfully run at speeds up to 350 MHz, care should be taken when routing the analog RAMDAC signals. Intel recommends that each analog R, G, B signal be routed single-endedly. The analog RGB signals should be routed with an impedance of 37.5 Ω. Intel recommends that these routes be routed on an inner routing layer and that it be shielded with VSS planes, if possible. Spacing between R, G, and B channels and to other signals should be maximized; 20-mil spacing is recommended. The RGB signals require pi filters that should be placed near the VGA connector. It consists of two 3.3-pF caps with a 75 Ω at 100-MHz FB between them. The RGB signals should have a 75-Ω, 1% terminating pull-down resistor. The complement signals (R#, G#, and B#) should be grounded to the ground plane.

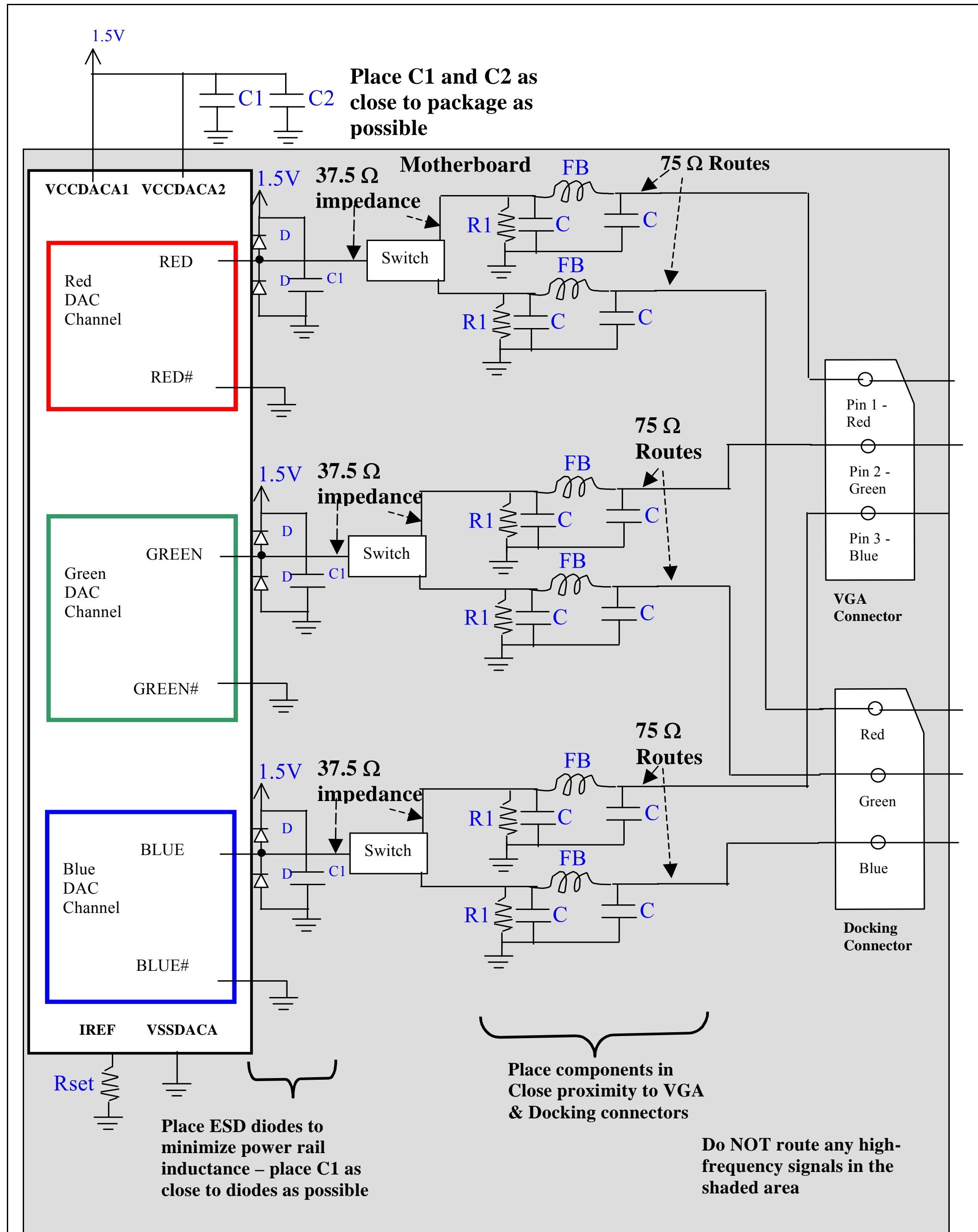
Intel recommends that the pi filter and terminating resistors be placed as close as possible to the VGA connector. After the 75-Ohm termination resistor, the RGB signals should continue on to their pi filters and the VGA connector, *but should now ideally be routed with a 75-Ohm impedance (~ 5 mil traces).*

The RGB signals also require protection diodes between 1.5 V and ground. These diodes should have low C ratings (~5 pF max) and small leakage current (~ 10 µA at 120˚C) and should be properly decoupled with a 0.1-µF cap. These diodes and decoupling should be placed to minimize power rail inductance. The choice between diodes (or diode packs) should comprehend the recommended electrical characteristics in addition to cost.

The RGB signals should be length matched as closely as possible (from the Intel 852GM GMCH to VGA connector) and should not exceed 200 mils of mismatch.

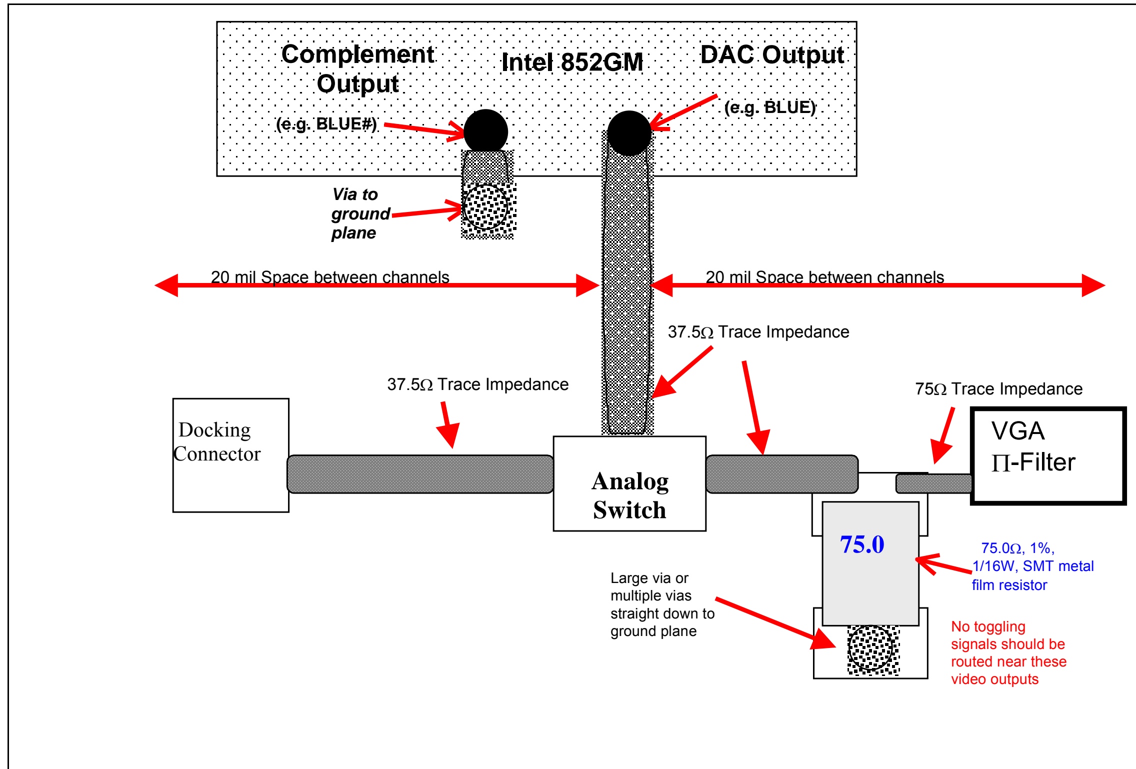
8.1.4. RAMDAC Routing Guidelines

Figure 63. GMCH RAMDAC Routing Guidelines with Docking Connector



The RAMDAC channel (red, green, blue) outputs are routed as single-ended (with 37.5 ohm trace impedance) shielded current output routes that are terminated prior to connecting to the video PI-filter and VGA/docking connector.

Figure 64. RAMDAC Routing w/ Resistor and Analog Switch Layout Example for Docking Connector



NOTES:

1. The routing to the docking connector is not shown in this figure; however, this routing scheme applies to the docking connector as well.
2. The analog switch should meet the following characteristics of C < 10pf and Ron~5ohms in order to meet VESA analog specifications Actual value will vary depending on routing topology.

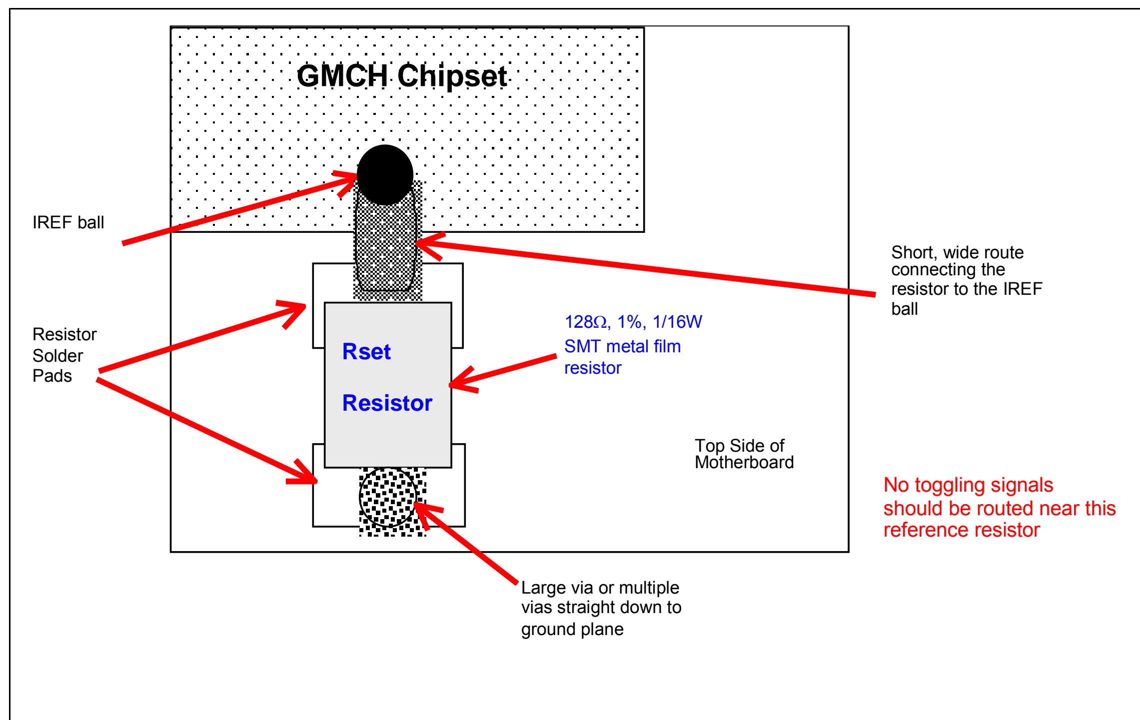
The recommended routing of the termination resistors is shown in Figure 64.

Table 48. Recommended GMCH RAMDAC Components

Recommended DAC Board Components				
Component	**Value**	**Tolerance**	**Power**	**Type**
R1	75.0 Ω	1%	1/16 W	SMT, Metal Film
Rset	128.0 Ω	1%	1/16 W	SMT, Metal Film
C1	0.1 µF	20%	-----	SMT, Ceramic
C2	0.01 µF	20%	-----	SMT, Ceramic
C	3.3 pF	10%	-----	SMT, Ceramic
D	PAC DN006	-------	350 mW	California Micro Devices – ESD diodes for VGA SOIC package or equivalent diode array
FB	75 Ω @ 100 MHz	--------	-------	MuRata* BLM11B750S

Figure 65 shows the recommended Rset placement.

Figure 65. Rset Resistor Placement



8.1.5. DAC Power Requirements

The DAC requires a 1.5-V supply through its two VCCADAC balls. The two may share a set of capacitors, 0.1 µF and 0.01 µF, but this connection should have low inductance. Separate analog power or ground planes are not required for the DAC.

However, since the DAC is an analog circuit, it is particularly sensitive to AC noise seen on its power rail. Designs should provide as clean and quiet a supply as possible to the VCCA_DAC. Additional

filtering and/or separate voltage rail may be needed to do so. On the Intel CRB, there is a place holder for a LC filter in case there is noise present in the VCCA power rail.

Video DAC Power Supply DC Specification: 1.50 V ± 5%
Video DAC Power Supply AC Specification:
+/- 0.3% from 0.10 Hz to 10 MHz
+/- 0.95% from 10 MHz to max pixel clock frequency

Absolute minimum voltage at the VCCA package ball = 1.40 V

Please contact your Intel Field Representative for latest AC/DC specification.

8.1.6. HSYNC and VSYNC Design Considerations

HSYNC and VSYNC signals are connected to the analog display attached to the VGA connector. These are 3.3-V outputs from the GMCH. A 39 ohm series resistor is required before routing to the VGA connector. Capacitors before and after the series resistor may be needed to meet the VESA VGA connector over/undershoot specification. Please refer to Chapter 13 and 14 for for details on Intel costomer reference board implementation. Unidirectional buffers (high impedance buffers) are required when routing to the CRT connector to prevent potential electrical overstress and illegal operation of the GMCH, since some display monitors may attempt to drive HSYNC and VSYNC signals back to GMCH.

8.1.7. DDC and I2C Design Considerations

DDCADATA and DDCACLK are 3.3-V IO buffers connecting the GMCH to the monitor. To avoid potential electrical overstress on these signals, bi-directional level-shifting devices are required. These signals require 2.2-kΩ pull-ups (or pull-ups with the appropriate value derived from simulation) on each of these signals. See Section 8.4 for further pullup recommendations for the DDC (GPIO) signal group.

8.2. LVDS Transmitter Interface

The Intel LVDS (Low Voltage Differential Signaling) Transmitter serializer converts up to 24 bits of parallel digital RGB data, (8 bits per RGB), along with up to 4 bits for control (SHFCLK, HSYNC, VSYNC, DE) into 2, 4 channel serial bit streams, for output by the LVDS transmitter.

The transmitter is fully differential and utilizes a current mode drive with a high impedance output. The drive current develops a differential swing in the range of 250 mV to 450 mV across a 100-Ohm termination load.

The parallel digital data is serially converted to a 7-bit serial bit stream that is transmitted over the 8 channel LVDS interface at 7x the input clock. The differential output clock channel transmits the output clock at the input clock frequency. While the differential output channels transmit the data at the 7x clock rate (1 bit time is 7x the input clock). The 7x serializer will synchronize and regenerate and input clock from 35 MHz to 112 MHz. Typical operation is at 65 MHz (15.4 ns), therefore, at a 7x clock rate, 1-bit time would be 2.2 ns. With data cycle times as small as 2.2 ns, propagation delay mismatch is critical, such that intra-channel skew (skew between the inverting and non-inverting output) must be kept minimal.

The following differential signal groups comprise the LVDS Interface. The topology rules for each group are defined in subsequent sections.

Table 49. Signal Group and Signal Pair Names

Channel	Signal Group	Signal Pair Names
Channel A	Clocks	ICLKAM, ICLKAP
	Data Bus	IYAM[3:0], IYAP[3:0]
Channel B	Clocks	ICLKBM, ICLKBP
	Data Bus	IYBM[3:0], IYBP[3:0]

8.2.1. Length Matching Constraints

The routing guidelines presented in the following subsections define the recommended routing topologies, trace width and spacing geometries, and absolute minimum and maximum routed lengths for each signal group. These recommendations are provided to achieve optimal SI and timing. In addition to the absolute length limits provided, more restrictive length matching requirements are also provided. The additional requirements further restrict the minimum to maximum length range of each signal group with respect to clock strobe, within the overall boundaries defined in the guideline tables, as required to guarantee adequate timing margins. These secondary constraints are referred to as length matching constraints. The amount of minimum to maximum length variance allowed for each group around the clock strobe reference length varies from signal group to signal group depending on the amount of timing variation that can be tolerated. Refer to Table 50 for LVDS length matching requirements.

Each LVDS channel is length matched to the LVDS strobe signals. The strobes on a given channel are matched to within ± 25 mils of the target length.

Table 50. LVDS Signal Trace Length Matching Requirements

Signal Group	Data pair	Signal Matching	Clock Strobes associated With the Channel	Strobe Matching
CHANNEL A	IYAM0, IYAP0	± 20 mils	ICLKAM, ICLKAP	± 25 mils
	IYAM1, IYAP1	± 20 mils		
	IYAM2, IYAP2	± 20 mils		
	IYAM3, IYAP3	± 20 mils		
CHANNEL B	IYBM0, IYBP0	± 20 mils	ICLKAM, ICLKAP	± 25 mils
	IYBM1, IYBP1	± 20 mils		
	IYBM2, IYBP2	± 20 mils		
	IYBM3, IYBP3	± 20 mils		

NOTE: All length matching formulas are based on GMCH die-pad to LVDS connector pin total length. Package length tables are provided for all signals in order to facilitate this pad to pin matching.

8.2.1.1. Package Length Compensation

As mentioned in Section 8.2.1, all length matching is done from GMCH die-pad to LVDS connector pin. The reason for this is to compensate for the package length variation across each signal group in order to minimize timing variance. The GMCH does not equalize package lengths internally as some previous GMCH components have, and therefore, the GMCH requires a length matching process. See Table 52 for the Intel 852GM LVDS package lengths information.

Package length compensation should not be confused with length matching as discussed in the previous section. Length matching refers to constraints on the minimum and maximum length bounds of a signal group based on clock length, whereas package length compensation refers to the process of adjusting out package length variance across a signal group. There is of course some overlap in that both affect the target length of an individual signal. Intel recommends that the initial route be completed based on the length matching formulas in conjunction with nominal package lengths and that package length compensation is performed as a secondary operation.

8.2.2. LVDS Routing Guidelines

Table 51. LVDS Signal Group Routing Guidelines

Parameter	Definition
Signal Group	LVDS
Topology	Differential Pair Point to Point
Reference Plane	Ground Referenced
Differential Mode Impedance (Zdiff)	100 ohms ± 15%
Nominal Trace Width	4 mils
Nominal Pair Spacing (edge to edge)	7 mils
Minimum Pair to Pair Spacing (see exceptions for breakout region below)	20 mils
Minimum Serpentine Spacing	20 mils
Minimum Spacing to Other LVDS Signals (see exceptions for breakout region below)	20 mils
Minimum Isolation Spacing to non-LVDS Signals	20 mils
Maximum Via Count	2 (per line)
Package Length Range – P1	550 mils ± 150mils (see LVDS package length Table 52 for exact lengths)
Total Length –	Max 10"
Clock Length Matching	Match all segments to ± 20 mils (see Section 8.2.1)
Clock to Clock Length Matching (Total Length)	Match clocks to X0 ± 20 mils
Breakout Exceptions (Reduced geometries for GMCH breakout region)	Breakout section should be as shorter as possible. Try to maintain trace width as 4 mils, spacing 7 mils, while the spacing between pairs can be 10-20 mils.

The traces associated with the LVDS Transmitter timing domain signals are differential traces terminated across 100 ohms ± 15 % and should be routed as:

- Strip-line only.
- Isolate all other signals from the LVDS signals to prevent coupling from other sources onto the LVDS lines.
- Use controlled impedance traces that match the differential impedance of your transmission medium (i.e. cable) and termination resistor
- Run the differential pair trace lines as close together as possible as soon as they leave the IC, not greater than 10 mils. This will help eliminate reflections and ensure noise is coupled as common mode. Plus, noise induced on the differential lines is much more likely to appear as common mode, which is rejected by the receiver.
- The LVDS Transmitter timing domain signals have a maximum trace length of 10.0 inches. This maximum applies to all of the LVDS Transmitter signals.
- Traces must be ground referenced and must not switch layers between the GMCH and connector.

When choosing cables, it is important to remember:

- Use controlled impedance media. The differential impedance of the LVDS cable uses to connect to the panel should be 100 Ω. Cables should not introduce major impedance discontinuities that cause signal reflection.
- Balanced cables (twisted pair) are usually better than unbalanced cables (ribbon cable, multi-conductor) for noise reduction and signal quality.
- Cable length must be less than 16 inches.

Table 52. LVDS Package Lengths

Signal Group	GMCH Signal Name	Package Trace Length (mils)	Board Length	Total Trace Length
CHANNEL A	ICLKAP	503.7		
	ICLKAM	498.8		
	IYAP0	399.6		
	IYAM0	385.4		
	IYAP1	487.5		
	IYAM1	466.2		
	IYAP2	572.6		
	IYAM2	566.2		
	IYAP3	643.2		
	IYAM3	637.8		
CHANNEL B	ICLKAP	502.0		
	ICLKAM	499.1		
	IYBP0	359.8		
	IYBM0	353.7		

Signal Group	GMCH Signal Name	Package Trace Length (mils)	Board Length	Total Trace Length
	IYBP1	524.7		
	IYBM1	516.6		
	IYBP2	623.3		
	IYBM2	604.2		
	IYBP3	441.8		
	IYBM3	441.7		

8.3. Digital Video Out Port

The GMCH DVO port interface supports a wide variety of third party DVO compliant devices (e.g. TV encoder, TMDS transmitter or integrated TV encoder and TMDS transmitter The Intel 852GM has a single dedicated Digital Video Out Port (DVOC). Intel's DVO port is a 1.5-V only interface that can support transactions up to 165 MHz. Some of the DVO port command signals may require voltage translation circuit depending on the third party device.

8.3.1. DVO Interface Signal Groups

8.3.1.1. DVOC Interface Signals

Input Signals

- DVOCFLDSTL
- DVOBCCLKINT
- DVOBCINTR#
- ADDID[7:0]
- DVODETECT

Output Data Signals

- DVOCHSYNC
- DVOCVSYNC
- DVOCBLANK#
- DVOCD[11:0]

Output Strobe Signals

- DVOCCLK (DVOCCLK[0])
- DVOCCLK# (DVOCCLK[1])

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Voltage References, PLL Power Signals

- DVORCOMP
- GVREF

8.3.2. DVO Port Interface Routing Guidelines

8.3.2.1. Length Mismatch Requirements

The routing guidelines presented in the following subsections define the recommended routing topologies, trace width and spacing geometries, and absolute minimum and maximum routed lengths for each signal group, which are recommended to achieve optimal SI and timing. In addition to the absolute length limits provided in the individual guideline tables, more restrictive length matching requirements are also provided which further restrict the minimum to maximum length range of each signal group with respect to clock strobe, within the overall boundaries defined in the guideline tables, as required to guarantee adequate timing margins. Refer to Table 53 for DVO length matching requirements.

Table 53. DVO Interface Trace Length Mismatch Requirements

Data Group	Signal Matching to Strobe Clock	DVO Clock Strobes Associated With the Group	Clock Strobe Matching	Notes
DVOCD [11:0]	± 100 mils	DVOCCLK[1:0]	± 10 mils	1,2

NOTES:
1. Data signals of the same group should be trace length matched to the clock within ±100 mil including package lengths.
2. ***All length matching formulas are based on GMCH die-pad to DVO device pin total length.*** Package length table are provided for all signals in order to facilitate this pad to pin matching.

8.3.2.2. Package Length Compensation

As mentioned in Section 8.3.2.1, all length matching is done from GMCH die-pad to DVO connector pin. The reason for this is to compensate for the package length variation across each signal group in order to minimize timing variance. The GMCH does not equalize package lengths internally as some previous GMCH components have, and therefore, the GMCH requires a length matching process. See Table 55 for DVOC package lengths information.

Package length compensation should not be confused with length matching as discussed in the previous section. Length matching refers to constraints on the minimum and maximum length bounds of a signal group based on clock length, whereas package length compensation refers to the process of adjusting out package length variance across a signal group. There is of course some overlap in that both affect the target length of an individual signal. Intel recommends that the initial route be completed based on the length matching formulas in conjunction with nominal package lengths and that package length compensation is performed as a secondary operation.

8.3.2.3. DVO Routing Guidelines

Table 54 provides the DVOC routing guideline summary.

Table 54. DVOC Routing Guideline Summary

Parameter	Definition
Signal Group	DVCBD [11:0]
Motherboard Topology	Point to point
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Zo)	55 Ω ± 15%
Nominal Trace Width	Inner layers: 4 mils
Minimum Spacing to Trace Width Ratio	2 to 1 (e.g. 8 mil space to 4 mil trace)
Minimum Isolation Spacing to non-DVO Signals	20 mils
Minimum Spacing to Other DVO Signals	12 mils (see exceptions for breakout region below)
Minimum Spacing of DVOCCLK [1:0] to any other signals	12 mils
Package Length Range – P1	See Table 55 for package lengths.
Total Length –	Max 6”
Data to Clock Strobe Length Matching Requirements	± 100 mils (See Table 53 for length matching requirements)
CLK0 to CLK1 Length Matching Requirements	± 10 mils (See Table 53 for length matching requirements.)

Refer to Table for GMCH DVOC package lengths.

- All signals should be routed as striplines (inner layers).
- All signals in a signal group should be routed on the same layer. Routing studies have shown that these guidelines can be met. The trace length and trace spacing requirements ***must*** not be violated by any signal.
- Route the DVOCCLK[1:0] signal pairs 4 mils wide and 8 mils apart (2:1) with a max trace length of 6 inches. This signal pair should be a minimum of 12 mils from any adjacent signals.
- In order to break out of the Intel 852GM GMCH, the DVOC data signals can be routed with a trace width of 4 mils and a trace spacing of 7 mils. The signals should be separated to a trace width of 4 mils and a trace spacing of 8 mils within 0.3 inches of the GMCH component.

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Table 55. DVOC Interface Package Lengths

Signal	Pin Number	Package Length (mils) P1
DVOCBLANK#	L3	541
DVOCCLK	J3	601
DVOCCLK#	J2	675
DVOCD[0]	K5	489
DVOCD[1]	K1	692
DVOCD[2]	K3	622
DVOCD[3]	K2	685
DVOCD[4]	J6	536
DVOCD[5]	J5	518
DVOCD[6]	H2	720
DVOCD[7]	H1	771
DVOCD[8]	H3	649
DVOCD[9]	H4	625
DVOCD[10]	H6	521
DVOCD[11]	G3	762
DVOCFLDSTL	H5	566
DVOCHSYNC	K6	491
DVOCVSYNC	L5	440

8.3.2.4. DVO Port Termination

The DVO interface does not require external termination.

8.4. DVO GMBUS and DDC Interface Considerations

The GMCH DVOC port controls the video front-end devices via the GMBUS (I2C) interface. DDCADATA and DDCACLK should be connected to the CRT connector. The GMBUS should be connected to the DVO device, as required by the specifications for those devices. The protocol and bus may be used to configure registers in the TV encoder, TMDS transmitter, or any other external DVI device. The GMCH also has an option to utilize the DDCPCLK and DDCPDATA to collect EDID (Extended Display Identification) from a digital display panel.

Pull-ups (or pull-ups with the appropriate value derived from simulating the signal) typically ranging from 2.2 kΩ to 10 kΩ are required on each of these signals.

The following GMCH signal groups list the six possible GMBUS pairs.

Table 56. GMBUS Pair Mapping and Options

Pair #	Signal Name	Buffer Type	Description	Notes
0	DDCADATA	3.3 V	DDC for Analog monitor (CRT) connection.	This cannot be shared with other DDC or I2C pairs due to legacy monitor issues.
	DDCACLK			
1	LCLKCTRLA	3.3 V	For control of SSC clock generator devices down on motherboard.	If SSC is not supported then can be used for DVOC GMBUS.
	LCLKCTRLB			
2	DDCPDATA	3.3 V	DDC for Digital Display connection via the integrated LVDS display port for support for EDID panel.	If EDID panels are not supported. Can optionally use as GMBUS for DVOC.
	DDCPCLK			
3	MDVIDATA	1.5 V	GMBUS control of DVI devices (TMDS or TV encoder)	Can optionally use as GMBUS for DVOC.
	MDVICLK			
4	MI2CDATA	1.5 V	GMBUS control of DVI devices (TMDS or TV encoder)	Can optionally use as GMBUS for DVOC.
	MI2CCLK			
5	MDDCDATA	1.5 V	DDC for Digital Display connection via TMDS device	Can optionally use as GMBUS for DVOC.
	MDDCCLK			

NOTE: All GMBUS pairs can be optionally programmed to support any interface and is programmed through the BMP utility.

If any of GMBUS pairs (expect DDCADATA/DDCCLK for CRT) are not used, 2.2 k – 100 kΩ pull-up (or pull-ups with the appropriate value derived from simulating the signal), resistors are required except for LCLKCTRLA/LCLKCTRLB GMBUS pair. LCLKCTRLA/LCLKCTRLB are used as bootup straps, please refer to Chapter 13 for details on strapping option. This will prevent the DVO interface from confusing noise on these lines for false cycles.

8.4.1. Leaving the DVO Port Unconnected

If the motherboard does not implement any of the possible video devices with the DVO port, please follow the guidelines recommended on the motherboard. DVO Output signals may be left unconnected if they are not used.

Pull-down resistors are required for the following signals if not used:

- DVOCFLDSTL
- DVOBCCLKINT

Pull-up resistors are required for the following signals if not used:

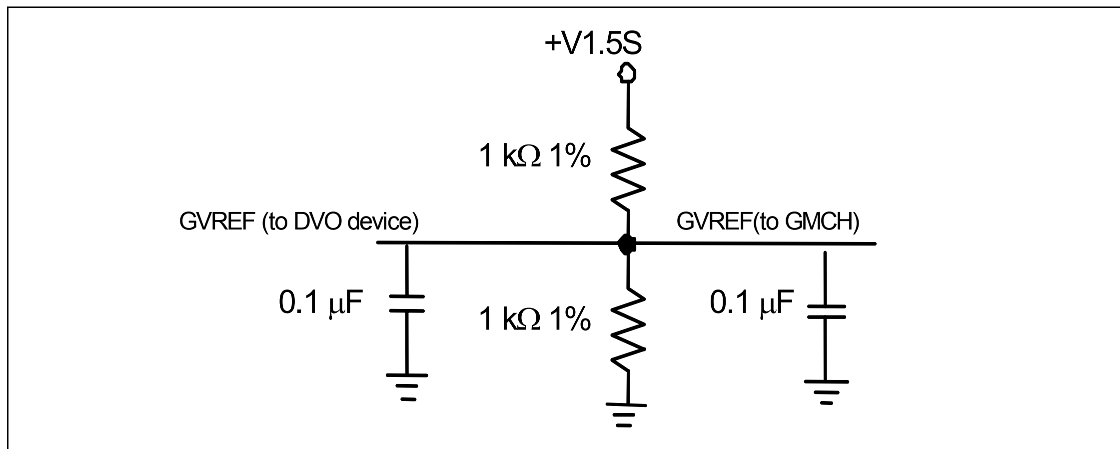
- DVOBCINTR#

8.5. Miscellaneous Input Signals and Voltage Reference

- ADDID[7]: Pulldown to ground with a 1 kΩ resistor when using the DVOC port. This is a vBIOS strapping option to load the TPV AIM module for DVOC port. Pulldown not required DVOC is not enabled.
- ADDID[6:0]: Leave unconnected (NC).

- DVODETECT: Leave unconnected (NC) when using the DOVC port.
- AGPBUSY#: Connect directly to ICH4-M. A 10-k, pullup resistor is required.
- DVORCOMP is used to calibrate the DVO buffers. It should be connected to ground via a 40.2-Ω, 1% resistor using a routing guideline of 10-mil trace and 20-mil spacing.
- DPMS: connects to 1.5 V-version of the ICH4-M's SUSCLK or a clock that runs during S1.
- GVREF: Reference voltage for the DVOC input buffers. Refer to the figure below for proper signal conditioning.

Figure 66. GVREF Reference Voltage



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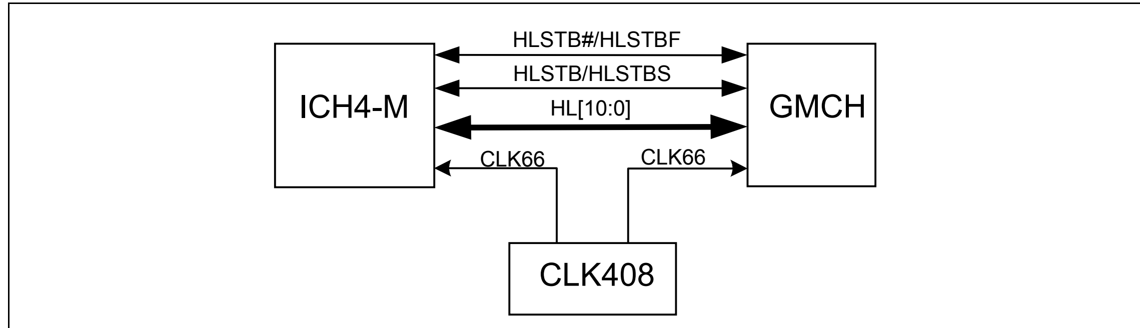
9. Hub Interface

The GMCH and ICH4-M pin-map assignments have been optimized to simplify the hub interface routing between these devices. It is recommended that the hub interface signals be routed directly from the GMCH to the ICH4-M with all signals referenced to VSS. Layer transitions should be kept to a minimum. If a layer change is required, use only two vias per net and keep all data signals and associated strobe signals on the same layer.

The hub interface signals are broken into two groups: data signals (HL) and strobe signals (HLSTB). For the 11-bit hub interface, HL[10:0] are associated with the data signals while HLSTB/HLSTBS and HLSTB#/HLSTBF are associated with the strobe signals.

Figure 67. Hub Interface Routing Example



9.1. Hub Interface Compensation

This section documents the routing guidelines for the 11-bit Hub Interface using enhanced (parallel) termination (the method of termination is dependant upon the processor). This Hub Interface connects the ICH4-M to the GMCH. The ICH4-M should strap its HLRCOMP pin to V_{CC}=1.5 V, as summarized in Table 57. The GMCH should strap its HLRCOMP pin to V_{CC}=1.2 V, as summarized in Table 57.

The trace impedance must equal 55 Ω ± 15%.

Table 57. Hub Interface RCOMP Resistor Values

Component	Trace Impedance	HLCOMP Resistor Value	HLCOMP Resistor Tied to
ICH4-M	55 Ω ± 15%	48.7 Ω ± 1%	Vcc1_5
GMCH	55 Ω ± 15%	27.4 Ω ± 1%	Vcc1_2

9.2. Hub Interface Data HL[10:0] and Strobe Signals

The Hub interface HL[10:0] data signals should be routed on the same layer as Hub interface strobe signals.

9.2.1. HL[10:0] and Strobe Signals Internal Layer Routing

Traces should be routed 4 mils wide with 8 mils trace spacing (4 on 8) and 20 mils spacing from other signals. In order to break out of the GMCH and ICH4-M packages, the HL[10:0] signals can be routed 4 on 7. The signal must be separated to 4 on 8 within 300 mils from the package.

The maximum HL[10:0] signal trace length is 6 inches. The HL[10:0] signals must be matched within ± 100 mils of the HLSTB differential pair. There is no explicit matching requirement between the individual HL[10:0] signals.

The hub interface strobe signals HLSTB and HLSTB# should be routed as a differential pair, 4 mils wide with 8 mils trace spacing (4 on 8). The maximum length for strobe signals is 6 inches. Each strobe signal must be the same length and each HL[10:0] signal must be matched to within ± 100 mils of the strobe signals. All length matching should be done from the Intel 852GM die to the ICH4-M die. Refer to the package length Table 59 and Table 60.

Table 58. Hub Interface Signals Internal Layer Routing Summary

Signal	Max length (inch)	Width (mils)	Space (mils)	Mismatch length (mils)	Relative To	Space with other signals (mils)	Notes
HL[10:0]	6”	4	8	± 100	Differential HSTB pair	20	
HLSTB HLSTB#	6”	4	8	± 100	Data lines	20	HLSTB and HLSTB# must be ± 10 mils of each other.

Table 59. Hub Interface Package Lengths for ICH4-M

Signal	Pin Number	Package Length (mils)
HUB_PD0	L19	551
HUB_PD1	L20	562
HUB_PD2	M19	552
HUB_PD3	M21	567
HUB_PD4	P19	599
HUB_PD5	R19	627
HUB_PD6	T20	623
HUB_PD7	R20	593
HUB_PD8	P23	668
HUB_PD9	L22	559
HUB_PD10	N22	682
HUB_PD11	K21	560
HUB_CLK	T21	605
HUB_PSTRB	P21	541
HUB_PSTRB#	N20	565

Table 60. Hub Interface Package Lengths for GMCH

Signal	Pin Number	Package Length (mils)
HL[0]	U7	281
HL[1]	U4	408
HL[2]	U3	476
HL[3]	V3	484
HL[4]	W2	551
HL[5]	W6	355
HL[6]	V6	328
HL[7]	W7	343
HL[8]	T3	499
HL[9]	V5	399
HL[10]	V4	457
GCLKIN	Y3	539
HLSTB	W3	504
HLSTB#	V2	548

9.2.2. Terminating HL[11]

The HL[11] signal exists on the ICH4-M but not the GMCH and is not used on the platform. HL[11] must be pulled down to ground via a 56-Ω resistor.

9.3. Hub VREF/VSWING Generation/Distribution

The Hub interface reference voltage (VREF) is used on both the GMCH (HLVREF) and the ICH4-M (HIREF). The Hub interface also has a reference voltage (VSWING) for the GMCH (PSWING) and the ICH4-M (HI_VSWING), to control voltage swing and impedance strength of the hub interface buffers. The VREF voltage requirements must be set appropriately for proper operation. See Table 61 for the VREF and VSWING voltage specifications. Sections 9.3.1 to 9.3.3 provide details on the different options for VREF and VSWING voltage divider circuitry requirements.

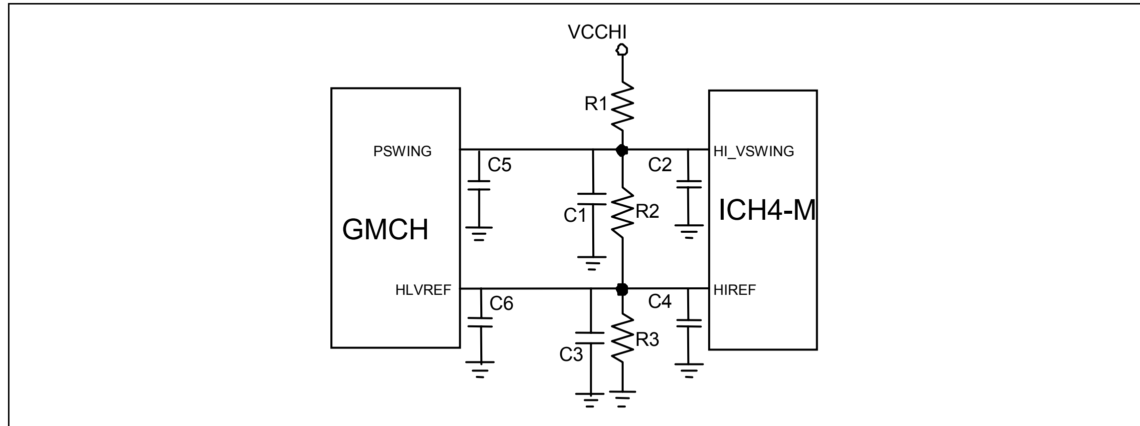
Table 61. Hub Interface VREF/VSWING Reference Voltage Specifications

VREF	VSWING	NOTES
HIREF (ICH4-M) HLVREF (GMCH)	HI_VSWING (ICH4-M) PSWING (GMCH)	
350 mV ± 8%	800 mV ± 8%	See Sections 9.3.1, 9.3.2, and 9.3.3 for recommendations for the VREF/VSWING voltage generation circuitry. See Table 62, Table 63, and Table 64 for recommended resistor values.

9.3.1. Single Generation Voltage Reference Divider Circuit

The GMCH and ICH4-M may share the same single voltage divider circuit. This option provides one voltage divider circuit to generate both VREF and VSWING reference voltage. The reference voltage for both VREF and VSWING must meet the voltage specification in Table 61. If the voltage specifications are not met then individual locally generated voltage divider circuit is required. The maximum trace length from the GMCH to ICH4-M is 4 inches or less. The voltage divider circuit should be place midway between the GMCH and ICH4-M. Normal care needs to be taken to minimize crosstalk to other signals (< 10-15 mV). If the trace length exceeds 4 inches then the locally generated voltage reference divider should be used. See Section 9.3.2 for the more details.

Figure 68. Single VREF/VSWING Voltage Generation Circuit for Hub Interface



The resistor values, R1, R2, and R3 must be rated at 1% tolerance. See Table 62 for recommended resistor value. The selected resistor values ensure that the reference voltage tolerance is maintained over the input leakage specification. Two 0.1-µF capacitors (C1 and C3) should be placed close to the divider. In addition, the 0.01-µF bypass capacitor (C2, C4, C5, and C6) should be placed within 0.25 inches of HLVREF/VREF pin (for C4 and C6) and HI_VSWING pin (for C2 and C5).

Table 62. Recommended Resistor Values for Single VREF/VSWING Divider Circuit

	Recommended Resistor Values			VCCHI
Option 1	R1 = 80.6 Ω ± 1%	R2 = 51.1 Ω ± 1%	R3 = 40.2 Ω ± 1%	1.5 V
Option 2	R1 = 255 Ω ± 1%	R2 = 162 Ω ± 1%	R3 = 127 Ω ± 1%	1.5 V
Option 3	R1 = 226 Ω ± 1%	R2 = 147 Ω ± 1%	R3 = 113 Ω ± 1%	1.5 V
	C1 and C3 = 0.1 µF (near divider) C2, C4, C5, C6 = 0.01 µF (near component)			

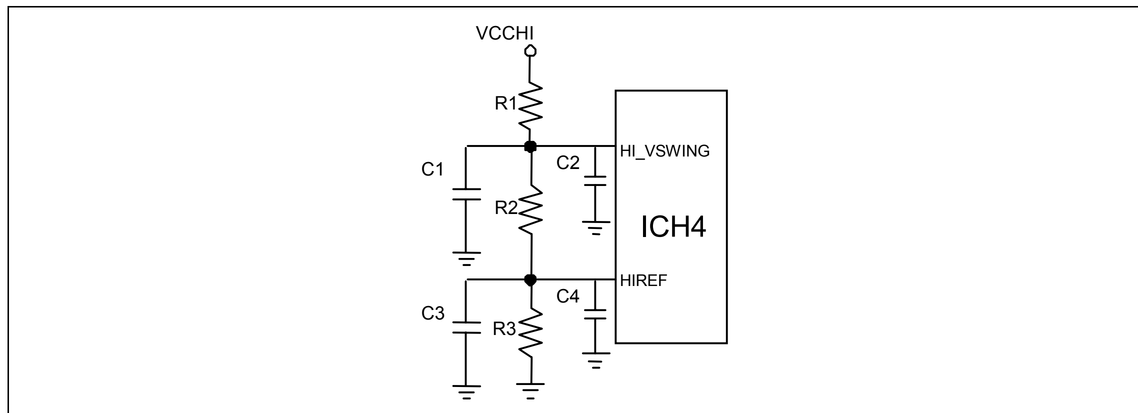
9.3.2. Locally Generated Voltage Reference Divider Circuit

Sections 9.3.2.1 and 9.3.2.2 provide the option to generate the voltage references separately for GMCH and ICH4-M. This option should be used if the routing distance between GMCH and ICH4-M is greater than 4 inches.

9.3.2.1. ICH4-M Single Generated Voltage Reference Divider Circuit

This option allows the ICH4-M to use one voltage divider circuit to generate both HIVREF and HI_VSWING voltage references. The reference voltage for both HIVREF and HI_VSWING must meet the voltage specification in Table 61. The resistor values R1, R2, and R3 must be rated at 1% tolerance (see Table 62). Normal care needs to be taken to minimize crosstalk to other signals (< 10-15 mV). If the voltage specifications are not met then individually generated voltage divider circuit for HIVREF and HI_VSWING is required.

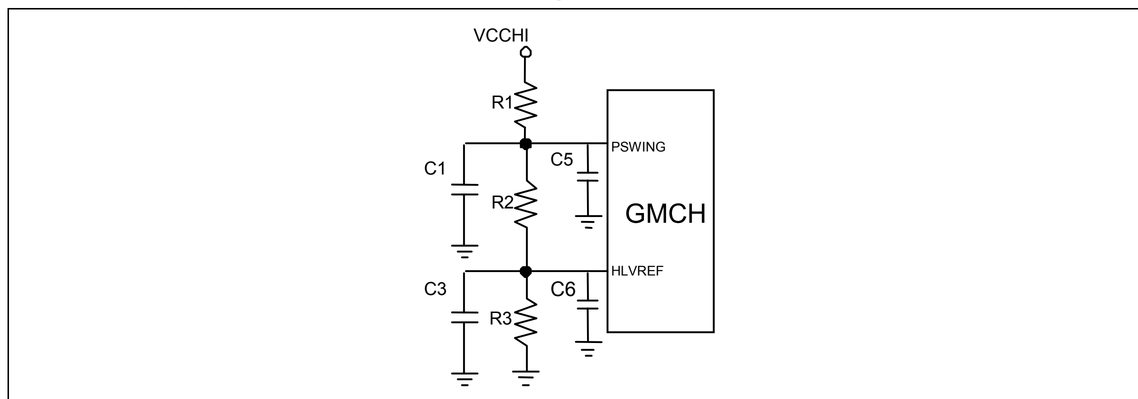
Figure 69. ICH4-M Locally Generated Reference Voltage Divider Circuit



9.3.2.2. GMCH Single Generated Voltage Reference Divider Circuit

This option allows the GMCH to use one voltage divider circuit to generate both HLVREF and HLPSWING voltage references. The reference voltage for both HLVREF and HLPSWING must meet the voltage specification in Table 61. The resistor values R1, R2, and R3 must be rated at 1% tolerance (see Table 62). Normal care needs to be taken to minimize crosstalk to other signals (< 10-15 mV). If the voltage specifications are not met, then individually generated voltage divider circuits for HLVREF and PSWING is required.

Figure 70. GMCH Locally Generated Reference Voltage Divider Circuit



9.3.3. Separate GMCH and ICH4-M Voltage Divider Circuits for VREF and VSWING

Sections 9.3.3.1 and 9.3.3.2 provide the option to generate individual voltage reference for VREF and VSWING separately for GMCH and ICH4-M.

9.3.3.1. Separate ICH4-M Voltage Divider Circuits for HIVREF and HI_VSWING

This option allows for tuning the voltage references HIVREF and HI_VSWING individually. The reference voltage for both HIVREF and HI_VSWING must meet the voltage specification in Table 61. Normal care needs to be taken to minimize crosstalk to other signals (< 10-15 mV).

Figure 71. Individual HIVREF and HI_VSWING Voltage Reference Divider Circuits for ICH4-M

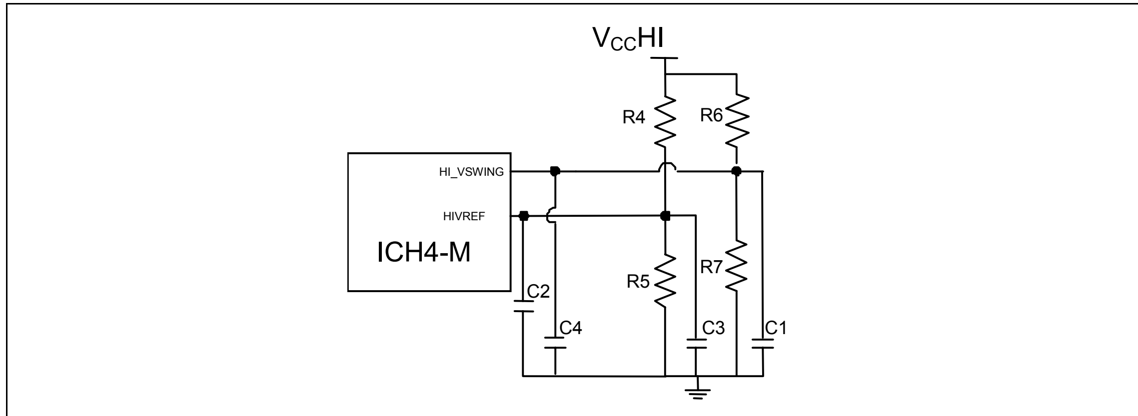


Table 63. Recommended Resistor Values for HIVREF and HI_VSWING Divider Circuits for ICH4-M

Signal	Recommended Resistor Values	VCCHI	Capacitor value
HIVREF (350 mV)	R4 = 487 Ω ± 1% R5 = 150 Ω ± 1%,	VCCHI=1.5 V	C3 = 0.1 μF (near divider) C2 = 0.01 μF (near component)
HI_VSWING (800 mV)	R6 = 130 Ω ± 1% R7 = 150 Ω ± 1%,	VCCHI=1.5 V	C1 = 0.1 μF (near divider) C4 = 0.01 μF (near component)

9.3.3.2. Separate GMCH Voltage Divider Circuits for HLVREF and PSWING

This option allows for tuning the voltage references HLVREF and PSWING individually. The reference voltage for both HLVREF and PSWING must meet the voltage specification in Table 61. Normal care needs to be taken to minimize crosstalk to other signals (< 10-15 mV).

Figure 72. Individual HLVREF and PSWING Voltage Reference Divider Circuits for GMCH

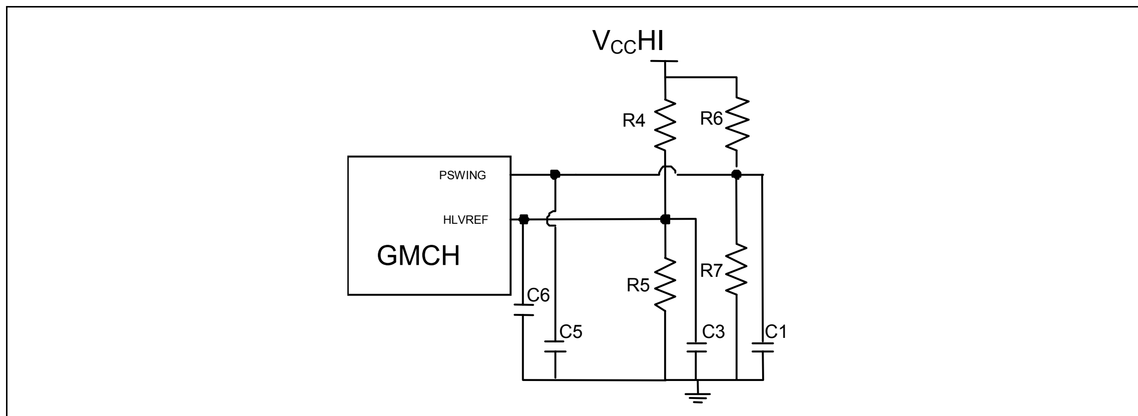


Table 64. Recommended Resistor Values for HLVREF and PSWING Divider Circuits for GMCH

Signal Name	Recommended Resistor Values	VCCHI	Capacitor
HLVREF (350 mV)	R4 = 243 Ω ± 1% R5 = 100 Ω ± 1%	VCCHI=1.2 V	C3 = 0.1 µF (near divider) C6 = 0.01 µF (near component)
PSWING (800 mV)	R6 = 49.9 Ω ± 1% R7 = 100 Ω ± 1%	VCCHI=1.2 V	C1 = 0.1 µF (near divider) C5 = 0.01 µF (near component)

9.4. Hub Interface Decoupling Guidelines

To improve I/O power delivery, use two 0.1-µF capacitors per each component (i.e. the ICH4-M and GMCH). These capacitors should be placed within 50 mils from each package, adjacent to the rows that contain the Hub Interface. If the layout allows, wide metal fingers running on the V_{SS} side of the board should connect the V_{CC}HI side of the capacitors to the V_{CC}HI power pins. Similarly, if layout allows, metal fingers running on the V_{CC}HI side of the board should connect the groundside of the capacitors to the V_{SS} power pins.

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10. I/O Subsystem

10.1. IDE Interface

This section contains guidelines for connecting and routing the ICH4-M IDE interface. The ICH4-M has two independent IDE channels. The ICH4-M has integrated the series resistors that have been typically required on the IDE data signals (PDD[15:0] and SDD[15:0]) running to the two ATA connectors. While it is not anticipated that additional series termination resistors will be required, OEMs should verify motherboard signal integrity through simulation. Additional external 0-Ω resistors can be incorporated into the design to address possible noise issues on the motherboard. The additional resistor layout increases flexibility by offering stuffing options at a later date.

The IDE interface can be routed with 5-mil traces on 7-mil spaces, and must be less than 8 inches long (from ICH4-M to IDE connector). Additionally, the maximum length difference between the shortest data signal and the longest strobe signal of a channel is 0.5 inches.

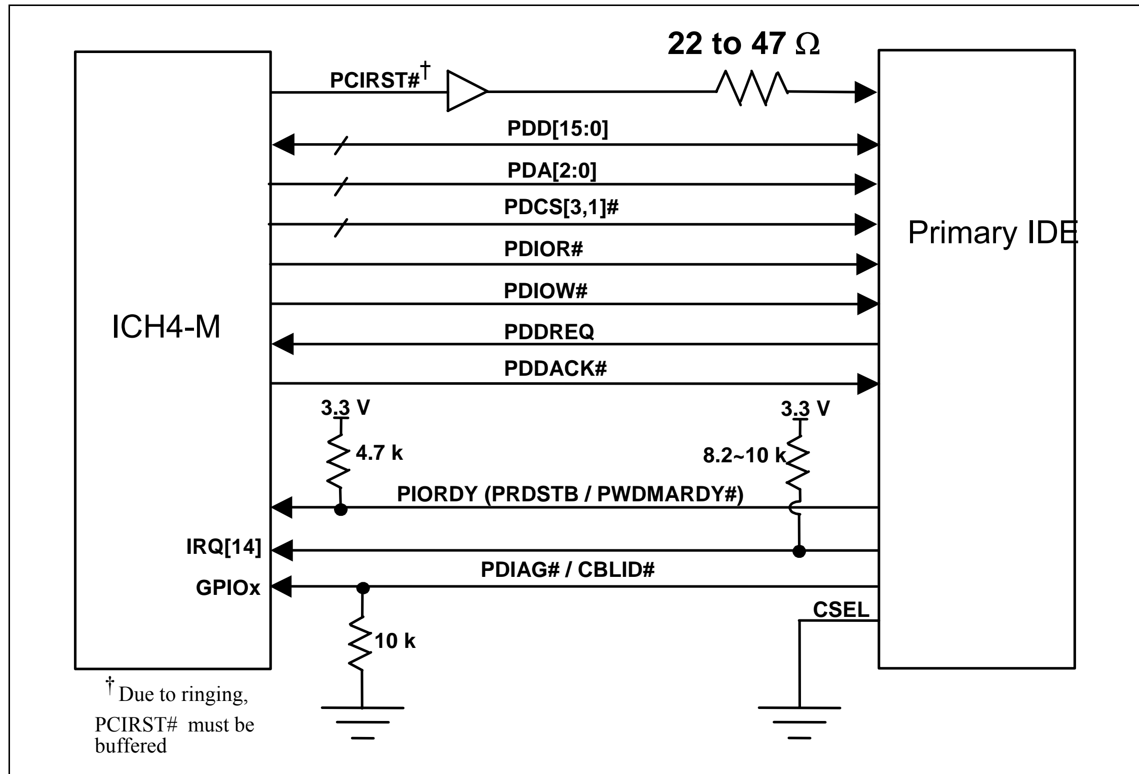
10.1.1. Cabling

This section provides guidelines for IDE connector cabling and motherboard design, including component and resistor placement, and signal termination for both IDE channels.

- Length of cable: Each IDE cable must be equal to or less than 18 inches.
- Capacitance: Less than 35 pF.
- Placement: A maximum of 6 inches between drive connectors on the cable. If a single drive is placed on the cable it should be placed at the end of the cable. If a second drive is placed on the same cable, it should be placed on the next closest connector to the end of the cable (6 inches away from the end of the cable).
- Grounding: Provide a direct low impedance chassis path between the motherboard ground and hard disk drives.
- The ICH4-M Placement: The ICH4-M must be placed equal to or less than 8 inches from the ATA connector(s).

10.1.2. Primary IDE Connector Requirements

Figure 73. Connection Requirements for Primary IDE Connector



- 22 Ω - 47 Ω series resistors are required on RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.
- An 8.2 kΩ - 10 kΩ pull-up resistor is required on IRQ14 to VCC3_3.
- A 4.7-kΩ, pull-up resistor to VCC3_3 is required on PIORDY.
- Series resistors can be placed on the control and data line to improve signal quality. The resistors are placed as close to the connector as possible. Values are determined for each unique motherboard design.
- The 10-kΩ resistor to ground on the PDIAG#/CBLID# signal is required on the Primary Connector. This change is to prevent the GPI pin from floating if a device is not present on the IDE interface.

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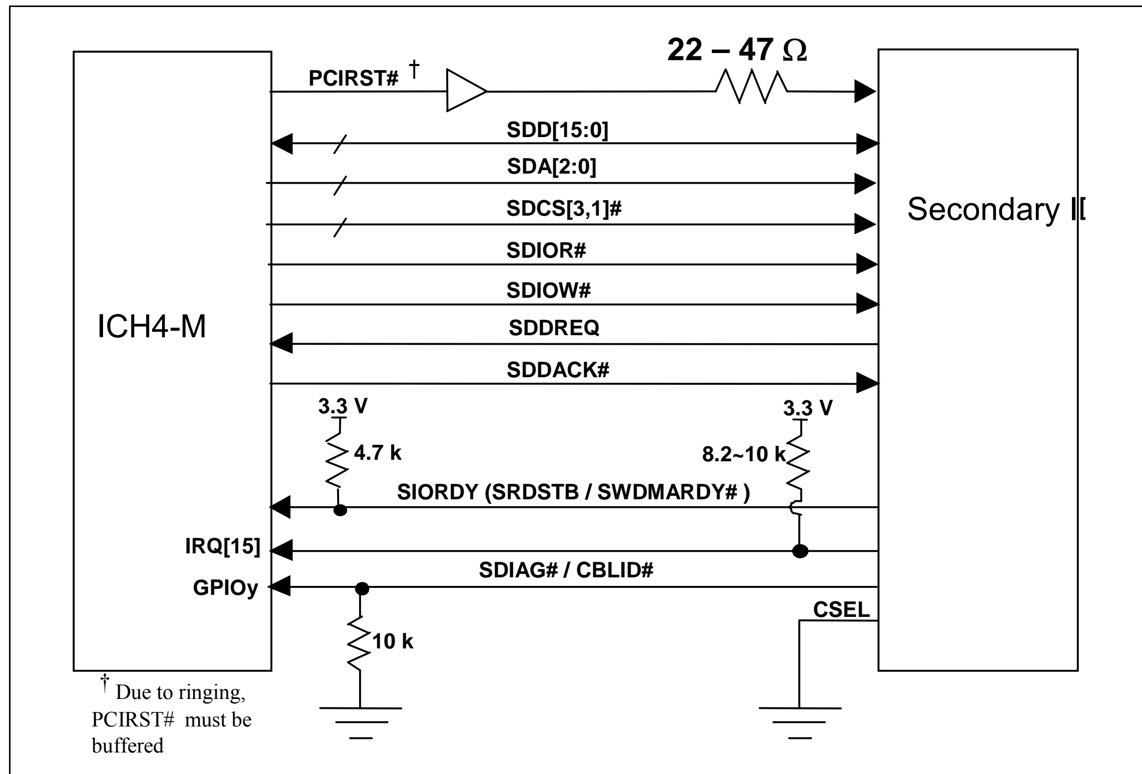
10.1.3. Secondary IDE Connector Requirements

Figure 74. Connection Requirements for Secondary IDE Connector



- 22 Ω - 47 Ω series resistors are required on RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.
- An 8.2 kΩ - 10 kΩ pull-up resistor is required on IRQ15 to VCC3_3.
- A 4.7-kΩ, pull-up resistor to VCC3_3 is required on SIORDY.
- Series resistors can be placed on the control and data line to improve signal quality. The resistors are placed as close to the connector as possible. Values are determined for each unique motherboard design.
- The 10-kΩ resistor to ground on the SDIAG#/CBLID# signal is required on the Secondary Connector. This change is to prevent the GPI pin from floating if a device is not present on the IDE interface.

10.1.4. Mobile IDE Swap Bay Support

Systems that require the support for an IDE "hot" swap drive bay can be designed to utilize the tri-state feature of the ICH4-M's IDE interface to achieve this functionality. To support a mobile "hot" sway bay, the ICH4-M allows the IDE output signals to be tri-stated and input buffers to be turned off. This requires certain hardware and software requirements to be met for proper operation.

From a hardware perspective a minimum of two spare control signals (i.e. GPIO's) and a FET are needed to properly utilize the IDE tri-state feature. An IDE drive must have a reset signal (i.e. first

additional control signal) driving its reset pin and a power supply that is isolated from the rest of the IDE interface. To isolate the power supplied to the IDE drive bay, a second additional control signal is needed to control the enabling/disabling of a FET that supplies a separate plane flood powering the IDE drive and its interface.

Although actual hardware implementations may vary, the isolated reset signal and power plane are strict requirements. Systems that connect the IDE swap bay drive to the same power plane and reset signals of the ICH4-M should not use this IDE tri-state feature. Many IDE drives use the control and address lines as straps that are used to enter test modes. If the IDE drive is powered up along with the ICH4-M while the IDE interface is tri-stated rather than being driven to the default state, then the IDE drive could potentially enter a test mode. To avoid such a situation, the aforementioned hardware requirements or equivalent solution should be implemented.

10.1.4.1. ICH4-M IDE Interface Tri-State Feature

The new IDE interface tri-state capabilities of the ICH4-M also include a number of configuration bits that must be programmed accordingly for proper system performance. The names of the critical registers, their location, and brief description are listed below.

1. B0:D31:F0 Offset D5h (BACK_CNTL – Backed Up Control Register) bits [7:6] needs to be set to '1' in order to enable the tri-stating of the primary and secondary IDE pins when the interfaces are put into reset. By default both bits are set to '1'.
2. B0:D31:F0 Offset D0-D3h (GEN_CNTL – General Control Register) bit [3] should be set to '1' in order to lock the state of bits [7:6] at B0:D31:F0 Offset D5h. This prevents any inadvertent reprogramming of the IDE interface pins to a non-tri-state mode during reset by a rogue software program. By default this bit is set to '0' and BIOS should set this bit to '1'. This is a write once bit only and requires a PCIRST# to reset to '0'. Thus, this bit also needs to be set to '1' after resume from S3-S5.
3. B0:D31:F1 Offset 54h (IDE_CONFIG – IDE I/O Configuration Register) bits [19:18] (SEC_SIG_MODE) and bits [17:16] (PRIM_SIG_MODE) control the reset states of the secondary and primary IDE channels, respectively. The values in SEC_SIG_MODE and PRIM_SIG_MODE are tied to the values set by the BACK_CNTRL register bits [7:6], respectively. When bits [7:6] are set to '1', the PRIM_SIG_MODE and SEC_SIG_MODE will be set to '01' for tri-state when the either IDE channel is put in reset.
4. B0:D31:F1 Offset 40-41h (Primary) and 42-23h (Secondary) bit [5] and bit [1] (IDE_TIM – IDE Timing Register) are the IORDY Sample Point Enable bits for drive 1 and 0 of the primary and secondary IDE channels, respectively. By default, these bits are set to '0' and during normal power-up, should be set to '1' by the BIOS to enable IORDY assertion from the IDE device when an access is requested.

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10.1.4.2. S5/G3 to S0 Power-Up Procedures for IDE Swap Bay

The procedures listed below summarize the steps that must be followed during power-up of an IDE sway bay drive:

1. ICH4-M powers up, IDE interface is tri-stated, disk drive is not powered up. IDE drive is recognized as being on a separate power plane and its reset is different from the ICH4-M.
2. BIOS powers on the IDE drive. e.g. GPIO is used to switch on a FET on the board.
3. Once the IDE drive and interface is powered up, the ICH4-M exits from tri-state mode and begins to actively the interface.
4. Once ready, the BIOS can de-assert the reset signal to the IDE drive. e.g. GPIO routed to the IDE drive's reset pin.

10.1.4.3. Power Down Procedures for Mobile Swap Bay

The procedures listed below summarize the steps that must be followed in order to remove an IDE device from the mobile swap bay.

1. User indicates to the system that removal of IDE device from the mobile swap bay should begin. Once the system recognizes that all outstanding IDE accesses have completed, the reset signal to the swap device should be asserted.
2. The IDE channel (primary or secondary) that the device resides on should then be set to drive low mode rather than the default tri-state mode. This requires setting the IDE_CONFIG register (B0:D31:F0 Offset 54h) bits [19:18] or [17:16] to '10' (10b). This will cause all IDE outputs to the IDE drive to drive low rather than the default tri-state (which is useful during boot up to prevent any IDE drives from entering a test mode).
3. The IORDY Sample Point Enable bit of the IDE_TIM register for the appropriate IDE device should then be set to '0' to disable IORDY sampling by the ICH4-M. This ensures that zeros will always be returned if the OS attempts to access the IDE device being swapped.
4. Power to the isolated power plane of the IDE device can then be removed and the system can indicate to the user that the mobile swap bay can be removed and the IDE device replaced.

10.1.4.4. Power-Up Procedures After Device "Hot" Swap Completed

The procedures listed below summarize the steps that must be followed after a new IDE device has been added to the mobile swap bay and the swap bay must be powered back up:.

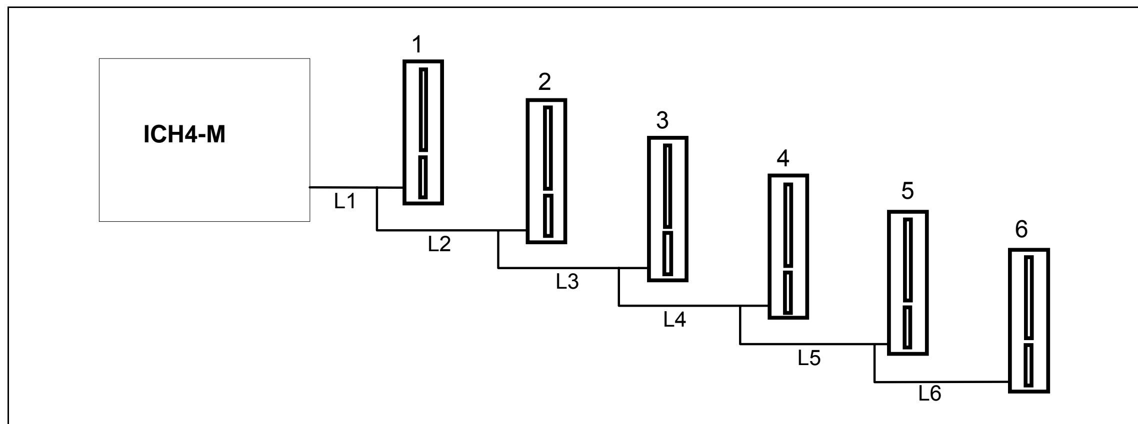
1. Once the IDE swap bay is replaced into the system, the power plane to the device should be enabled once again.
2. The IORDY Sample Point Enable bit of the IDE_TIM register for the appropriate IDE device should then be set to '1' to enable IORDY sampling by the ICH4-M. This allows the OS to access the IDE device once again and waits for the assertion of IORDY in response to an access request.
3. Once the system IDE interface is configured for normal operation once again, the reset signal to the swap device should be deasserted to allow the drive to initialize.

10.2. PCI

The ICH4-M provides a PCI Bus interface that is compliant with the *PCI Local Bus Specification Revision 2.2*. The implementation is optimized for high performance data streaming when the ICH4-M is acting as either the target or the initiator in the PCI bus.

The ICH4-M supports six PCI Bus masters (excluding the ICH4-M), by providing six REQ#/GNT# pairs. In addition, the ICH4-M supports two PC/PCI REQ#/GNT# pairs, one of which is multiplexed with a PCI REQ#/GNT# pair.

Figure 75. PCI Bus Layout Example



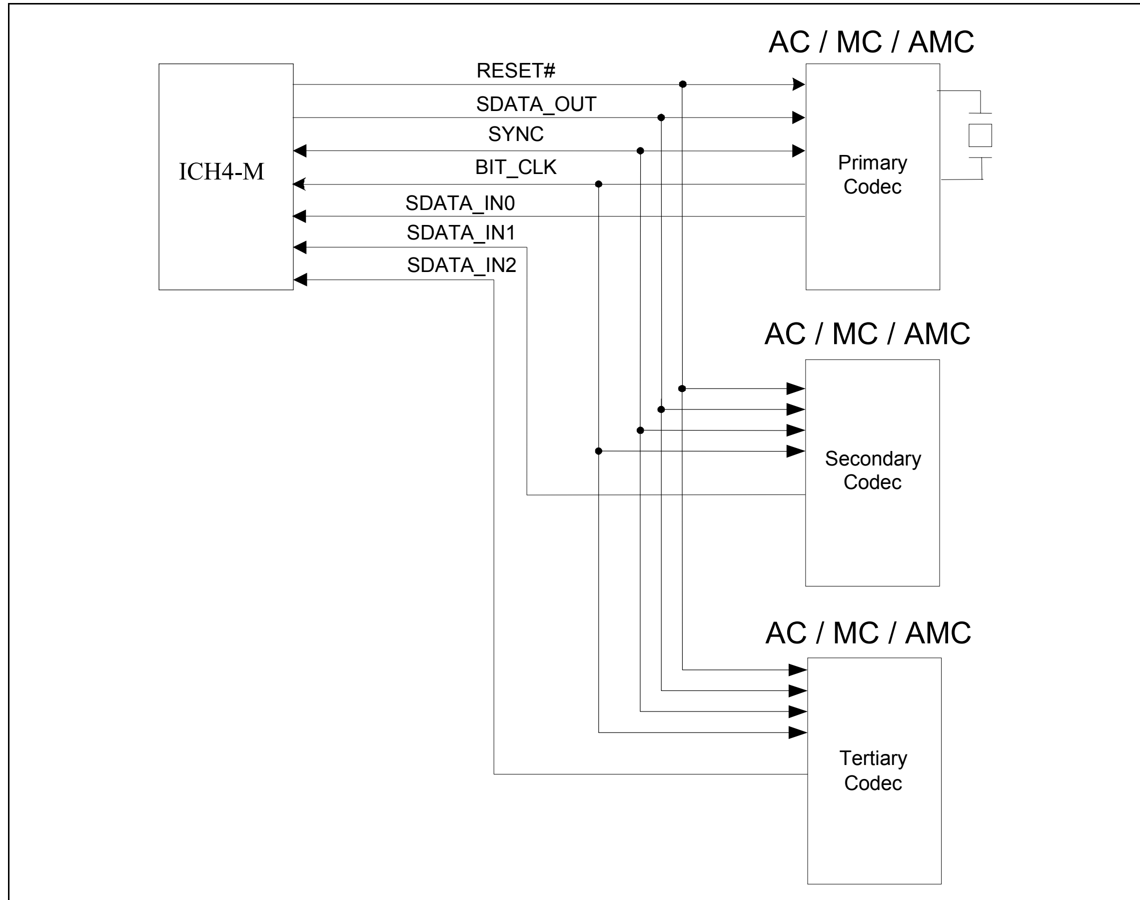
10.3. AC'97

The ICH4-M implements an AC'97 2.1, 2.2, and 2.3 compliant digital controller. Please contact your codec IHV (Independent Hardware Vendor) for information on 2.2 compliant products. The AC'97 2.2 specification is on the Intel website:

http://developer.intel.com/ial/scalableplatforms/audio/index.htm - 97spec/

The AC-link is a bi-directional, serial PCM digital stream. It handles multiple input and output data streams, as well as control register accesses that employs a time division multiplexed (TDM) scheme. The AC-link architecture provides for data transfer through individual frames transmitted in a serial fashion. Each frame is divided into 12 outgoing and 12 incoming data streams or slots. The architecture of the ICH4-M AC-link allows a maximum of three codecs to be connected. Figure 76 shows a three-codec topology of the AC-link for the ICH4-M.

Figure 76. ICH4-M AC'97 – Codec Connection



Note: If a modem codec is configured as the primary AC-link Codec, there should not be any Audio Codecs residing on the AC-link. The primary codec may be connected to AC_SDIN0 as documented in the *Intel® 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)I/O Controller Datasheet*.

Clocking is provided from the primary codec on the link via AC_BIT_CLK and is derived from a 24.576-MHz crystal or oscillator. Refer to the primary codec vendor for crystal or oscillator requirements. AC_BIT_CLK is a 12.288-MHz clock driven by the primary codec to the digital controller (ICH4-M) and to any other codec present. That clock is used as the time base for latching and driving data. **Clocking AC_BIT_CLK directly off the CK-408 clock chip's 14.31818 MHz output is not supported.**

The ICH4-M supports wake-on-ring from S1M-S5 via the AC'97 link. The codec asserts AC_SDIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec.

The ICH4-M has weak pull-down and pull-ups that are always enabled. This will keep the link from floating when the AC-link is off or there are no codecs present.

If the Shut-off bit is not set, it implies that there is a codec on the link. Therefore, AC_BIT_CLK and AC_SDOUT will be driven by the codec and the ICH4-M respectively. However, AC_SDIN0, AC_SDIN1, and AC_SDIN2 may not be driven. If the link is enabled, the assumption can be made that there is at least one codec.

Figure 77. ICH4-M AC'97 – AC_BIT_CLK Topology

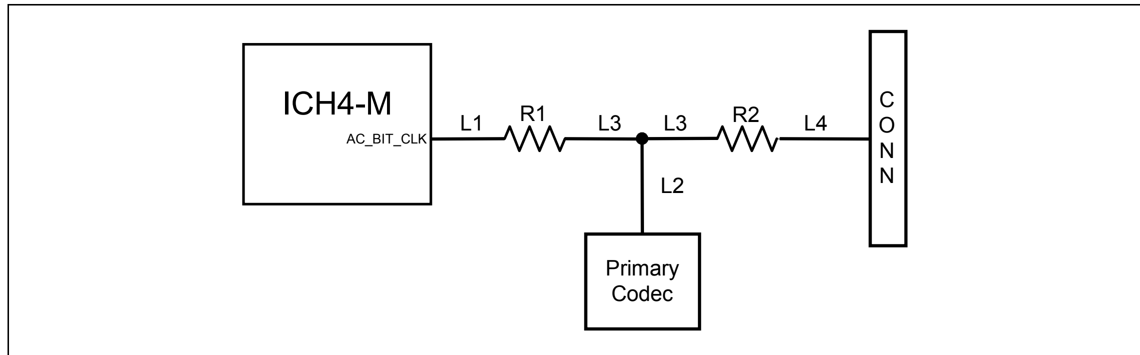


Table 65. AC'97 AC_BIT_CLK Routing Summary

AC'97 Routing Requirements	Maximum Trace Length (inches)	Series Termination Resistance	AC_BIT_CLK Signal Length Matching
5 on 5	L1 = (1 to 8) – L3 L2 = 0.1 to 6 L3 = 0.1 to 0.4 L4 = (1 to 6) – L3	R1 = 33 Ω - 47 Ω R2 = Option 0 Ω resistor for debugging purposes	N/A

NOTES:

1. Simulations were performed using Analog Device's Codec (AD1885) and the Cirrus Logic's Codec (CS4205b). Results showed that if the AD1885 codec was used a 33-Ω resistor was best for R1 and if the CS4205b codec was used a 47-Ω resistor for R1 was best.
2. Bench data shows that a 47-Ω resistor for R1 is best for the Sigmatel* 9750 codec.

Figure 78. ICH4-M AC'97 – AC_SDOUT/AC_SYNC Topology

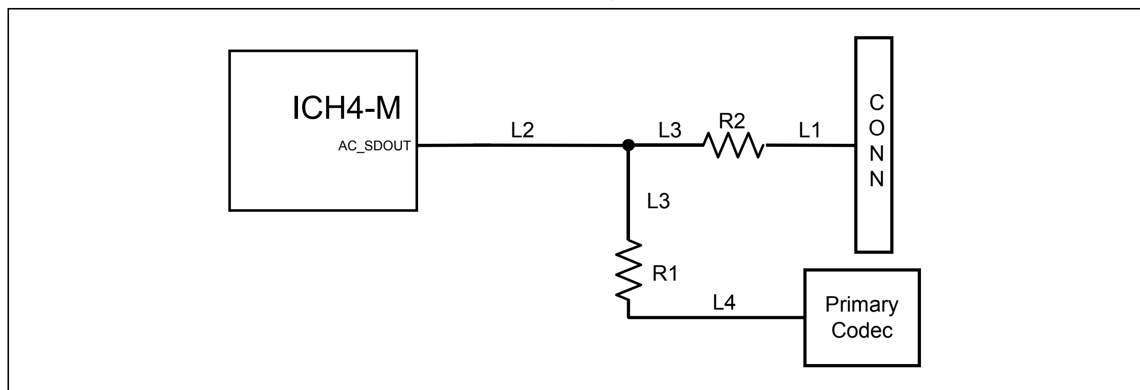


Table 66. AC'97 AC_SDOUT/AC_SYNC Routing Summary

AC'97 Routing Requirements	Maximum Trace Length (inches)	Series Termination Resistance	AC_SDOUT/AC_SYNC Signal Length Matching
5 on 5	L1 = (1 to 6) – L3 L2 = 1 to 8 L3 = 0.1 to 0.4 L4 = (0.1 to 6) – L3	R1 = 33 Ω - 47 Ω R2 = R1 if the connector card that will be used with the platform does not have a series termination on the card. Otherwise R2 = 0 Ω	N/A

NOTES:

1. Simulations were performed using Analog Device's* Codec (AD1885) and the Cirrus Logic's* Codec (CS4205b). Results showed that if the AD1885 codec was used a 33-Ω resistor was best for R1 and if the CS4205b codec was used a 47-Ω resistor for R1 was best.
2. Bench data shows that a 47-Ω resistor for R1 is best for the Sigmatel* 9750 codec.

Figure 79. ICH4-M AC'97 – AC_SDIN Topology

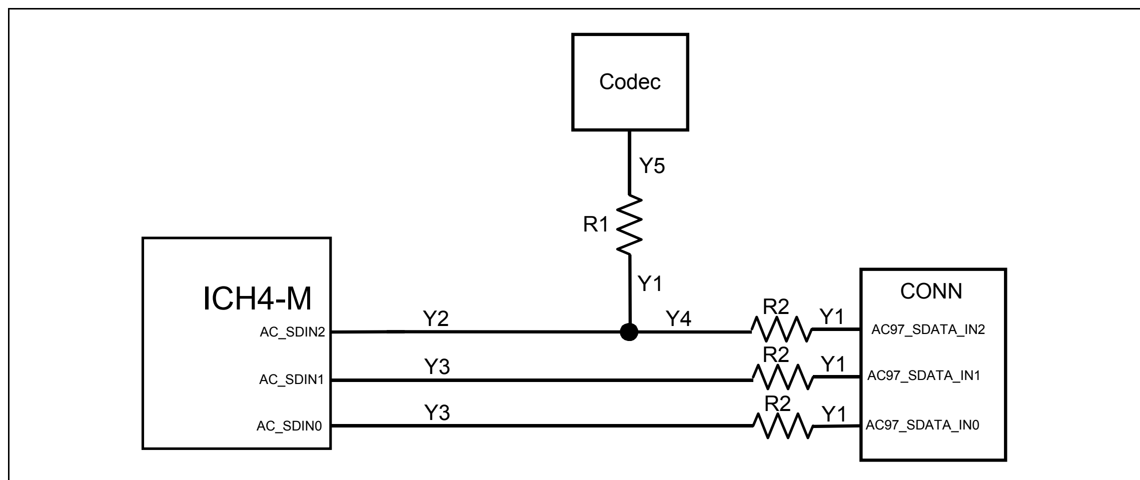


Table 67. AC'97 AC_SDIN Routing Summary

AC'97 Routing Requirements	Maximum Trace Length (inches)	Series Termination Resistance	AC_SDIN Signal Length Matching
5 on 5	Y1 = 0.1 to 0.4 Y2 = (1 to 8) – Y1 Y3 = (1 to 14) – Y1 Y4 = (1 to 6) – Y1 Y5 = (0.1 to 6) – Y1	R1 = 33 Ω - 47 Ω R2 = R1 if the connector card that will be used with the platform does not have a series termination on the card. Otherwise R2 = 0 Ω	N/A

NOTES:

1. Simulations were performed using Analog Device's Codec (AD1885) and the Cirrus Logic's Codec (CS4205b). Results showed that if the AD1885 codec was used a 33-Ω resistor was best for R1 and if the CS4205b codec was used a 47-Ω resistor for R1 was best.
2. Bench data shows that a 47-Ω resistor for R1 is best for the Sigmatel 9750 codec.

10.3.1. AC'97 Routing

To ensure the maximum performance of the codec, proper component placement and routing techniques are required. These techniques include properly isolating the codec, associated audio circuitry, analog power supplies, and analog ground planes, from the rest of the motherboard. This includes plane splits and proper routing of signals not associated with the audio Section. Contact your vendor for device-specific recommendations.

The basic recommendations are as follows:

- Special consideration must be given for the ground return paths of the analog signals.
- Digital signals routed in the vicinity of the analog audio signals must not cross the power plane split lines. Analog and digital signals should be located as far as possible from each other.
- Partition the board with all analog components grouped together in one area and all digital components in another.
- Separate analog and digital ground planes should be provided, with the digital components over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. The split between planes must be a minimum of 0.05 inches wide.
- Keep digital signal traces, especially the clock, as far as possible from the analog input and voltage reference pins.
- Do not completely isolate the analog/audio ground plane from the rest of the board ground plane. There should be a single point (0.25 inches to 0.5 inches wide) where the analog/isolated ground plane connects to the main ground plane. The split between planes must be a minimum of 0.05 inches wide.
- Any signals entering or leaving the analog area must cross the ground split in the area where the analog ground is attached to the main motherboard ground. That is, no signal should cross the split/gap between the ground planes because doing so would cause a ground loop, thereby greatly increasing EMI emissions and degrading the analog and digital signal quality.
- Analog power and signal traces should be routed over the analog ground plane.
- Digital power and signal traces should be routed over the digital ground plane.
- Bypassing and decoupling capacitors should be close to the IC pins, or positioned for the shortest connections to pins, with wide traces to reduce impedance.
- All resistors in the signal path or on the voltage reference should be metal film. Carbon resistors can be used for DC voltages and the power supply path, where the voltage coefficient, temperature coefficient, and noise are not factors.
- Regions between analog signal traces should be filled with copper, which should be electrically attached to the analog ground plane. Regions between digital signal traces should be filled with copper, which should be electrically attached to the digital ground plane.
- Locate the crystal or oscillator close to the codec.

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10.3.2. Motherboard Implementation

The following design considerations are provided for the implementation of an ICH4-M platform using AC'97. These design guidelines have been developed to ensure maximum flexibility for board designers, while reducing the risk of board-related issues. These recommendations are not the only implementation or a complete checklist, but they are based on the ICH4-M platform.

- Active components such as FET switches, buffers or logic states should not be implemented on the AC-link signals, except for AC_RST#. Doing so would potentially interfere with timing margins and signal integrity.
- The ICH4-M supports wake-on-ring from S1M-S5 states via the AC'97 link. The codec asserts AC_SDIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec. If no codec is attached to the link, internal pull-downs will prevent the inputs from floating, so external resistors are not required.
- PC_BEEP should be routed through the audio codec. Care should be taken to avoid the introduction of a pop when powering the mixer up or down.

10.3.2.1. Valid Codec Configurations

Table 68. Supported Codec Configurations

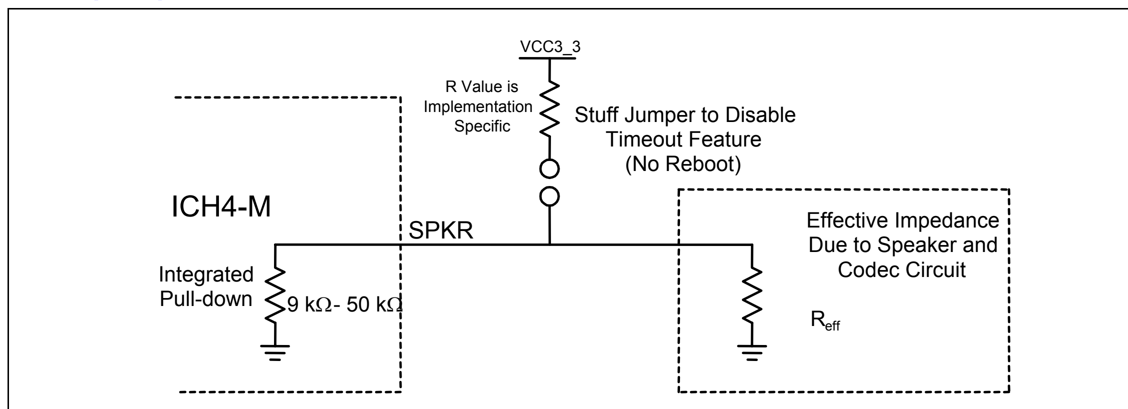
Option	Primary Codec	Secondary Codec	Tertiary Codec	Notes
1	Audio	Audio	Audio	1
2	Audio	Audio	Modem	1
3	Audio	Audio	Audio/Modem	1
4	Audio	Modem	Audio	1
5	Audio	Audio/Modem	Audio	1
6	Audio/Modem	Audio	Audio	1

NOTES:
1. For power management reasons, codec power management registers are in audio space. As a result, if there is an audio codec in the system it must be Primary.
2. There cannot be two modems in a system since there is only one set of modem DMA channels.
3. The ICH4-M supports a codec on any of the AC_SDIN lines; however, the modem codec ID must be either 00 or 01.

10.3.3. SPKR Pin Configuration

SPKR is used as both the output signal to the system speaker and as a functional strap. The strap function enables or disables the "TCO Timer Reboot function" based on the state of the SPKR pin on the rising edge of PWROK. When enabled, the ICH4-M sends an SMI# to the processor upon a TCO timer timeout. The status of this strap is readable via the NO_REBOOT bit (bit 1, D31: F0, Offset D4h). The SPKR signal has a weak integrated pull-down resistor (the resistor is only enabled during boot/reset). Therefore, its default state is a logical zero or set to reboot. To disable the feature, a jumper can be populated to pull the signal line high (see Figure 80). The value of the pull-up must be such that the voltage divider output caused by the pull-up, the effective pull-down (R_{eff}), and the ICH4-M's integrated pull-down resistor will be read as logic high (0.5 * VCC3_3 to VCC3_3 + 0.5 V).

Figure 80. Example Speaker Circuit



10.4. USB 2.0 Guidelines and Recommendations

10.4.1. Layout Guidelines

10.4.1.1. General Routing and Placement

Use the following general routing and placement guidelines when laying out a new design. These guidelines will help to minimize signal quality issuesand EMI problems. The USB 2.0 validation efforts focused on a four-layer motherboard where the first layer is a signal layer, the second plane is power, the third plane is ground, and the fourth plane is a signal layer. This results in the placement of most of the routing on the fourth plane (closest to the ground plane), allowing a higher component density on the first plane.

1. Place the ICH4-M and major components on the un-routed board first. With minimum trace lengths, route high-speed clock, periodic signals, and USB 2.0 differential pairs first. Maintain maximum possible distance between high-speed clocks/periodic signals to USB 2.0 differential pairs and any connector leaving the PCB (i.e. I/O connectors, control and signal headers, or power connectors).
2. USB 2.0 signals should be ***ground referenced*** (on recommended stack-up this would be the bottom signal layer).
3. Route USB 2.0 signals using a minimum of vias and corners. This reduces reflections and impedance changes.
4. When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal by minimizing impedance discontinuities. (As shown in Figure 102.)
5. Do not route USB 2.0 traces under crystals, oscillators, clock synthesizers, magnetic devices or IC's that use and/or duplicate clocks.
6. Stubs on high speed USB signals should be avoided, as stubs will cause signal reflections and affect signal quality. If a stub is unavoidable in the design, the sum of all stubs for a particular signal line should not exceed 200 mils.
7. Route all traces over continuous planes (VCC or GND), with no interruptions. Avoid crossing over anti-etch if at all possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with USB 2.0

traces as much as practical. It is preferable to change layers to avoid crossing a plane split. Refer to Section 10.4.2.

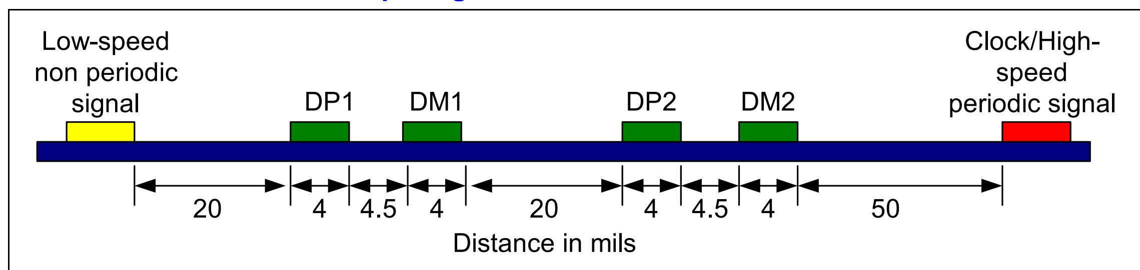
8. Separate signal traces into similar categories and route similar signal traces together (such as routing differential pairs together).
9. Keep USB 2.0 USB signals clear of the core logic set. High current transients are produced during internal state transitions and can be very difficult to filter out.
10. Follow the 20*h thumb rule by keeping traces at least 20*(height above the plane) away from the edge of the plane (VCC or GND, depending on the plane the trace is over). For the suggested stack-up the height above the plane is 4.5 mils. This calculates to a 90-mil spacing requirement from the edge of the plane. This helps prevent the coupling of the signal onto adjacent wires and also helps prevent free radiation of the signal from the edge of the PCB.

10.4.1.2. USB 2.0 Trace Separation

Use the following separation guidelines.

1. Maintain parallelism between USB differential signals with the trace spacing needed to achieve 90-Ω differential impedance. Deviations will normally occur due to package breakout and routing to connector pins. Just ensure the amount and length of the deviations are kept to the minimum possible.
2. Use an impedance calculator to determine the trace width and spacing required for the specific board stack-up being used. 4-mil traces with 4.5-mil spacing results in approximately 90-Ω differential trace impedance.
3. Minimize the length of high-speed clock and periodic signal traces that run parallel to high speed USB signal lines, to minimize crosstalk. Based on EMI testing experience, the minimum suggested spacing to clock signals is 50 mils.
4. Based on simulation data, use 20-mil minimum spacing between high-speed USB signal pairs and other signal traces for optimal signal quality. This helps to prevent crosstalk.

Figure 81. Recommended USB Trace Spacing



10.4.1.3. USBRBIAS Connection

The USBRBIAS pin and the USBRBIAS# pin can be shorted and routed 5 on 5 to one end of a 22.6 Ω ± 1% resistor to ground. Place the resistor within 500 mils of the ICH4-M and avoid routing next to clock pins.

Figure 82. USBRBIAS Connection

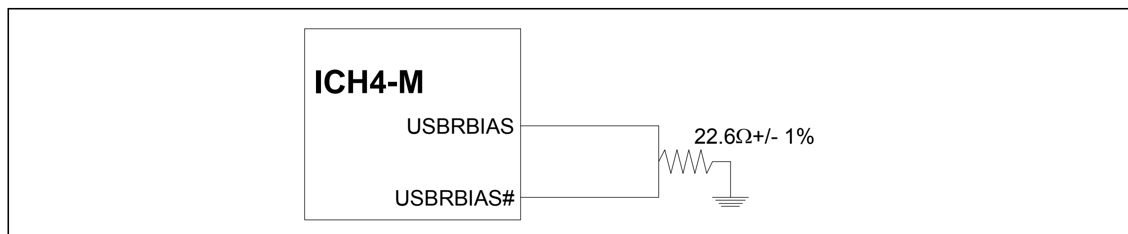


Table 69. USBRBIAS/USBRBIAS# Routing Summary

USBRBIAS/ USBRBIAS# Routing Requirements	Maximum Trace Length	Signal Length Matching	Signal Referencing
5 on 5	500 mils	N/A	N/A

10.4.1.4. USB 2.0 Termination

A common-mode choke should be used to terminate the USB 2.0 bus. Place the common-mode choke as close as possible to the connector pins. See Section 10.4.4 for details.

10.4.1.5. USB 2.0 Trace Length Pair Matching

USB 2.0 signal pair traces should be trace length matched. Max trace length mismatch between USB 2.0 signal pair should be no greater that 150 mils.

10.4.1.6. USB 2.0 Trace Length Guidelines

Table 70. USB 2.0 Trace Length Preliminary Guidelines (with Common Mode Choke)

Configuration	Signal Referencing	Signal Matching	Motherboard Trace Length	Card Trace Length	Maximum Total Length
Back Panel	Ground	150 mils	17 inches	N/A	17 inches

NOTES:
1. These lengths are based upon simulation results and may be updated in the future.
2. All lengths are based upon using a common-mode choke (see Section 10.4.4.1 for details on common-mode choke).

10.4.2. Plane Splits, Voids, and Cut-Outs (Anti-Etch)

The following guidelines apply to the use of plane splits voids and cutouts.

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10.4.2.1. VCC Plane Splits, Voids, and Cut-Outs (Anti-Etch)

Use the following guidelines for the V_{CC} plane.

1. Traces should not cross anti-etch, for it greatly increases the return path for those signal traces. This applies to USB 2.0 signals, high-speed clocks, and signal traces as well as slower signal traces that might be coupling to them. USB signaling is not purely differential in all speeds (i.e. the Full-speed Single Ended Zero is common mode).
2. Avoid routing of USB 2.0 signals 25 mils of any anti-etch to avoid coupling to the next split or radiating from the edge of the PCB.

When breaking signals out from packages it is sometimes very difficult to avoid crossing plane splits or changing signal layers, particularly in today's motherboard environment that uses several different voltage planes. Changing signal layers is preferable to crossing plane splits if a choice has to be made between one or the other.

If crossing a plane split is completely unavoidable, proper placement of stitching caps can minimize the adverse effects on EMI and signal quality performance caused by crossing the split. Stitching capacitors are small-valued capacitors (1 µF or lower in value) that bridge voltage plane splits close to where high speed signals or clocks cross the plane split. The capacitor ends should tie to each plane separated by the split. They are also used to bridge, or bypass, power and ground planes close to where a high-speed signal changes layers. As an example of bridging plane splits, a plane split that separates $V_{CC}5$ and $V_{CC}3_3$ planes should have a stitching cap placed near any high-speed signal crossing. One side of the cap should tie to $V_{CC}5$ and the other side should tie to $V_{CC}3_3$. Stitching caps provide a high frequency current return path across plane splits. They minimize the impedance discontinuity and current loop area that crossing a plane split creates.

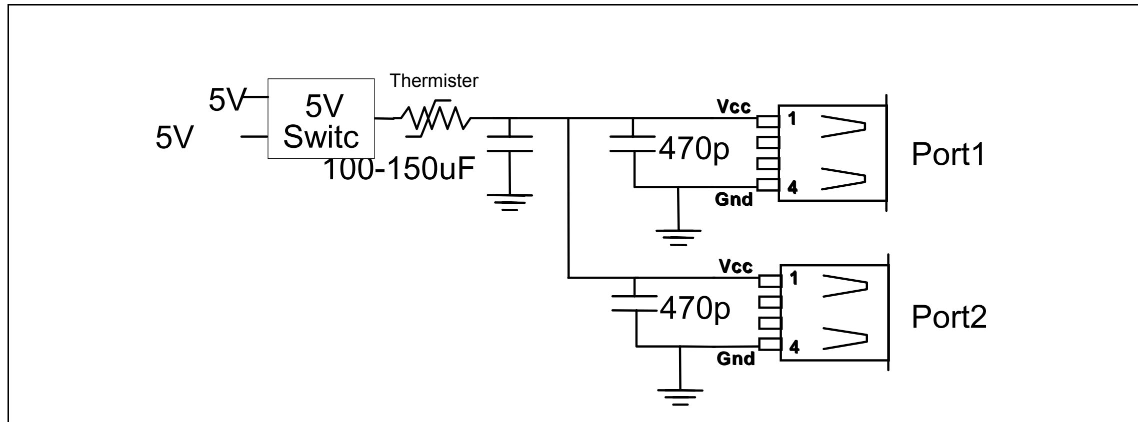
10.4.2.2. GND Plane Splits, Voids, and Cut-Outs (Anti-Etch)

Avoid anti-etch on the GND plane.

10.4.3. USB Power Line Layout Topology

The following is a suggested topology for power distribution of Vbus to USB ports. Circuits of this type provide two types of protection during dynamic attach and detach situations on the bus: inrush current limiting (droop) and dynamic detach fly-back protection. These two different situations require both bulk capacitance (droop) and filtering capacitance (for dynamic detach fly-back voltage filtering). It is important to minimize the inductance and resistance between the coupling capacitors and the USB ports. Capacitors should be placed as close as possible to the port and the power carrying traces should be as wide as possible, preferably, a plane. A good rule is to make the power carrying traces wide enough that the system fuse will blow on an over current event. If the system fuse is rated at 1 amp, then the power carrying traces should be wide enough to carry at least 1.5 amps.

Figure 83. Good Downstream Power Connection



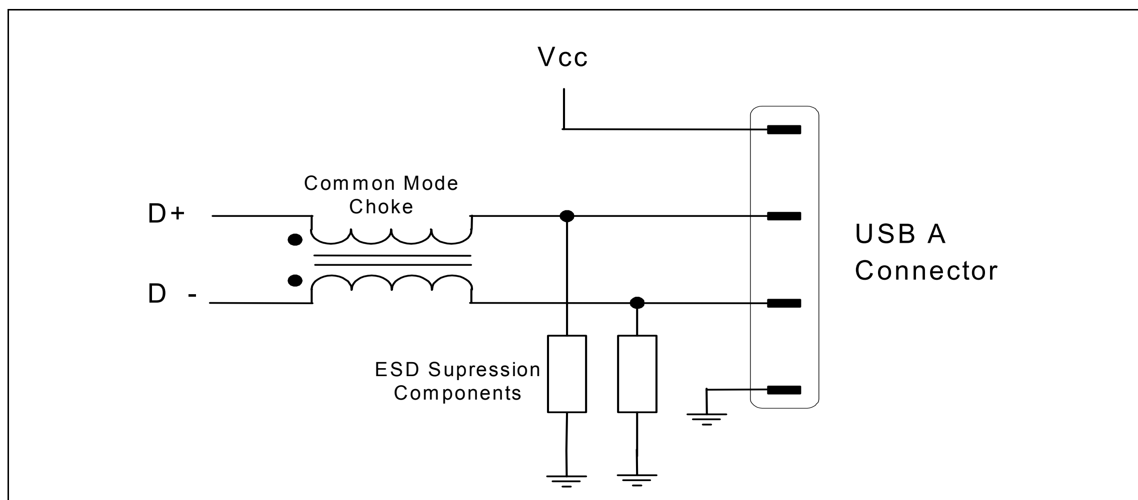
10.4.4. EMI Considerations

The following guidelines apply to the selection and placement of common-mode chokes and ESD protection devices.

10.4.4.1. Common Mode Chokes

Testing has shown that common-mode chokes can provide required noise attenuation. A design should include a common-mode choke footprint to provide a stuffing option **in the event** the choke is needed to pass EMI testing. Figure 84 shows the schematic of a typical common-mode choke and ESD suppression components. The choke should be placed as close as possible to the USB connector signal pins.

Figure 84. Common Mode Choke Schematic



Common mode chokes distort full-speed and high-speed signal quality. As the common mode impedance increases, the distortion will increase, so you should test the effects of the common mode choke on full speed and high-speed signal quality. Common mode chokes with a target impedance of 80 Ω to 90 Ω at 100 MHz generally provide adequate noise attenuation.

Finding a common mode choke that meets the designer's needs is a two-step process. A part must be chosen with the impedance value that provides the required noise attenuation. This is a function of the electrical and mechanical characteristics of the part chosen and the frequency and strength of the noise present on the USB traces that you are trying to suppress.

Once you have a part that gives passing EMI results, the second step is to test the effect this part has on signal quality. Higher impedance common-mode chokes generally have a greater damaging effect on signal quality, so care must be used when increasing the impedance without doing thorough testing. Thorough testing means that the signal quality must be checked for Low-speed, Full-speed, and High-speed USB operation.

10.4.5. ESD

Classic USB (1.0/1.1) provided ESD suppression using in line ferrites and capacitors forms a low pass filter. This technique doesn't work for USB 2.0 due to the much higher signal rate of high-speed data. A device that has been tested successfully is based on spark gap technology. Proper placement of any ESD protection device is on the data lines between the common-mode choke and the USB connector data pins as shown in Figure 84. Other types of low-capacitance ESD protection devices may work as well but were not investigated. As with the common mode choke solution, it is recommended to include footprints for some type of ESD protection device as a stuffing option in case it is needed to pass ESD testing.

10.5. IOAPIC (I/O Advanced Programmable Interrupt Controller)

On a Mobile Intel Pentium 4 Processor-M, mobile Intel Celeron Processor and Intel Celeron M Processor based platforms, the serial IOAPIC bus interface of the Intel ICH4-M should be disabled. IOAPIC is supported on the platform and the servicing of interrupts is accomplished via a processor Front Side Bus interrupt delivery mechanism.

IOxAPIC is enabled by setting DT bit, xAPIC and APIC_EN bit, BIOS needs to program these bits when IOxAPIC is enabled.

The IOxAPIC only use FSB as a medium of message transfer so grounding PICD[1:0] and PICCLK will not have any effect on FSB interrupt delivery and it will only affect serial APIC transfer.

The serial IOAPIC bus interface of the Intel ICH4-M should be disabled as follows.

- Tie APICCLK directly to ground
- Tie PICD0, PICD1 to ground through a 10-kΩ resistor (separate pull-downs are required if using XOR chain testing)

The Mobile Intel Pentium 4 processor- M, mobile Intel Celeron processor and Intel Celeron M processors do not have pins dedicated for an IOAPIC bus interface and no hardware change is necessary.

10.5.1. IOAPIC Disabling Options

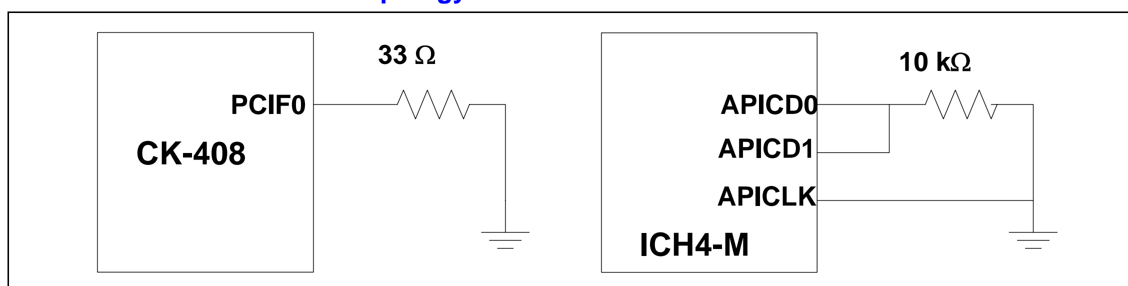
10.5.1.1. Recommended Implementation

Intel recommends that IOAPIC be disabled in software while the connections to the board are as shown in Figure 85. Software can be used to turn off PICCLK from clock generator.

To disable IOAPIC in BIOS:

- ICH4-M: D31:F0; Offset: D1; bit 7:8
- Mobile Pentium 4 Processor-M Processor: MSR 1Bh bit 11

Figure 85. Minimum IOAPIC Disable Topology



10.6. SMBus 2.0/SMLink Interface

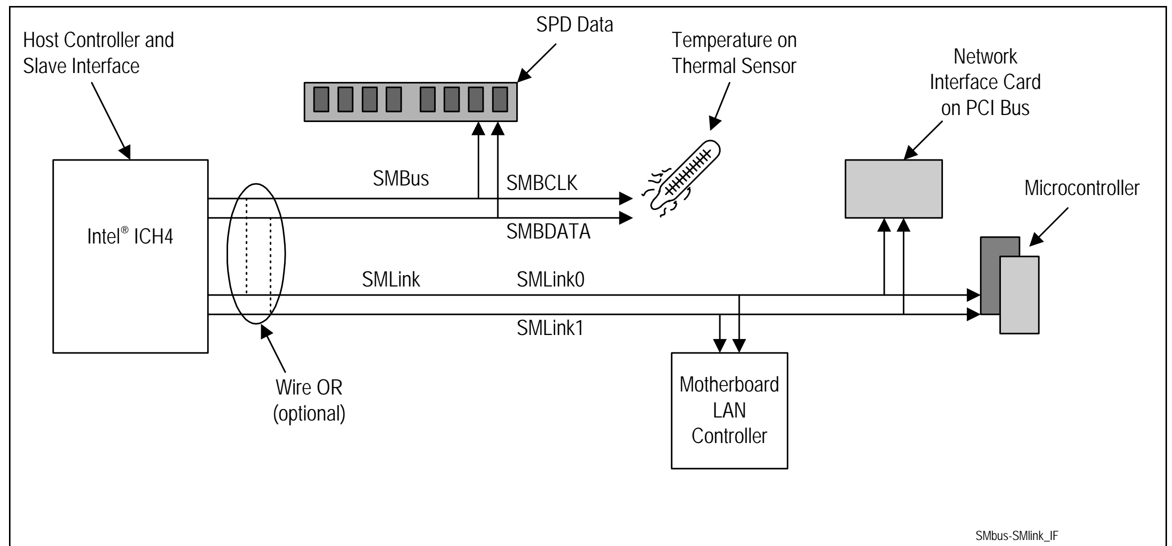
The SMBus interface on the ICH4-M uses two signals SMBCLK and SMBDATA to send and receive data from components residing on the bus. These signals are used exclusively by the SMBus Host Controller. The SMBus Host Controller resides inside the ICH4-M.

The ICH4-M incorporates an SMLink interface supporting Alert-on-LAN*, Alert-on-LAN2*, and a slave functionality. It uses two signals SMLINK[1:0]. SMLINK[0] corresponds to an SMBus clock signal and SMLINK[1] corresponds to an SMBus data signal. These signals are part of the SMB Slave Interface.

For Alert-on-LAN* functionality, the ICH4-M transmits heartbeat and event messages over the interface. When using the Intel® 82562EM Platform LAN Connect Component, the ICH4-M's integrated LAN Controller will claim the SMLink heartbeat and event messages and send them out over the network. An external, Alert-on-LAN2*-enabled LAN Controller (i.e. Intel 82562EM 10/100 Mbps Platform LAN Connect) will connect to the SMLink signals to receive heartbeat and event messages, as well as access the ICH4-M SMBus Slave Interface. The slave interface function allows an external micro-controller to perform various functions. For example, the slave write interface can reset or wake a system, generate SMI# or interrupts, and send a message. The slave read interface can read the system power state, read the watchdog timer status, and read system status bits.

Both the SMBus Host Controller and the SMBus Slave Interface obey the SMBus 1.0 protocol, so the two interfaces can be externally wire-OR'ed together to allow an external management ASIC (such as Intel 82562EM 10/100 Mbps Platform LAN Connect) to access targets on the SMBus as well as the ICH4-M Slave Interface. Additionally, the ICH4-M supports slave functionality, including the Host Notify protocol, on the SMLink pins. Therefore, in order to be fully compliant with the SMBus 2.0 specification (which requires the Host Notify cycle), the SMLink and SMBus signals **must** be tied together externally. This is done by connecting SMLink[0] to SMBCLK and SMLink[1] to SMBDATA.

Figure 86. SMBUS 2.0/SMLink Protocol



Note: Intel does not support external access of the ICH4-M's Integrated LAN Controller via the SMLink interface. Also, Intel does not support access of the ICH4-M's SMBus Slave interface by the ICH4-M's SMBus Host Controller. Refer to the *Intel® 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)I/O Controller Datasheet* for full functionality descriptions of the SMLink and SMBus interface.

10.6.1. SMBus Architecture and Design Considerations

10.6.1.1. SMBus Design Considerations

There is not a single SMBus design solution that will work for all platforms. One must consider the total bus capacitance and device capabilities when designing SMBus segments. Routing SMBus to the PCI slots makes the design process even more challenging since they add so much capacitance to the bus. This extra capacitance has a large affect on the bus time constant which in turn affects the bus rise and fall times.

Primary considerations in the design process are:

1. Device class (High/Low power). Most designs use primarily High Power Devices.
2. Are there devices that must run in S3?
3. Amount of $V_{CC_SUSPEND}$ current available, i.e. minimizing load of $V_{CC_SUSPEND}$.

10.6.1.2. General Design Issues and Notes

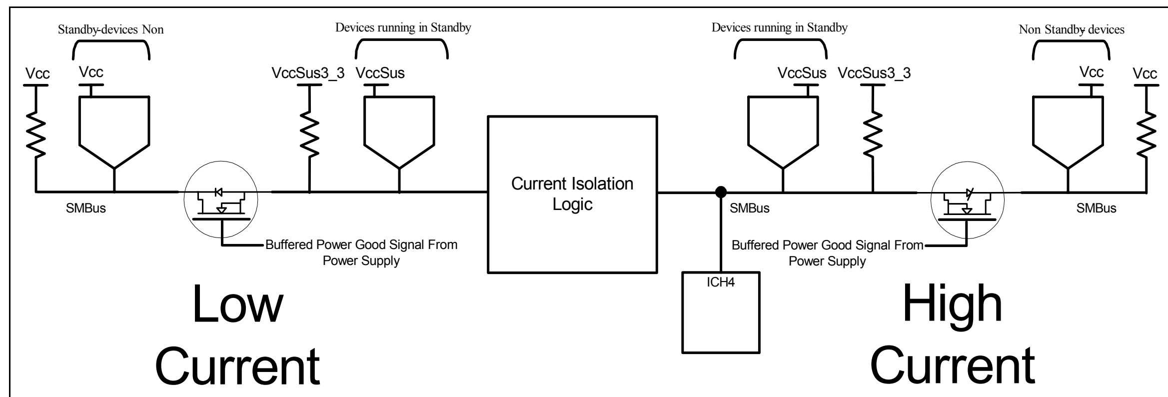
Regardless of the architecture used, there are some general considerations.

1. The pull-up resistor size for the SMBus data and clock signals is dependent on the bus load (this includes all device leakage currents). Generally the SMBus device that can sink the least amount of current is the limiting agent on how small the resistor can be. The pull-up resistor cannot be made so large that the bus time constant (Resistance X Capacitance) does not meet the SMBus rise and fall time specification.
2. The maximum bus capacitance that a physical segment can reach is 400 pF.
3. The ICH4-M does not run SMBus cycles while in S3.
4. SMBus devices that can operate in S3 must be powered by the $V_{CC_SUSPEND}$ supply.

10.6.1.3. High Power and Low Power Mixed Architecture

This design allows for current isolation of high and low current devices while also allowing SMBus devices to communicate during the S3 state. Keeping non-essential devices on the core supply minimizes VCC_SUSPEND leakage. This is accomplished by the use of a "FET" to isolate the devices powered by the core and suspend supplies. See Figure 87.

Figure 87. High Power/Low Power Mixed $V_{CC_SUSPEND}$/V_{CC_CORE} Architecture



1. The bus switch must be powered by $V_{CC_SUSPEND}$.
2. Devices that are powered by the $V_{CC_SUSPEND}$ well must not drive into other devices that are powered off. This is accomplished with the "bus switch".
3. The bus bridge can be a device like the Phillips* PCA9515.

10.6.1.4. Calculating the Physical Segment Pull-Up Resistor

The following tables are provided as a reference for calculating the value of the pull-up resistor that may be used for a physical bus segment. If any physical bus segment exceeds 400 pF, then a bus bridge device like the Phillips* PCA9515 must be used to separate the physical segment into two segments that individually have a bus capacitance less than 400 pF.

Table 71. Bus Capacitance Reference Chart

Device	# of Devices/ Trace Length	Capacitance Includes	Cap (pF)
ICH4-M	1	Pin Capacitance	12
CK408	1	Pin Capacitance	10
SO-DIMMS	2	Pin Capacitance (10 pF) + 1 inch worth of trace capacitance (2 pF/inch) per SO-DIMM and 2 pF connector capacitance per SO-DIMM	28
	3		42
PCI Slots	2	Each PCI add-in card is allowed up to 40 pF + 3 pF per each connector	86
	3		129
	4		172
	5		215
	6		258
Bus Trace Length in inches	≥24	2 pF per inch of trace length	48
	≥36		72
	≥48		96

Table 72. Bus Capacitance/Pull-Up Resistor Relationship

Physical Bus Segment Capacitance	Pull-Up Range (For Vcc = 3.3 V
0 to 100 pF	8.2 kΩ to 1.2 kΩ
100 to 200 pF	4.7 kΩ to 1.2 kΩ
200 to 300 pF	3.3 kΩ to 1.2 kΩ
300 to 400 pF	2.2 kΩ to 1.2 kΩ

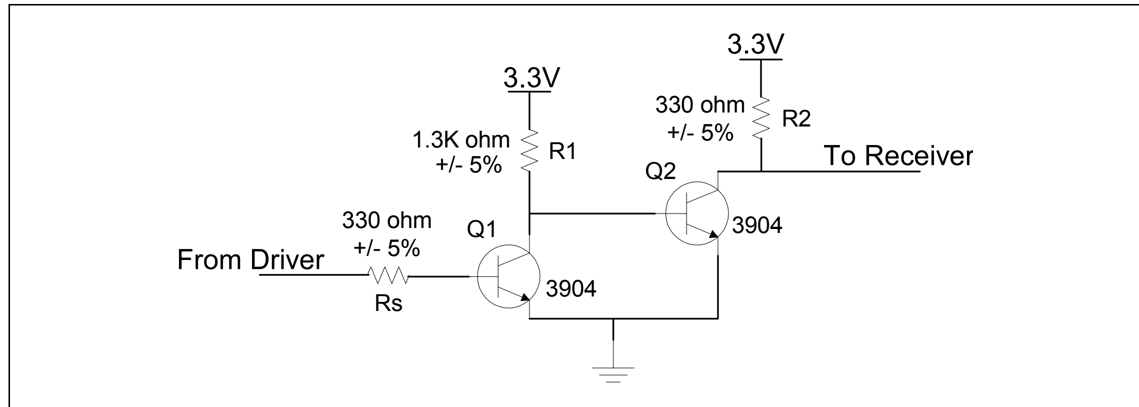
10.7. FWH

The following provides general guidelines for compatibility and design recommendations for supporting the FWH device. The majority of the changes will be incorporated in the BIOS. Refer to the *FWH Datasheet* or equivalent.

10.7.1. FWH Decoupling

Place a 0.1-µF capacitor between the V_{CC} supply pins and the V_{SS} ground pins to decouple high frequency noise, which may affect the programmability of the device. Additionally, place a 4.7-µF capacitor between the V_{CC} supply pins and the V_{SS} ground pins to decouple low frequency noise. The capacitors should be placed no further than 390 mils from the V_{CC} supply pins.

Figure 88. Voltage Translation Circuit for 3.3-V Receivers



10.7.2. In Circuit FWH Programming

All cycles destined for the FWH will appear on PCI. The ICH4-M hub interface to PCI Bridge will put all CPU boot cycles out on PCI (before sending them out on the FWH interface). If the ICH4-M is set for subtractive decode, these boot cycles can be accepted by a positive decode agent on the PCI bus. This enables the ability to boot from a PCI card that positively decodes these memory cycles. In order to boot from a PCI card, it is necessary to keep the ICH4-M in subtractive decode mode. If a PCI boot card is inserted and the ICH4-M is programmed for positive decode, there will be two devices positively decoding the same cycle.

10.7.3. FWH INIT# Voltage Compatibility

The FWH INIT# signal trip points need to be considered because they are NOT consistent among different FWH manufacturers. The INIT# signal is active low. Therefore, the inactive state of the Intel ICH4-M INIT# signal needs to be at a value slightly higher than the V_{IH} min FWH INIT# pin specification. The inactive state of this signal is typically governed by the formula V_CPU_IO(min) – noise margin. Therefore if the V_CPU_IO(min) of the processor is 1.60 V, the noise margin is 200 mV and the V_{IH} min spec of the FWH INIT# input signal is 1.35 V, there would be no compatibility issue because 1.6 V - 0.2 V = 1.40 V which is greater than the 1.35 V minimum of the FWH. If the V_{IH} min of the FWH was 1.45 V, then there would be an incompatibility and logic translation would need to be used. The examples above do not take into account any noise that may be encountered on the INIT# signal. Care must be taken to ensure that the V_{IH} min specification is met with ample noise margin. In applications where it is necessary to use translation logic, refer to Section 4.3.4.7.

The solution assumes that level translation is necessary. The Figure 16 implements a UP topology solution for the Intel Pentium 4 processor-M / Mobile Intel Celeron processor and Intel ICH4-M FWH signal INIT#. Trace lengths and resistor values can be found in

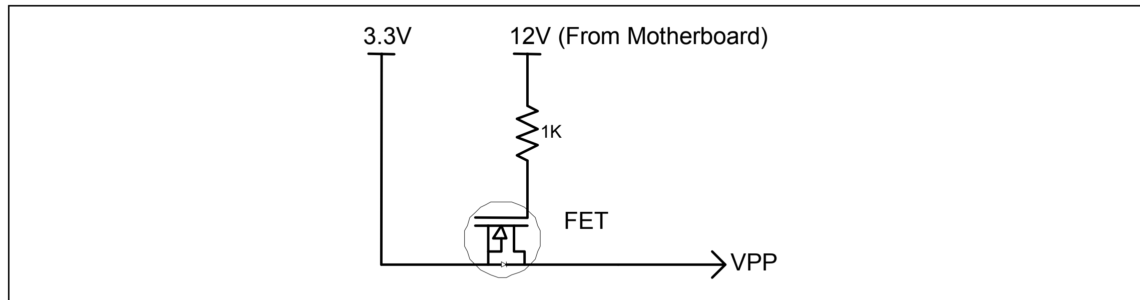
Table 11. The Voltage Translator circuitry is shown in Figure 17. Figure 29 implements a UP topology solution for the Intel Celeron M processor and Intel ICH4-M FWH signal INIT#. Trace lengths and resistor values can be found in Table 27. The Voltage Translator circuitry is shown in Figure 30.

10.7.4. FWH V_{PP} Design Guidelines

The V_{PP} pin on the FWH is used for programming the flash cells. The FWH supports V_{PP} of 3.3 V or 12 V. If $_{PP}$ is 12 V, the flash cells will program about 50% faster than at 3.3 V. However, the FWH only supports 12 V V_{PP} for 80 hours (3.3 V on Vpp does not affect the life of the device). The 12 V V_{PP} would be useful in a programmer environment, which is typically an event that occurs very infrequently (much less than 80 hours). The V_{PP} pin MUST be tied to 3.3 V on the motherboard.

In some instances, it is desirable to program the FWH during assembly with the device soldered down on the board. In order to decrease programming time it becomes necessary to apply 12 V to the V_{PP} pin. The following circuit will allow testers to put 12 V on the V_{PP} pin while keeping this voltage separated from the 3.3-V plane to which the rest of the power pins are connected. This circuit also allows the board to operate with 3.3 V on this pin during normal operation.

Figure 89. FWH VPP Isolation Circuitry

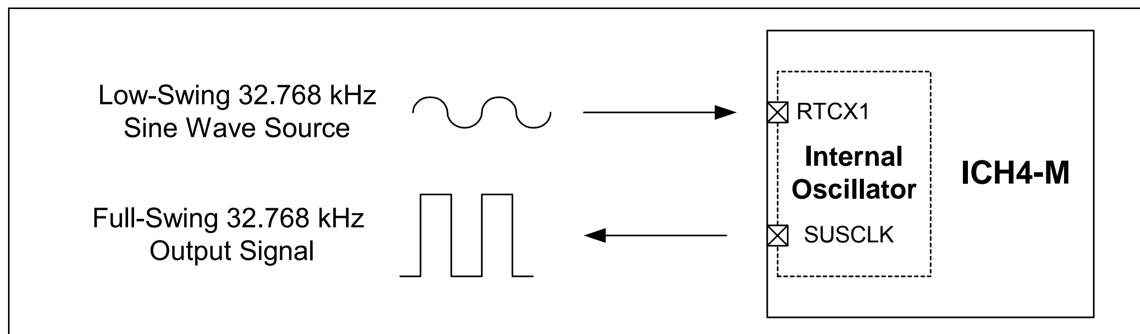


10.8. RTC

The ICH4-M contains a real time clock (RTC) with 256 bytes of battery backed SRAM. The internal RTC module provides two key functions: keeping date and time and storing system data in its RAM when the system is powered down.

The ICH4-M uses a crystal circuit to generate a low-swing, 32-kHz input sine wave. This input is amplified and driven back to the crystal circuit via the RTCX2 signal. Internal to the ICH4-M, the RTCX1 signal is amplified to drive internal logic as well as generate a free running full swing clock output for system use. This output ball of the ICH4-M is called SUSCLK. This is illustrated in Figure 90.

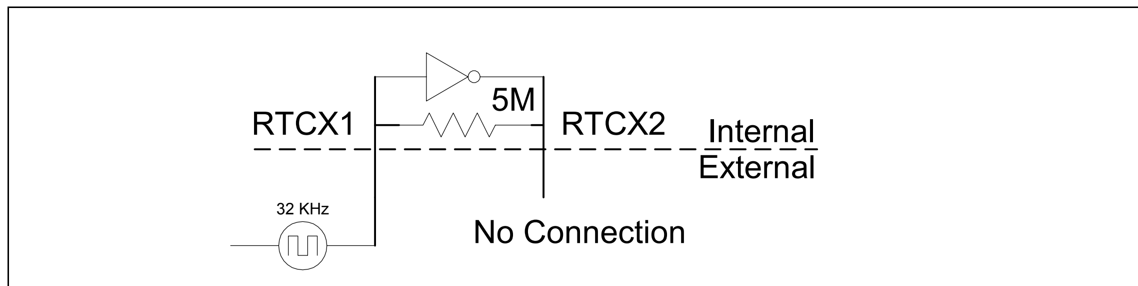
Figure 90. RTCX1 and SUSCLK Relationship in ICH4-M



For further information on the RTC, please consult Application Note AP-728 *ICH Family Real Time Clock (RTC) Accuracy and Considerations Under Test Conditions*. This application note is valid for the ICH4-M.

Even if the ICH4-M internal RTC is not used, it is still necessary to supply a clock input to RTCX1 of the ICH4-M because other signals are gated off that clock in suspend modes. However, in this case, the frequency accuracy (32.768 kHz) of the clock inputs is not critical; a single clock input can be driven into RTCX1with RTCX2 left as no connect; Figure 91 illustrates the connection. **This is not a validated feature on the ICH4-M. Please note that the peak-to-peak swing on RTCX1 cannot exceed 1.0 V.**

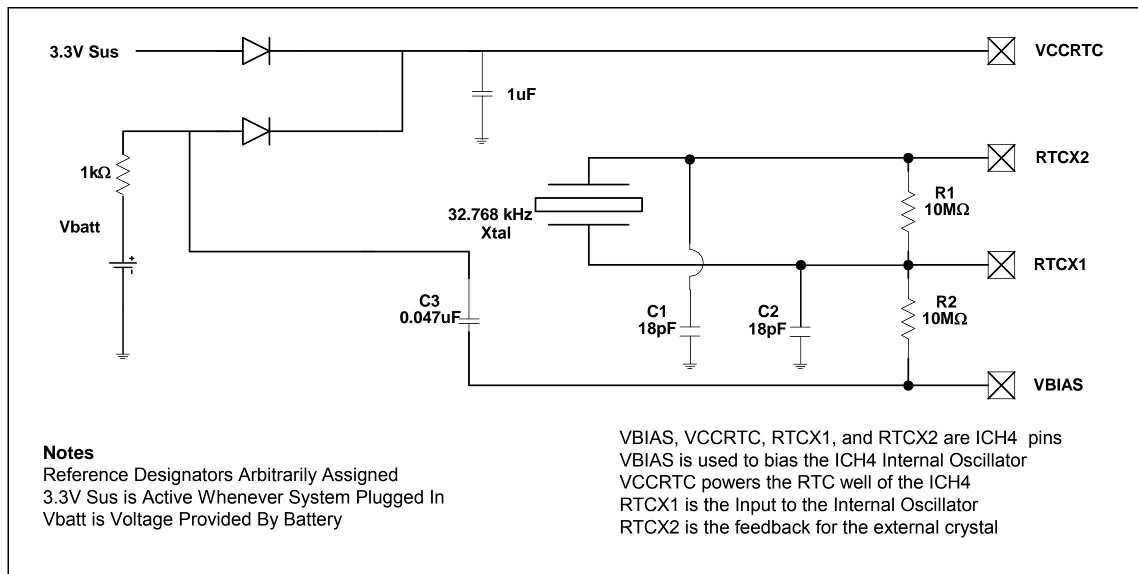
Figure 91. External Circuitry for the ICH4-M Where the Internal RTC Is Not Used



10.8.1. RTC Crystal

The ICH4-M RTC module requires an external crstal oscillating source of 32.768 kHz connected on the RTCX1 and RTCX2 balls. Figure 92 documents the external circuitry that comprises the oscillator of the ICH4-M RTC.

Figure 92. External Circuitry for the ICH4-M RTC



NOTES:

1. The exact capacitor value needs to be based on what the crystal maker recommends. (Typical values for C1 and C2 are 18 pF, based on crystal load of 12.5 pF).
2. V_{CCRTC}: Power for RTC Well
3. RTCX2: Crystal Input 2 – Connected to the 32.7 68-kHz crystal.
4. RTCX1: Crystal Input 1 – Connected to the 32.7 68-kHz crystal.

5. V_{BIAS}: RTC BIAS Voltage – This ball is used to provide a reference voltage and this DC voltage sets a current, which is mirrored throughout the oscillator and buffer circuitry.
6. V_{SS}: Ground

Table 73. RTC Routing Summary

RTC Routing Requirements	Maximum Trace Length To Crystal	Signal Length Matching	R1, R2, C1, and C2 tolerances	Signal Referencing
5 mil trace width (results in ~2 pF per inch)	1 inch	NA	R1 = R2 = 10 MΩ ± 5% C1 = C2 = (NPO class) See Section 10.8.2 for calculating a specific capacitance value for C1 and C2.	Ground

10.8.2. External Capacitors

To maintain the RTC accuracy, the external capacitor C_3 needs to be 0.047 µF and capacitor values C_1 and C_2 should be chosen to provide the manufacturer's specified load capacitance (C_{load}) for the crystal when combined with the parasitic capacitance of the trace, socket (if used), and package. The following equation can be used to choose the external capacitance values:

$$C_{load} = [(C_1 + C_{in1} + C_{trace1})*(C_2 + C_{in2} + C_{trace2})]/[(C_1 + C_{in1} + C_{trace1} + C_2 + C_{in2} + C_{trace2})] + C_{parasitic}$$

Where:

- C_{load} = Crystal's load capacitance. This value can be obtained from Crystal's specification.
- C_{in1}, C_{in2} = input capacitances at RTCX1, RTCX2 balls of the ICH4-M. These values can be obtained in the *Intel® 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)I/O Controller Datasheet.*
- C_{trace1}, C_{trace2} = Trace length capacitances measured from Crystal terminals to RTCX1, RTCX2 balls. These values depend on the characteristics of board material, the width of signal traces and the length of the traces. A typical value, based on a 5 mil wide trace and a ½ ounce copper pour, is approximately equal to :
$$C_{trace} = \text{trace length} * 2\ \text{pF/inch}$$
- $C_{parasitic}$ = Crystal's parasitic capacitance. This capacitance is created by the existence of two electrode plates and the dielectric constant of the crystal blank inside the Crystal part. Refer to the crystal's specification to obtain this value.

Ideally, C_1, C_2 can be chosen such that $C_1 = C_2$. Using the equation of C_{load} above, the value of C_1, C_2 can be calculated to give the best accuracy (closest to 32.768 kHz) of the RTC circuit at room temperature. However, C_2 can be chosen such that $C_2 > C_1$. Then C_1 can be trimmed to obtain the 32.768 kHz.

In certain conditions, both C_1, C_2 values can be shifted away from the **theoretical values** (calculated values from the above equation) to obtain the closest oscillation frequency to 32.768 kHz. When C_1, C_2 values are smaller then the theoretical values, the RTC oscillation frequency will be higher.

The following example will illustrates the use of the practical values C_1, C_2 in the case that theoretical values cannot guarantee the accuracy of the RTC in low temperature condition:

Example 1:

According to a required 12-pF load capacitance of a typical crystal that is used with the ICH4-M, the calculated values of $C_1 = C_2$ is 10 pF at room temperature (25°C) to yield a 32.768-kHz oscillation.

At 0°C the frequency stability of crystal gives – 23 ppm (assumed that the circuit has 0 ppm at 25°C). This makes the RTC circuit oscillate at 32.767246 kHz instead of 32.768 kHz.

If the values of C_1, C_2 are chosen to be 6.8 pF instead of 10 pF, the RTC will oscillate at a higher frequency at room temperature (+23 ppm) but this configuration of C_1 / C_2 makes the circuit oscillate closer to 32.768 kHz at 0°C. The 6.8-pF value of C1 and 2 is the **practical value**.

Note that the temperature dependency of crystal frequency is a parabolic relationship (ppm / degree square). The effect of changing the crystal's frequency when operating at 0°C (25°C below room temperature) is the same when operating at 50°C (25°C above room temperature).

10.8.3. RTC Layout Considerations

Since the RTC circuit is very sensitive and requires high accuracy oscillation, reasonable care must be taken during layout and routing of the RTC circuit. Some recommendations are:

1. Reduce trace capacitance by minimizing the RTC trace length. ICH4-M requires a trace length less than 1 inch on each branch (from crystal's terminal to RTCXn ball). Routing the RTC circuit should be kept simple to simplify the trace length measurement and increase accuracy on calculating trace capacitances. Trace capacitance depends on the trace width and dielectric constant of the board's material. On FR-4, a 5-mil trace has approximately 2 pF per inch.
2. Trace signal coupling must be limited as much as possible by avoiding the routing of adjacent PCI signals close to RTCX1 and RTCX2, and VBIAS.
3. Ground guard plane is highly recommended.
4. The oscillator V_{CC} should be clean; use a filter, such as an RC low-pass, or a ferrite inductor.

10.8.4. RTC External Battery Connections

The RTC requires an external battery connection to maintain its functionality and its RAM while the ICH4-M is not powered by the system.

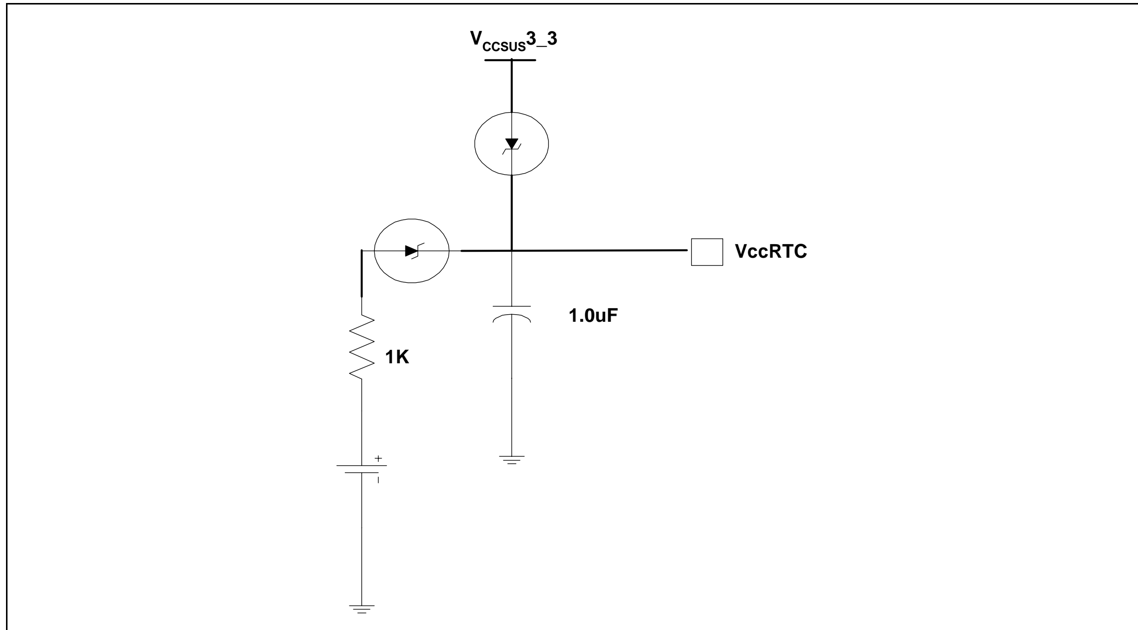
Example batteries are: Duracell* 2032, 2025, or 2016 (or equivalent), which can give many years of operation. Batteries are rated by storage capacity. The battery life can be calculated by dividing the capacity by the average current required. For example, if the battery storage capacity is 170 mAh (assumed usable) and the average current required is 5 µA, the battery life will be at least:

$$170{,}000\ \mu Ah / 5\ \mu A = 34{,}000\ h = 3.9\ years$$

The voltage of the battery can affect the RTC accuracy. In general, when the battery voltage decays, the RTC accuracy also decreases. High accuracy can be obtained when the RTC voltage is in the range of 3.0 V to 3.3 V.

The battery must be connected to the ICH4-M via a Schottky diode circuit for isolation. The Schottky diode circuit allows the ICH4-M RTC-well to be powered by the battery when the system power is not available, but by the system power when it is available. To do this, the diodes are set to be reverse biased when the system power is not available. Figure 93 is an example of a diode circuit that is used.

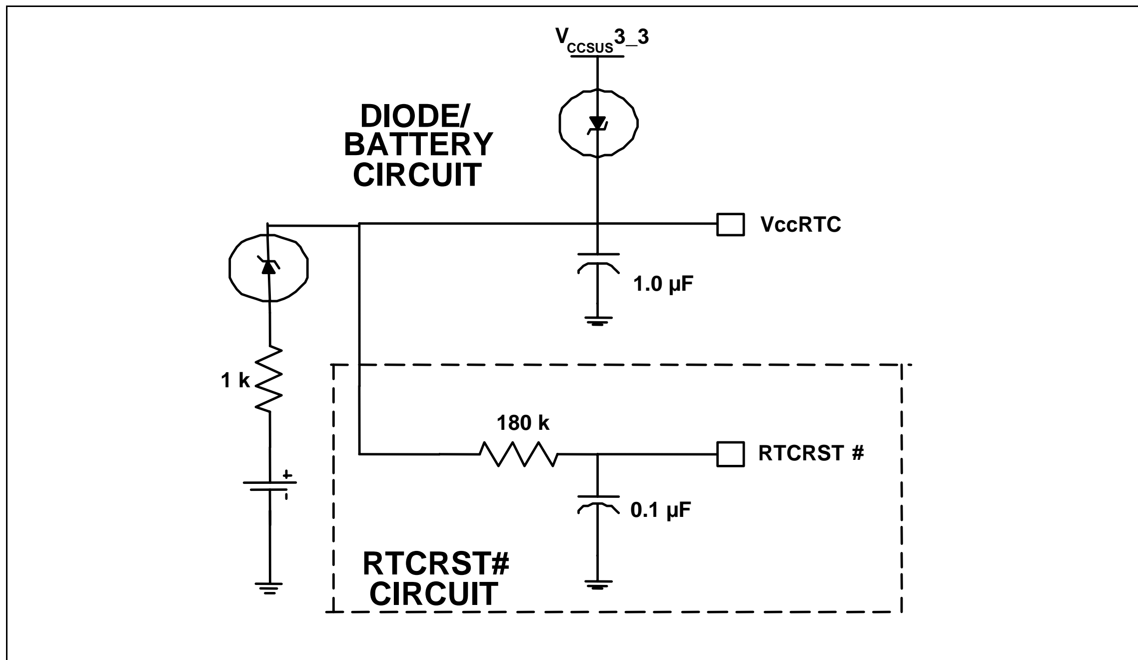
Figure 93. Diode Circuit to Connect RTC External Battery



A standby power supply should be used in a mobile system to provide continuous power to the RTC when available, which will significantly increase the RTC battery life and thereby the RTC accuracy.

10.8.5. RTC External RTCRST# Circuit

Figure 94. RTCRST# External Circuit for the ICH4-M RTC



The ICH4-M RTC requires some additional external circuitry. The RTCRST# signal is used to reset the RTC well. The external capacitor and the external resistor between RTCRST# and the RTC battery (VBAT) were selected to create an RC time delay, such that RTCRST# will go high some time after the battery voltage is valid. The RC time delay should be in the range of 18 ms - 25 ms. Any resistor and capacitor combination that yields a time constant is acceptable. When RTCRST# is asserted, bit 2 (RTC_PWR_STS) in the GEN_PMCON_3 (General PM Configuration 3) register is set to 1, and remains set until software clears it. As a result, when the system boots the BIOS knows that the RTC battery has been removed.

This RTCRST# circuit is combined with the diode circuit (shown in Figure 93) whose purpose is to allow the RTC well to be powered by the battery when the system power is not available. Figure 94 is an example of this circuitry that is used in conjunction with the external diode circuit.

10.8.6. V_{BIAS} DC Voltage and Noise Measurements

VBIAS is a DC voltage level that is necessary for biasing the RTC oscillator circuit. This DC voltage level is filtered out from the RTC oscillation signal by the RC network of R2 and C3 (see Figure 92). Therefore, it is a self-adjusting voltage. Board designers should not manually bias the voltage level on VBIAS. Checking VBIAS level is used for testing purposes only to determine the right bias condition of the RTC circuit.

VBIAS should be at least 200 mV DC. The RC network of R2 and C3 will filter out most of AC signal noise that exists on this ball. However, the noise on this ball should be kept minimal in order to guarantee the stability of the RTC oscillation.

Probing VBIAS requires the same technique as probing the RTCX1, RTCX2 signals (using Op-Amp). See *Application Note AP-728* for further details on measuring techniques.

Note: VBIAS is also very sensitive to environmental conditions.

10.8.7. SUSCLK

SUSCLK is a square waveform signal output from the RTC oscillation circuit. Depending on the quality of the oscillation signal on RTCX1 (largest voltage swing), SUSCLK duty cycle can be between 30-70%. If the SUSCLK duty cycle is beyond 30-70% range, it indicates a poor oscillation signal on RTCX1 and RTCX2.

SUSCLK can be probed directly using normal probe (50-Ω input impedance probe) and it is an appropriated signal to check the RTC frequency to determine the accuracy of the ICH4-M's RTC Clock (see *Application Note AP-728* for further details).

10.8.8. RTC-Well Input Strap Requirements

All RTC-well inputs (RSMRST#, RTCRST#, INTRUDER#) must be either pulled up to V_{CC}RTC or pulled-down to ground while in the G3 state. RTCRST# when configured as shown in Figure 94 meets this requirement. RSMRST# should have a weak external pull-down to ground and INTRUDER# should have a weak external pull-up to V_{CC}RTC. This will prevent these nodes from floating in G3, and correspondingly will prevent I_{CC}RTC leakage that can cause excessive coin-cell drain. The PWROK input signal should also be configured with an external weak pull-down.

10.9. Internal LAN Layout Guidelines

The ICH4-M provides several options for LAN capability. The platform supports several components depending upon the target market. Available LAN components include the Intel® 82562ET, and Intel® 82562EM Platform LAN Connect components.

Table 74. LAN Component Connections/Features

LAN Component	Interface to ICH4-M	Connection	Features
Intel 82562EM (48 Pin SSOP)	LCI	Advanced 10/100 Ethernet	Ethernet 10/100 connection, Alert on LAN* (AoL)
Intel 82562ET (48 Pin SSOP)	LCI	Basic 10/100 Ethernet	Ethernet 10/100 connection

Design guidelines are provided for each required interface and connection.

Figure 95. ICH4-M/Platform LAN Connect Section

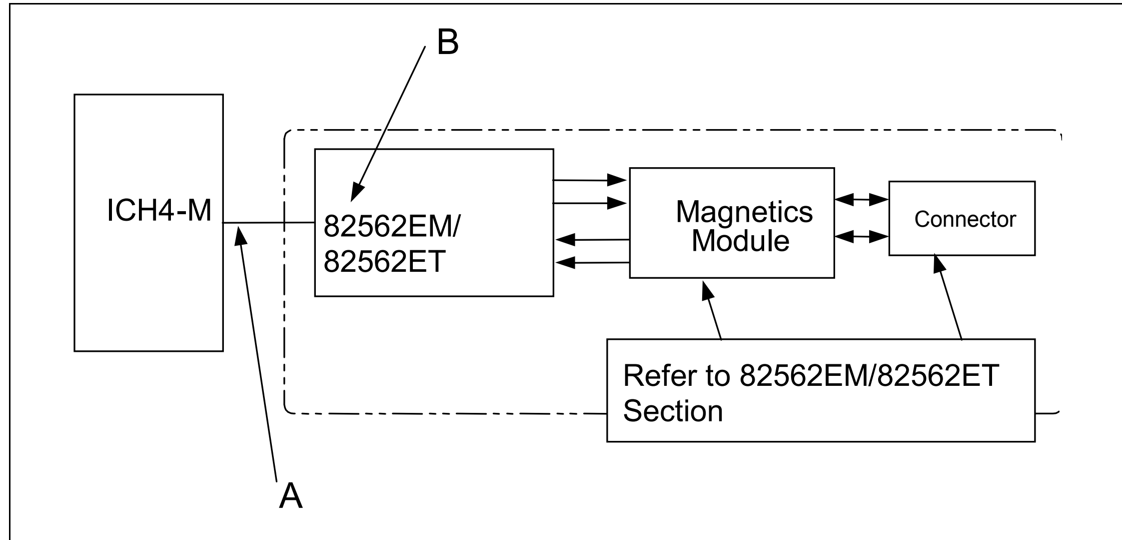


Table 75. LAN Design Guide Section Reference

Layout Section	Figure 95 Reference	Design Guide Section
ICH4-M – LAN Connect Interface (LCI)	A	Reference Section 10.9.1
Intel 82562ET / Intel 82562EM	B	Reference Section 10.9.2

10.9.1. ICH4-M – LAN Connect Interface Guidelines

This Section contains guidelines on how to implement a Platform LAN Connect device on a system motherboard. It should not be treated as a specification and the system designer must ensure through simulations or other techniques that the system meets the specified timings. Special care must be given to matching the LAN_CLK traces to those of the other signals, as shown below. The following signal lines are used on this interface and are guidelines for the ICH4-M to LAN Connect Interface.

- LAN_CLK
- LAN_RSTSYNC
- LAN_RXD[2:0]
- LAN_TXD[2:0]

This interface supports Intel 82562ET and Intel 82562EM components. Signal lines LAN_CLK, LAN_RSTSYNC, LAN_RXD[0], and LAN_TXD[0] are shared by all components.

10.9.1.1. Bus Topologies

The Platform LAN Connect Interface can be configured in several topologies:

- Direct point-to-point connection between the ICH4-M and the LAN component
- LOM Implementation

10.9.1.1.1. LOM (LAN On Motherboard) Point-To-Point Interconnect

The following are guidelines for a single solution motherboard. Either Intel 82562EM or Intel 82562ET is uniquely installed.

Figure 96. Single Solution Interconnect

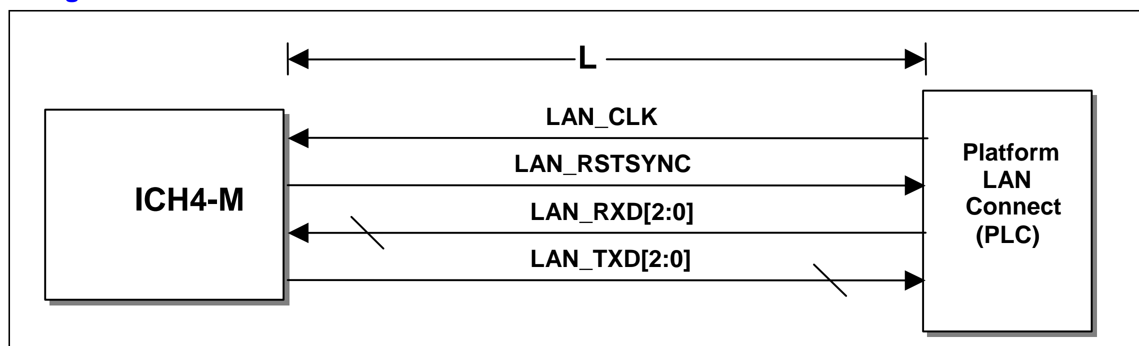


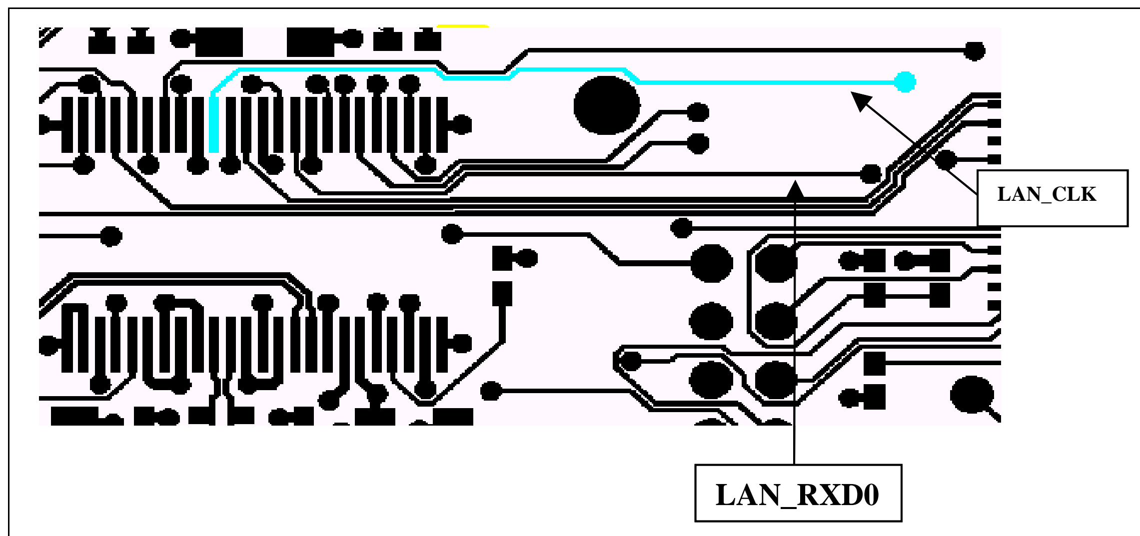
Table 76. LAN LOM Routing Summary

LAN Routing Requirements	Maximum Trace Length	Signal Referencing	LAN Signal Length Matching
5 on 10	4.5 to 12 inches	Ground	Data signals must be equal to or no more than 0.5 inches (500 mils) shorter than the LAN clock trace.

10.9.1.2. Signal Routing and Layout

Platform LAN Connect Interface signals must be carefully routed on the motherboard to meet the timing and signal quality requirements of this interface specification. The following are some general guidelines that should be followed. Intel recommends that the board designer simulate the board routing to verify that the specifications are met for flight times and skews due to trace mismatch and crosstalk. On the motherboard the length of each data trace is either equal in length to the LAN_CLK trace or up to 0.5 inches shorter than the LAN_CLK trace. (LAN_CLK should always be the longest motherboard trace in each group.)

Figure 97. LAN_CLK Routing Example



10.9.1.3. Crosstalk Consideration

Noise due to crosstalk must be carefully controlled to a minimum. Crosstalk is the key cause of timing skews and is the largest part of the t_{RMATCH} skew parameter. t_{RMATCH} is the sum of the trace length mismatch between LAN_CLK and the LAN data signals. To meet this requirement on the board, the length of each data trace is either equal to or up to 0.5 inches shorter than the LAN_CLK trace. Maintaining at least 100 mils of spacing should minimize noise due to crosstalk from non-PLC signals.

10.9.1.4. Impedances

The motherboard impedances should be controlled to minimize the impact of any mismatch between the motherboard. An impedance of 55 Ω ± 15% is strongly recommended; otherwise, signal integrity requirements may be violated.

10.9.1.5. Line Termination

Line termination mechanisms are not specified for the LAN Connect Interface. Slew rate controlled output buffers achieve acceptable signal integrity by controlling signal reflection, over/undershoot, and ringback. A 0-Ω to 33-Ω series resistor can be installed at the driver side of the interface should the developer have concerns about over/undershoot.

Note: The receiver must allow for any drive strength and board impedance characteristic within the specified ranges.

10.9.1.6. Terminating Unused LAN Connect Interface Signals

The LAN Connect Interface on the ICH4-M can be left as a no-connect if it is not used.

10.9.2. Intel 82562ET / Intel 82562 EM Guidelines

For correct LAN performance, designers must follow the general guidelines outlined in Section 10.9.1. Additional guidelines for implementing an Intel 82562ET or Intel 82562EM Platform LAN Connect component are provided below.

10.9.2.1. Guidelines for Intel 82562ET / Intel 82562EM Component Placement

Component placement can affect signal quality, emissions, and temperature of a board design. This Section will provide guidelines for component placement.

Careful component placement can:

- Decrease potential problems directly related to electromagnetic interference (EMI), which could cause failure to meet FCC and IEEE test specifications.
- Simplify the task of routing traces. To some extent, component orientation will affect the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces.

Minimizing the amount of space needed for the Ethernet LAN interface is important because all other interfaces will compete for physical space on a motherboard near the connector edge. As with most subsystems, the Ethernet LAN circuits need to be as close as possible to the connector. Thus, it is imperative that all designs be optimized to fit in a very small space.

10.9.2.2. Crystals and Oscillators

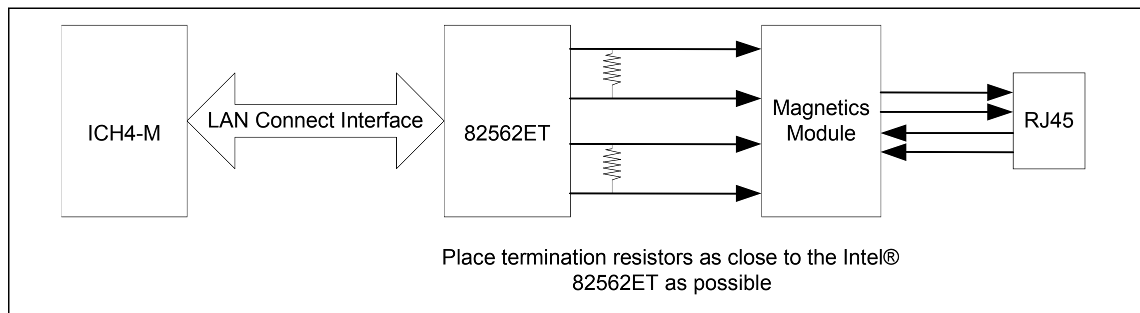
To minimize the effects of EMI, clock sources should not be placed near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis. Crystals should also be kept away from the Ethernet magnetics module to prevent interference of communication. The retaining straps of the crystal (if they should exist) should be grounded to prevent the possibility radiation from the crystal case and the crystal should lay flat against the PC board to provide better coupling of the electromagnetic fields to the board.

For a noise free and stable operation, place the crystal and associated discrete components as close as possible to the Intel 82562ET/EM, keeping the trace length as short as possible and do not route any noisy signals in this area.

10.9.2.3. Intel 82562ET / Intel 82562EM Termination Resistors

The 100 Ω ± 1% resistor used to terminate the differential transmit pairs (TDP/TDN) and the 121 Ω ± 1% receive differential pairs (RDP/RDN) should be placed as close to the Platform LAN connect component (Intel 82562ET or Intel 82562EM) as possible. This is due to the fact these resistors are terminating the entire impedance that is seen at the termination source (i.e. Intel 82562ET), including the wire impedance reflected through the transformer.

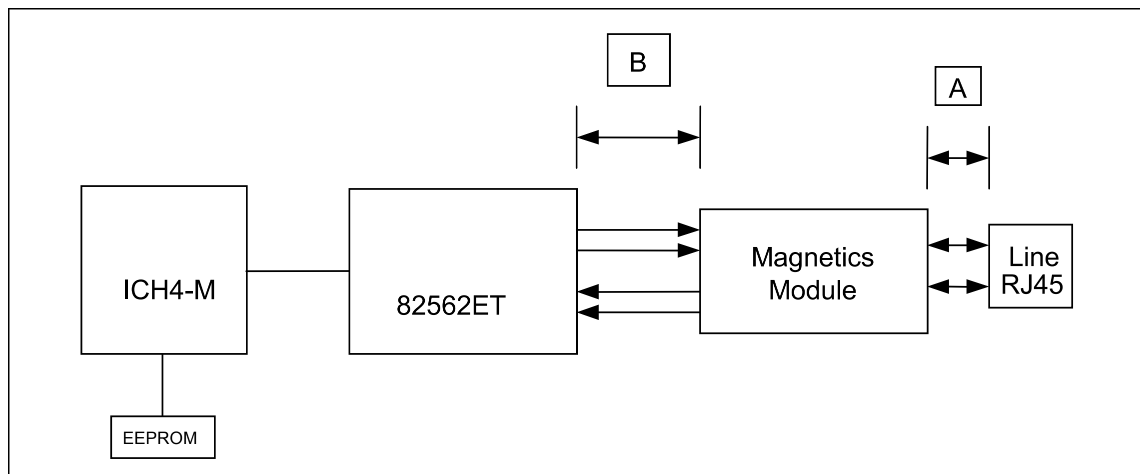
Figure 98. Intel 82562ET / Intel 82562EM Termination



10.9.2.4. Critical Dimensions

There are two dimensions to consider during layout. Distance 'A' from the line RJ-45 connector to the magnetics module and distance 'B' from the Intel 82562ET or Intel 82562EM to the magnetics module. The combined total distances A and B must not exceed 4 inches (preferably, less than 2 inches). (See Figure 99.)

Figure 99. Critical Dimensions for Component Placement



Distance	Priority	Guideline
A	1	< 1 inch
B	2	< 1 inch

10.9.2.4.1. Distance from Magnetics Module to RJ-45 (Distance A)

The distance A in Figure 99 above should be given the highest priority in board layout. The distance between the magnetics module and the RJ-45 connector should be kept to less than one inch of separation. The following trace characteristics are important and should be observed:

- Differential Impedance: The differential impedance should be 100 Ω. The single ended trace impedance will be approximately 50 Ω; however, the differential impedance can also be affected by the spacing between the traces.
- Trace Symmetry: Differential pairs (such as TDP and TDN) should be routed with consistent separation and with exactly the same lengths and physical dimensions (for example, width).

Caution: Asymmetric and unequal length traces in the differential pairs contribute to common mode noise. This can degrade the receive circuit's performance and contribute to radiated emissions from the transmit circuit. If the Intel 82562ET must be placed further than a couple of inches from the RJ-45 connector, distance B can be sacrificed. Keeping the total distance between the Intel 82562ET and RJ-45 will as short as possible should be a priority.

Note: Measured trace impedance for layout designs targeting 100 Ω often result in lower actual impedance. OEMs should verify actual trace impedance and adjust their layout accordingly. If the actual impedance is consistently low, a target of 105 Ω to 110 Ω should compensate for second order effects.

10.9.2.4.2. Distance from Intel 82562ET to Magnetics Module (Distance B)

Distance B should also be designed to be less than one inch between devices. The high-speed nature of the signals propagating through these traces requires that the distance between these components be closely observed. In general, any section of traces that is intended for use with high-speed signals should observe proper termination practices. Proper termination of signals can reduce reflections caused by impedance mismatches between device and traces. The reflections of a signal may have a high frequency component that may contribute more EMI than the original signal itself. For this reason, these traces should be designed to a 100-Ω differential value. These traces should also be symmetric and equal length within each differential pair.

10.9.2.5. Reducing Circuit Inductance

The following guidelines show how to reduce circuit inductance in both back planes and motherboards. Traces should be routed over a continuous ground plane with no interruptions. If there are vacant areas on a ground or power plane, the signal conductors should not cross the vacant area. This increases inductance and associated radiated noise levels. Noisy logic grounds should be separated from analog signal grounds to reduce coupling. Noisy logic grounds can sometimes affect sensitive DC subsystems such as analog to digital conversion, operational amplifiers, etc. All ground vias should be connected to every ground plane; and similarly, every power via, to all power planes at equal potential. This helps reduce circuit inductance. Another recommendation is to physically locate grounds to minimize the loop area between a signal path and its return path. Rise and fall times should be as slow as possible because signals with fast rise and fall times contain many high frequency harmonics that can radiate significantly. The most sensitive signal returns closest to the chassis ground should be connected

together. This will result in a smaller loop area and reduce the likelihood of crosstalk. The effect of different configurations on the amount of crosstalk can be studied using electronics modeling software.

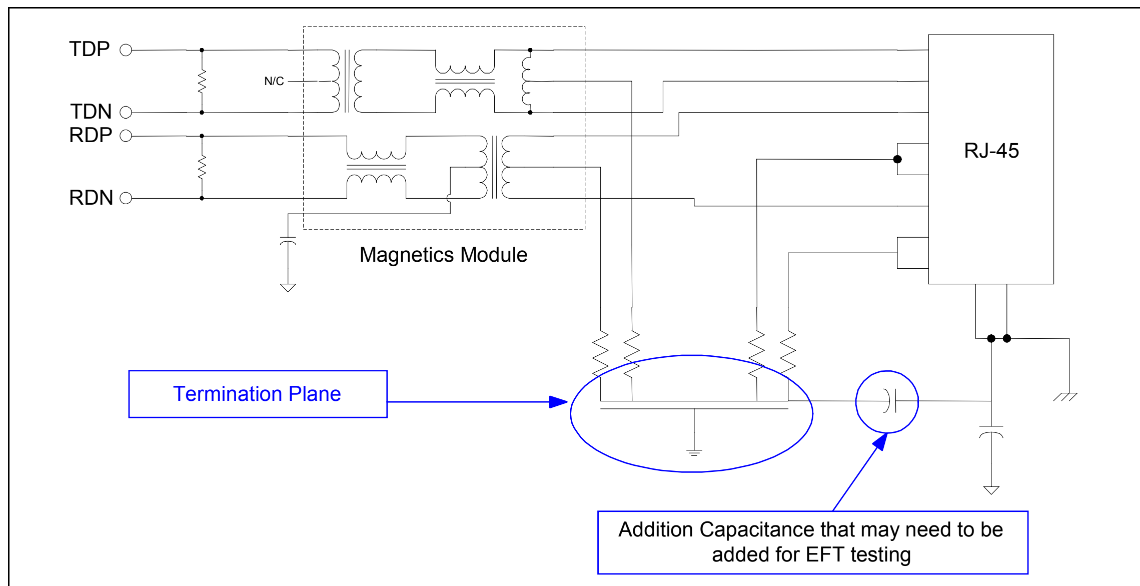
10.9.2.5.1. Terminating Unused Connections

In Ethernet designs, it is common practice to terminate unused connections on the RJ-45 connector and the magnetics module to ground. Depending on overall shielding and grounding design, this may be done to the chassis ground, signal ground, or a termination plane. Care must be taken when using various grounding methods to insure that emission requirements are met. The method most often implemented is called the "Bob Smith" Termination. In this method, a floating termination plane is cut out of a power plane layer. This floating plane acts as a plate of a capacitor with an adjacent ground plane. The signals can be routed through 75-Ω resistors to the plane. Stray energy on unused pins is then carried to the plane.

10.9.2.5.2. Termination Plane Capacitance

Intel recommends that the termination plane capacitance equals a minimum value of 1500 pF. This helps reduce the amount of crosstalk on the differential pairs (TDP/TDN and RDP/RDN) from the unused pairs of the RJ-45. Pads may be placed for an additional capacitance to chassis ground, which may be required if the termination plane capacitance is not large enough to pass EFT (Electrical Fast Transient) testing. If a discrete capacitor is used, to meet the EFT requirements it should be rated for at least 1000 Vac.

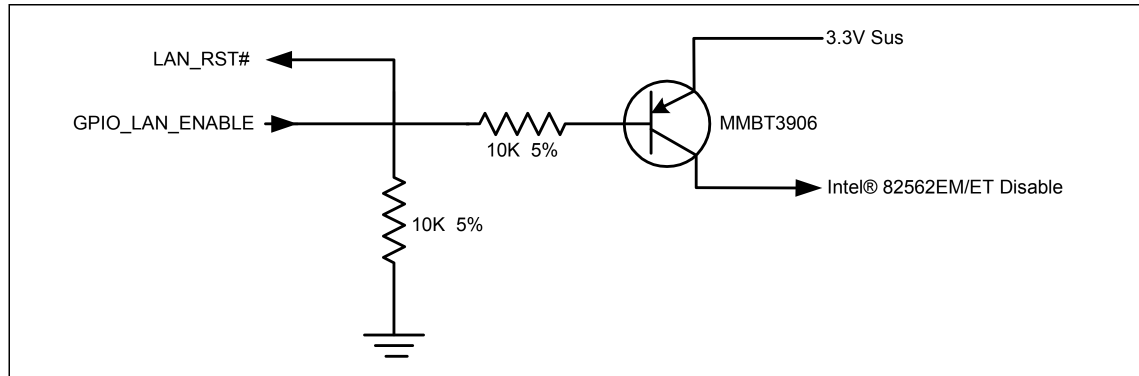
Figure 100. Termination Plane



10.9.3. Intel 82562ET/EM Disable Guidelines

To disable the Intel 82562ET/EM, the device must be isolated (disabled) prior to reset (RSM_PWROK) asserting. Using a GPIO, such as GPO28 to be LAN_Enable (enabled high), LAN will default to enabled on initial power-up and after an AC power loss. This circuit shown below will allow this behavior. The BIOS controlling the GPIO can disable the LAN micro-controller.

Figure 101. Intel 82562ET/EM Disable Circuitry



There are four pins which are used to put the Intel 82562ET/EM controller in different operating states: Test_En, Isol_Tck, Isol_Ti, and Isol_Tex. The table below describes the operational and disable features for this design.

The four control signals shown in the below table should be configured as follows: Test_En should be pulled-down through a 100-Ω resistor. The remaining three control signals should each be connected through 100-Ω series resistors to the common node "Intel 82562ET/EM _Disable" of the disable circuit.

Table 77. Intel 82562ET/EM Control Signals

Test_En	Isol_Tck	Isol_Ti	Isol_Tex	State
0	0	0	0	Enabled
0	1	1	1	Disabled w/ Clock (low power)
1	1	1	1	Disabled w/out Clock (lowest power)

In addition, if the LAN Connect Interface of the ICH4-M is not used, the VccLAN1_5 and the VccLAN3_3 are still required to be powered during normal operating states. It is acceptable to power the VccLAN1_5 and VccLAN3_3 power pins by the same switched voltage source that supplies power to the Vcc1_5 and Vcc3_3 power pins. Also, the LAN_RST# pin of the ICH4-M should be pulled-down to GND with a 10-kΩ to keep the interface disabled.

10.9.4. General Intel 82562ET/82562EM Differential Pair Trace Routing Considerations

Trace routing considerations are important to minimize the effects of crosstalk and propagation delays on sections of the board where high-speed signals exist. Signal traces should be kept as short as possible to decrease interference from other signals, including those propagated through power and ground planes.

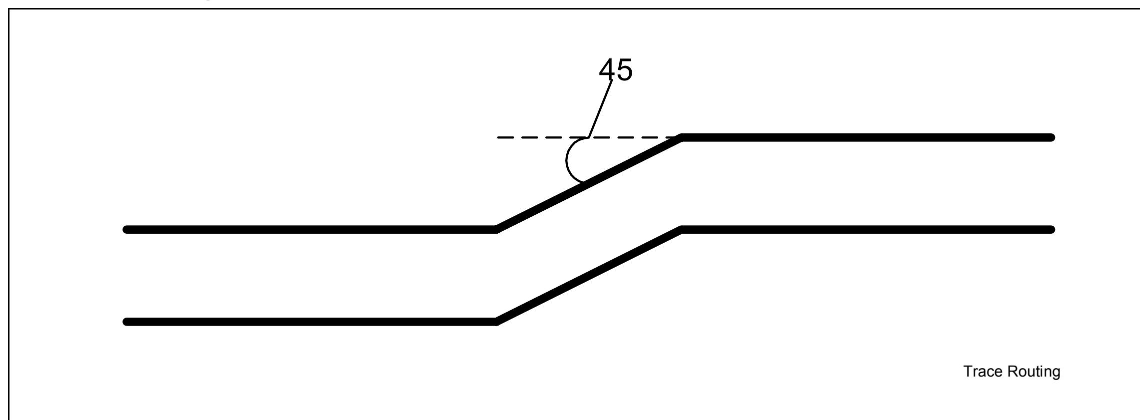
Observe the following suggestions to help optimize board performance.

Note: Some suggestions are specific to a 4.3-mil stack-up

- Maintain constant symmetry and spacing between the traces within a differential pair.
- Keep the signal trace lengths of a differential pair equal to each other.

- Keep the total length of each differential pair under 4 inches. (Many customer designs with differential traces longer than 5 inches have had one or more of the following issues: IEEE phy conformance failures, excessive EMI (Electro Magnetic Interference), and/or degraded receive BER (Bit Error Rate).)
- Do not route the transmit differential traces closer than 100 mils to the receive differential traces.
- Do not route any other signal traces both parallel to the differential traces, and closer than 100 mils to the differential traces (300 mils is recommended).
- Keep maximum separation between differential pairs to 7 mils.
- For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90° bend is required, it is recommended to use two 45° bends instead. Refer to Figure 102.
- Traces should be routed away from board edges by a distance greater than the trace height above the ground plane. This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.
- Do not route traces and vias under crystals or oscillators. This will prevent coupling to or from the clock. And as a general rule, place traces from clocks and drives at a minimum distance from apertures by a distance that is greater than the largest aperture dimension.

Figure 102. Trace Routing



10.9.4.1.1. Trace Geometry and Length

The key factors in controlling trace EMI radiation are the trace length and the ratio of trace-width to trace-height above the ground plane. To minimize trace inductance, high-speed signals and signal layers that are close to a ground or power plane should be as short and wide as practical. Ideally, this trace width to height above the ground plane ratio is between 1:1 and 3:1. To maintain trace impedance, the width of the trace should be modified when changing from one board layer to another if the two layers are not equidistant from the power or ground plane. Differential trace impedances should be controlled to be ~100 Ω. It is necessary to compensate for trace-to-trace edge coupling, which can lower the differential impedance by up to 10 Ω, when the traces within a pair are closer than 30 mils (edge to edge).

Traces between decoupling and I/O filter capacitors should be as short and wide as practical. Long and thin traces are more inductive and would reduce the intended effect of decoupling capacitors. Also for similar reasons, traces to I/O signals and signal terminations should be as short as possible. Vias to the

decoupling capacitors should be sufficiently large in diameter to decrease series inductance. Additionally, the PLC should not be closer than one inch to the connector/magnetics/edge of the board.

10.9.4.1.2. Signal Isolation

Some rules to follow for signal isolation:

- Separate and group signals by function on separate layers if possible. Maintain a gap of 100 mils between all differential pairs (Ethernet) and other nets, but group associated differential pairs together.

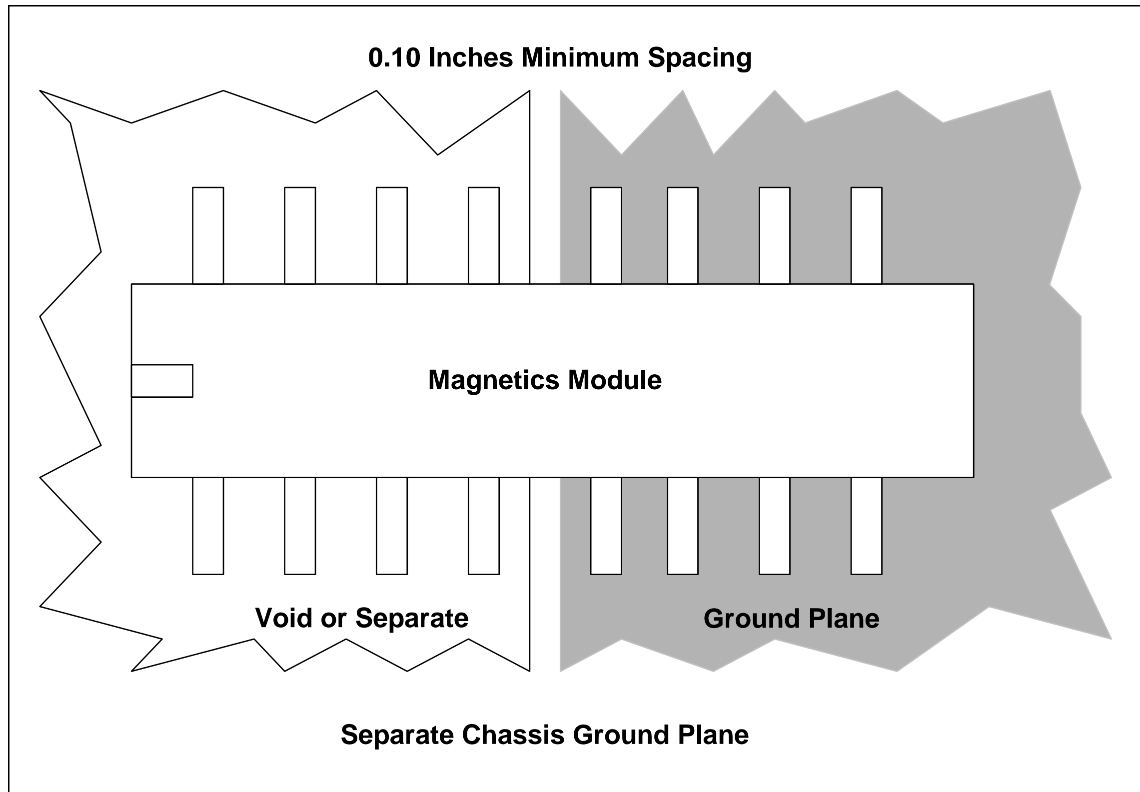
  NOTE: Over the length of the trace run, each differential pair should be at least 0.3 inches away from any parallel signal traces.

- Physically group together all components associated with one clock trace to reduce trace length and radiation.
- Isolate I/O signals from high speed signals to minimize crosstalk, which can increase EMI emission and susceptibility to EMI from other signals.
- Avoid routing high-speed LAN traces near other high-frequency signals associated with a video controller, cache controller, CPU, or other similar devices.

10.9.4.1.3. Magnetics Module General Power and Ground Plane Considerations

To properly implement the common mode choke functionality of the magnetics module the chassis or output ground (secondary side of transformer) should be separated from the digital or input ground (primary side) by a physical separation of 100-mils minimum.

Figure 103. Ground Plane Separation



Good grounding requires minimizing inductance levels in the interconnections and keeping ground returns short, signal loop areas small, and power inputs bypassed to signal return, will significantly reduce EMI radiation.

Some rules to follow that will help reduce circuit inductance in both back planes and motherboards.

- Route traces over a continuous plane with no interruptions (don't route over a split plane). If there are vacant areas on a ground or power plane, avoid routing signals over the vacant area. This will increase inductance and EMI radiation levels.
- Separate noisy digital grounds from analog grounds to reduce coupling. Noisy digital grounds may affect sensitive DC subsystems.
- All ground vias should be connected to every ground plane; and every power via should be connected to all power planes at equal potential. This helps reduce circuit inductance.
- Physically locate grounds between a signal path and its return. This will minimize the loop area.
- Avoid fast rise/fall times as much as possible. Signals with fast rise and fall times contain many high frequency harmonics, which can radiate EMI.
- The ground plane beneath the filter/transformer module should be split. The RJ-45 connector side of the transformer module should have chassis ground beneath it. By splitting ground planes beneath transformer, noise coupling between the primary and secondary sides of the transformer and between the adjacent coils in the transformer is minimized. There should not be a power plane under the magnetics module.

10.9.4.2. Common Physical Layout Issues

Here is a list of common physical layer design and layout mistakes in LAN On Motherboard Designs.

1. Unequal length of the two traces within a differential pair. Inequalities create common-mode noise and will distort the transmit or receive waveforms.
2. Lack of symmetry between the two traces within a differential pair. (Each component and/or via that one trace encounters, the other trace must encounter the same component or a via at the same distance from the PLC.) Asymmetry can create common-mode noise and distort the waveforms.
3. Excessive distance between the PLC and the magnetics or between the magnetics and the RJ-45 connector. Beyond a total distance of about 4 inches, it can become extremely difficult to design a spec-compliant LAN product. Long traces on FR4 (fiberglass epoxy substrate) will attenuate the analog signals. In addition, any impedance mismatch in the traces will be aggravated if they are longer (see #9 below). The magnetics should be as close to the connector as possible (≤ one inch).
4. Routing any other trace parallel to and close to one of the differential traces. Crosstalk getting onto the receive channel will cause degraded long cable BER. Crosstalk getting onto the transmit channel can cause excessive emissions (failing FCC) and can cause poor transmit BER on long cables. At a minimum, other signals should be kept 0.3 inches from the differential traces.
5. Routing the transmit differential traces next to the receive differential traces. The transmit trace that is closest to one of the receive traces will put more crosstalk onto the closest receive trace and can greatly degrade the receiver's BER over long cables. After exiting the PLC, the transmit traces should be kept 0.3 inches or more away from the nearest receive trace. The only possible exceptions are in the vicinities where the traces enter or exit the magnetics, the RJ-45, and the PLC.
6. Use of an inferior magnetics module. The magnetics modules that we use have been fully tested for IEEE PLC conformance, long cable BER, and for emissions and immunity. (Inferior magnetics modules often have less common-mode rejection and/or no auto transformer in the transmit channel.)
7. Use of an 82555 or 82558 physical layer schematic in a PLC design. The transmit terminations and decoupling are different. There are also differences in the receive circuit. Please follow the appropriate reference schematic or Application Note.
8. Not using (or incorrectly using) the termination circuits for the unused pins at the RJ-45 and for the wire-side center-taps of the magnetics modules. These unused RJ pins and wire-side center-taps must be correctly referenced to chassis ground via the proper value resistor and a capacitance or termplane. If these are not terminated properly, there can be emissions (FCC) problems, IEEE conformance issues, and long cable noise (BER) problems. The Application Notes have schematics that illustrate the proper termination for these unused RJ pins and the magnetics center-taps.
9. Incorrect differential trace impedances. It is important to have ~100-Ω impedance between the two traces within a differential pair. This becomes even more important as the differential traces become longer. It is very common to see customer designs that have differential trace impedances between 75 Ω and 85 Ω, even when the designers think they've designed for 100 Ω. (To calculate differential impedance, many impedance calculators only multiply the single-ended impedance by two. This does not take into account edge-to-edge capacitive coupling between the two traces. When the two traces within a differential pair are kept close[†] to each other, the edge coupling can lower the effective differential impedance by 5 Ω - 20 Ω. A 10-Ω - 15-Ω drop in impedance is common.) Short traces will have fewer problems if the differential impedance is a little off.
10. Use of a capacitor that is too large between the transmit traces and/or too much capacitance from the magnetic's transmit center-tap (on the Intel 82562ET side of the magnetics) to ground. Using capacitors more than a few pF in either of these locations can slow the 100 Mbps rise and fall time so much that they fail the IEEE rise time and fall time specs. This will also cause return loss to fail

at higher frequencies and will degrade the transmit BER performance. Caution should be exercised if a cap is put in either of these locations. If a cap is used, it should almost certainly be less than 22 pF. (6 pF to 12 pF values have been used on past designs with reasonably good success.) These caps are not necessary, unless there is some overshoot in 100-Mbps mode.

Note: It is important to keep the two traces within a differential pair close[†] to each other. Keeping them close[†] helps to make them more immune to crosstalk and other sources of common-mode noise. This also means lower emissions (i.e. FCC compliance) from the transmit traces, and better receive BER for the receive traces.

[†] Close should be considered to be less than 0.030 inches between the two traces within a differential pair. 0.007 inch trace-to-trace spacing is recommended.

10.10. Power Management Interface

10.10.1. SYS_RESET# Usage Model

The System Reset signal (SYS_RESET#) of the ICH4-M can be connected directly to a reset button or any other equivalent driver in the system where the desired effect is to immediately put the system into reset. A weak pull-up resistor pulled-up to the 3.3-V standby rail (VccSUS3_3) should be implemented to ensure that no potential floating inputs to SYS_RESET# cause a system reset. The ICH4-M will debounce signals on this pin (16 ms) and allow the SMBus to go idle before resetting the system. This delay to allow all outstanding SMBus cycles to complete first is to prevent a slave device on the SMBus from "hanging" by resetting in the middle of a SMBus cycle.

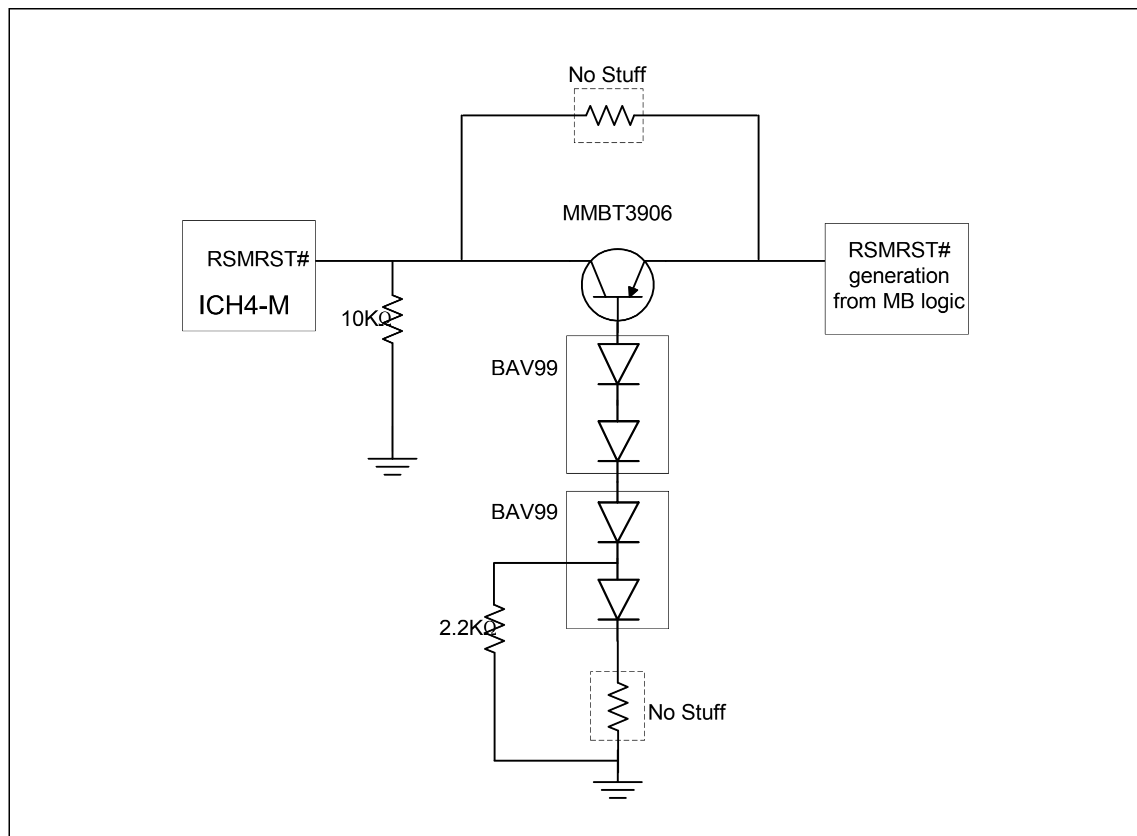
10.10.2. PWRBTN# Usage Model

The Power Button signal (PWRBTN#) of the ICH4-M can be connected directly to a power button or any other equivalent driver (e.g. power management controller) where the desired effect is to indicate a system request to go to a sleep state (if in a normal operating mode) or to cause a wake event (if in a sleep state already). This signal is internally pulled-up in the ICH4-M to the 3.3-V standby rail (VccSUS3_3) through a weak pull-up resistor (24 kΩ nominal). The ICH4-M has 16 ms of internal debounce logic on this pin.

10.10.3. Power Well Isolation Control Strap Requirements

The circuit shown in the figure below can be implemented to control well isolation between the VccSUS3_3 and RTC power wells in the event that RSMRST# is not being actively asserted during the discharge of the standby rail. Failure to implement this circuit or a circuit which functions similar to this may result in excessive droop on the VccRTC node during Sx-to-G3 power state transitions (removal of AC power and battery power). Droop on this node can potentially cause the CMOS to be cleared or corrupted, the RTC to lose time after several AC/battery power cycles, or the intruder bit might assert erroneously.

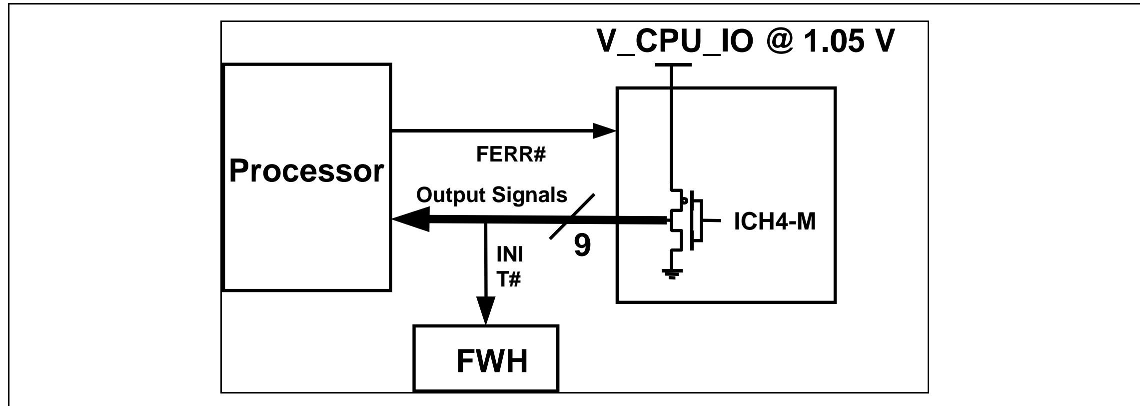
Figure 104. RTC Power Well Isolation Control



10.11. CPU CMOS Considerations

The Intel 82801DBM ICH4-M has been designed to be voltage compatible with the CMOS signals of the Intel Celeron M processor. For Intel Celeron M Processor based systems, the ICH4-M's V_CPU_IO rail uses the same 1.05-V voltage as the V_{CCP} rails for the processor the GMCH. It is important to verify that the voltage requirements of all CPU and ICH4-M signals are compatible with the FWH as well. See Section 10.7 for FWH details. Figure 105 shows a typical interface between the ICH4-M, CPU, and FWH. See Section 4.3.4 for recommended topologies and routing guidelines.

Figure 105. ICH4-M CPU CMOS Signals with CPU and FWH



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11. Platform Clock Routing Guidelines

11.1. System Clock Groups

The system clocks are considered as a subsystem in themselves. At the center of this subsystem is the Clock Synthesizer/Driver component. Several vendors offer suitable products, as defined in the Intel CK408 Synthesizer/Driver Specification. This device provides the set of clocks required to implement a platform level motherboard solution. Table 78 below provides a breakdown of the various individual clocks.

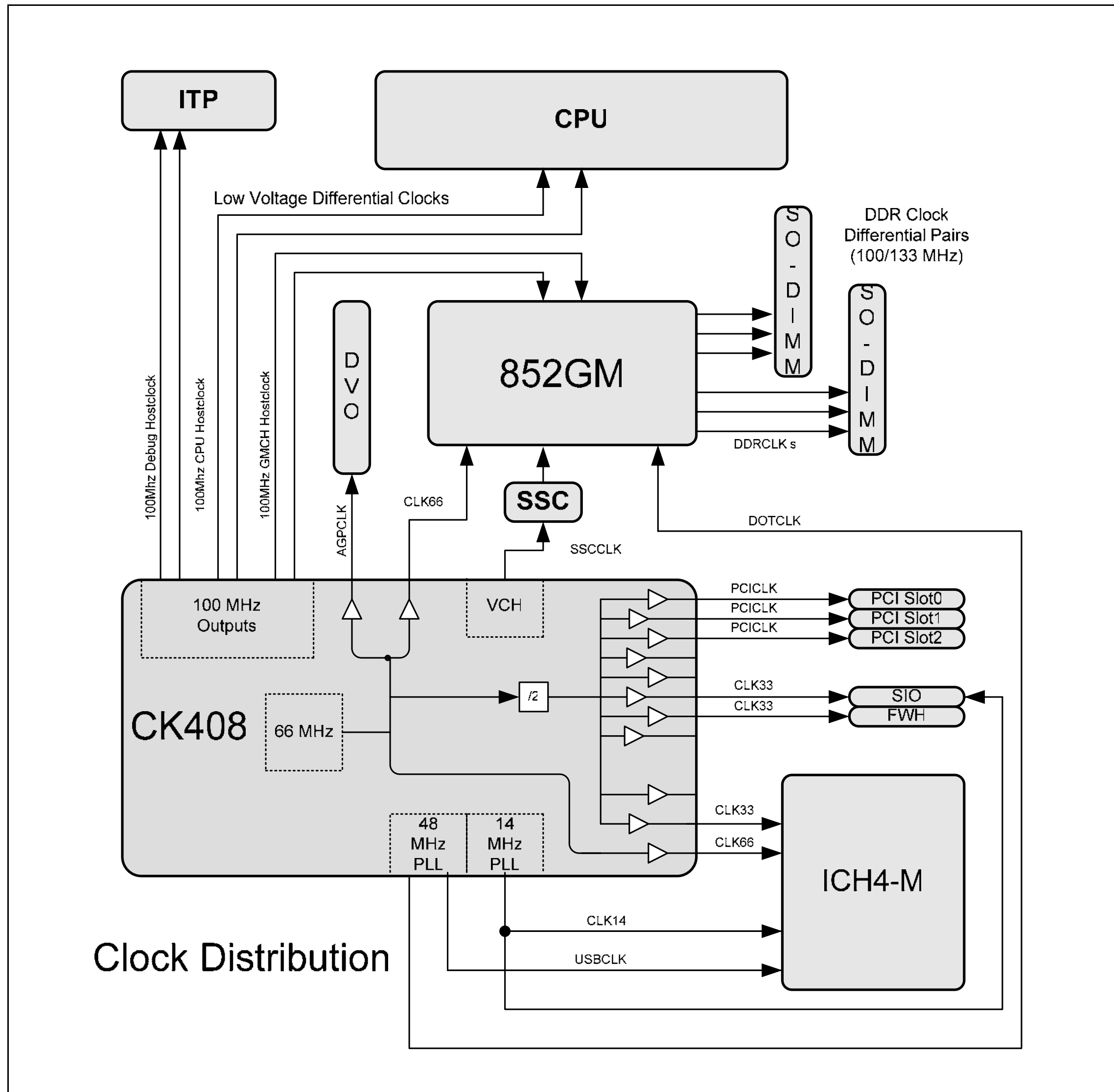
Note: When used in Intel 852GM platforms the CK408 is configured in the unbuffered mode and a host clock swing of 710 mV.

Table 78. Individual Clock Breakdown

Clock Group	Frequency	Driver/Pin	Receiver/s	Comments
HOST_CLK	100 MHz	CK408 CPU[2:0]	CPU GMCH Debug Port	Length matched Differential signaling
CLK66	66 MHz	CK408 3V66[5:0]	GMCH ICH4-M	Length matched
CLK33	33MHz	CK408 PCIF[2:0]	ICH4-M	Length matched to CLK66 Synchronous but not edge aligned with CLK66 Phase delay of 1.5 ns to 3.5 ns
	33 MHz	CK408 PCI[6:0]	SIO FWH	
PCICLK (Expansion)	33 MHz	CK408 PCI[6:0]	PCI Conn #1 PCI Conn #2 PCI Conn #3	Length matched to CLK33 * * CLK33 length minus 2.5”
CLK14	14 MHz	CK408 REF0	ICH4-M SIO	Independent clock
DOTCLK	48 MHz	CK408 48 MHz	GMCH	Independent clock
SSCCLK	48/66 MHz	CK408 VCH	GMCH	Independent clock
USBCLK	48 MHz	CK408 48 MHz	ICH4-M	Independent clock

Figure 106 below depicts the system clock subsystem including the clock generator, major platform components, all the related clock interconnects.

Figure 106. Clock Distribution Diagram



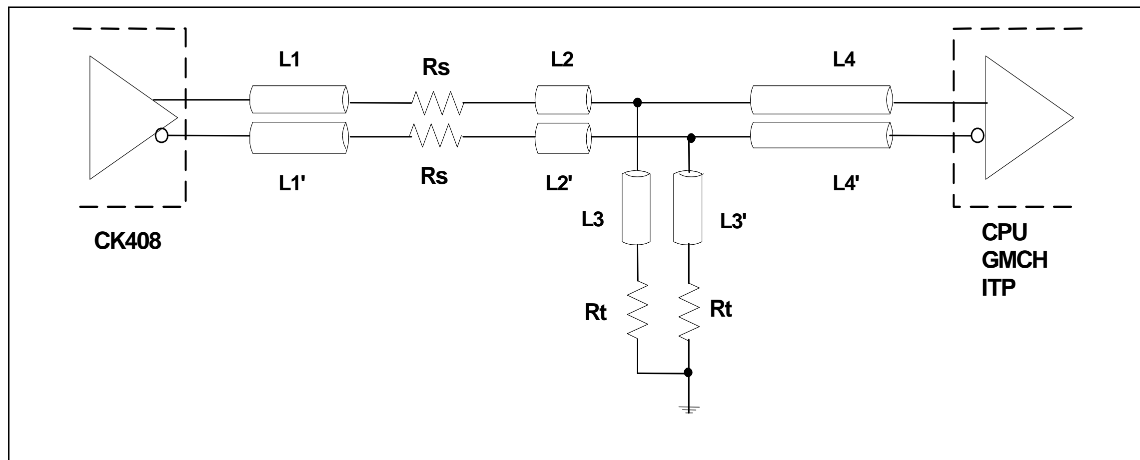
11.2. Clock Group Topologies and Routing Constraints

The topology diagrams and routing constraint tables provided on the following pages define the recommended topology and routing rules for each of the platform level clocks. These topologies and rules have been simulated and verified to produce the required waveform integrity and timing characteristics for reliable platform operation.

11.2.1. Host Clock Group

The clock synthesizer provides three pairs of 100-MHz differential clock outputs utilizing a 0.7-V voltage swing. The 100-MHz differential clocks are driven to the processor (Mobile Intel Pentium 4 Processor-M, Mobile Intel Celeron processor or Intel Celeron M processor) the GMCH, and the processor debug port with the topology shown in the figure below. The host clocks are routed point to point as closely coupled differential pairs on the motherboard, with dedicated buffers for each of the three loads. These clocks utilize a Source Shunt Termination scheme as shown below.

Figure 107. Source Shunt Termination Topology



The clock driver differential bus output structure is a "Current Mode Current Steering" output that develops a clock signal by alternately steering a programmable constant current to the external termination resistors Rt. The resulting amplitude is determined by multiplying IOUT by the value of Rt. The current IOUT is programmable by a resistor and an internal multiplication factor so the amplitude of the clock signal can be adjusted for different values of Rt to match impedances or to accommodate future load requirements.

The recommended termination for the differential bus clock is a "Source Shunt termination." Parallel Rt resistors perform a dual function, converting the current output of the clock driver to a voltage and matching the driver output impedance to the transmission line. The series resistors Rs provide isolation from the clock driver's output parasitics, which would otherwise appear in parallel with the termination resistor Rt.

The recommended value for Rt is a 49.9-Ω ±1% resistor. The tight tolerance is required to minimize crossing voltage variance. The recommended value for Rs is 33 Ω ± 5%. Simulations have shown that Rs values above 33 Ω provide no benefit to signal integrity but only degrade the edge rate.

The MULT0 pin (CK408 pin #43) should be pulled-up through a 10 kΩ to VCC – setting the multiplication factor to 6.

The IREF pin (CK408 pin #42) should be tied to ground through a 475 Ω ± 1 % resistor – making the IREF 2.32 mA.

Table 79. Host Clock Group Routing Constraints

Parameter	Definition
Class Name	HCLK
Class Type	Individual Differential Pairs
Topology	Differential Source Shunt Terminated
Reference Plane	Ground Referenced (contiguous over length)
Single Ended Trace Impedance (Zo)	55 Ω ± 15%
Differential Mode Impedance (Zdiff)	100 Ω ± 15%
Nominal Inner Layer Trace Width	4.0 mils
Nominal Inner Layer Pair Spacing (edge to edge)(except as allowed below)	7.0 mils
Nominal Outer Layer Trace Width	5.0 mils (pin escapes only)
Nominal Outer Layer Pair Spacing (edge to edge)	5.0 mils
Minimum Spacing to Other Signals	25 mils
Serpentine Spacing	25 mils
Maximum Via Count	5 (per side)
Series Termination Resistor Value	33 ohms ± 5%
Shunt Termination Resistor Value	49.9 ohms ± 1%
Trace Length Limits – L1 & L1’	Up to 500mils
Trace Length Limits – L2 & L2’	Up to 200 mils
Trace Length Limits – L3 & L3’	Up to 500 mils
Trace Length Limits – L4 & L4’	2.0” to 8.0”
Total Length Range– L1 + L2 + L4	2.0” to 8.5”
Length Matching Required	Yes (Package Compensated Pin to Pad)
HCLK to HCLKlk# Length Matching	± 10 mils (per segment) ± 10 mils (overall)
CPU Clock to GMCH Clock Length Matching	Match HCLKs (pin to pad) ± 20 mils Match L1 segment to ± 10 mils across all pairs. (See Section 11.2.1.2.)
Breakout Region Exceptions	No breakout exceptions allowed.
Clock to Clock Skew Budget (Measured at receiver crossing point)	250 ps (interconnect only) 400 ps (total skew, including 150 ps driver skew)

NOTES:

1. Differential pairs should be routed as a closely coupled side-by-side pair on a single layer over their entire length.
2. To minimize skew, Intel recommends that all clocks be routed on a single layer. If clock pairs are to be routed on multiple layers, the routed length on each layer should be equalized across all clock pairs.
3. To minimize skew, Intel recommends that all clock pairs be length matched from CK408 pin to CPU and GMCH die-pad, and length compensated on the motherboard for differences in package length and for socket/interposer effective length. A table of package lengths and equivalent socket length is provided.
4. The motherboard length of the ITP connector clock pair should be matched to the motherboard length of the CPU clock pair.

11.2.1.1. Host Clock Group General Routing Guidelines

When routing the 100-MHz differential clocks, do not split up the two halves of a differential clock pair between layers, and route to all agents on the same physical routing layer referenced to ground.

If a layer transition is required, make sure that the skew induced by the vias used to transition between routing layers is compensated in the traces to other agents.

Do not place vias between adjacent complementary clock traces. Vias placed in one half of a differential pair must be matched by a via in the other half. Differential vias can be placed within length L1, between clock driver and Rs, if needed to shorten length L1.

11.2.1.2. Clock to Clock Length Matching and Compensation

The HCLK pairs to the CPU and GMCH should be matched as close as possible in total length from CK408 pin to the die-pad of the receiving device. In addition, the L1/L1' segments of all three clock pairs should be length matched to within ± 10 mils. Pair to pair overall length matching requires knowledge of the package lengths of various CPUs, and the GMCH, as well as the effective length of the CPU socket/interposer if used. This information is provided in Table 80.

Once routing lengths are defined for the CPU and GMCH, match the motherboard length of the ITP clock pair to the motherboard length of the CPU clock pair.

Table 80. Clock Package Length

Parameter	Length
Mobile Intel Pentium 4 Processor-M / Mobile Intel Celeron Processor Package Length	596 mils
Intel Celeron M Processor Package Length	485 mils
Intel 852GM GMCH Package Length	1142 mils
CPU Socket Equivalent Length	157 mils

11.2.1.3. EMI Constraints

Clocks are a significant contributor to EMI and should be treated with care. The following recommendations can aid in EMI reduction:

- Maintain uniform spacing between the two halves of differential clocks.
- Route clocks on physical layer adjacent to the VSS reference plane only.

11.2.2. CLK66 Clock Group

The 66-MHz clocks are series terminated and routed point to point on the motherboard, with dedicated buffers for each of the loads. These clocks are all length tuned to match each other and the CLK33 clocks.

Figure 108. CLK66 Clock Group Topology

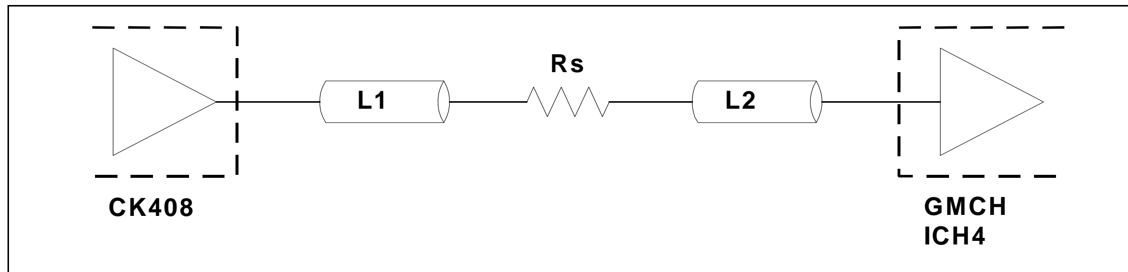


Table 81. CLK66 Clock Group Routing Constraints

Parameter	Definition
Class Name	CLK66
Class Type	Individual Nets
Topology	Series Terminated Point to Point
Reference Plane	Ground Referenced
Single Ended Trace Impedance (Zo)	55 Ω ±15%
Nominal Inner Layer Trace Width	4.0 mils
Nominal Outer Layer Trace Width	5.0 mils (pin escapes only)
Minimum Spacing (see exceptions below)	20 mils
Serpentine Spacing	20 mils
Maximum Via Count	4 (per side)
Series Termination Resistor Value	33 Ω ± 5 %
Trace Length Limits – L1	Up to 500 mils (breakout segment)
Trace Length Limits – L2	4.0” to 8.5”
Total Length Range – L1 + L2	4.0” to 9.0”
Length Matching Required	Yes (Pin to Pin)
Clock to Clock Length Matching	± 100 mils CLK66 to CLK66
Breakout Region Exceptions. (Reduced spacing for GMCH & ICH breakout region)	5 mil trace with 5 mil space on outers 4 mil trace with 4 mil space in inners Maximum breakout length is 0.3”

NOTE: The overall length of CLK66 is considered the reference length for all other clocks, except USBCLK and CLK14. The length of this clock should be set within the range and then used as the basis for defining the length of all other length matched clocks.

11.2.3. CLK33 Clock Group

The 33-MHz clocks are series terminated and routed point to point on the motherboard with dedicated buffers for each of the loads. These clocks are length tuned to match the CLK66 clocks, however, they are out of phase due to an internal phase delay in the CK408.

Figure 109. CLK33 Group Topology

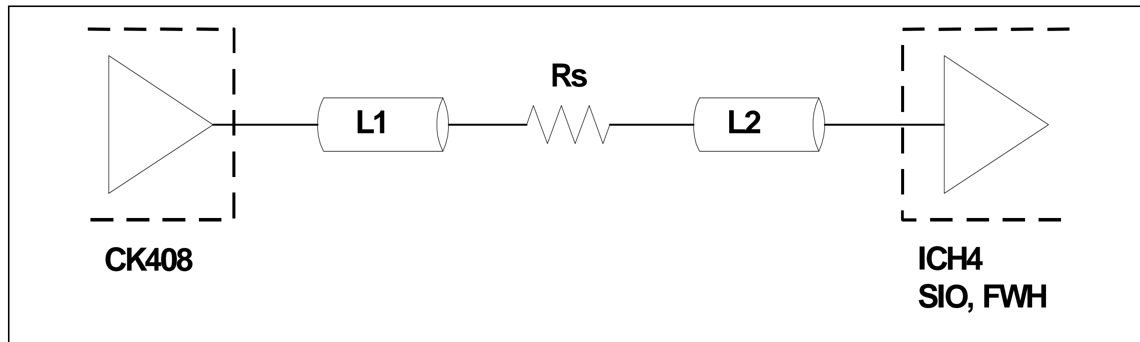


Table 82. CLK33 Clock Group Routing Constraints

Parameter	Definition
Class Name	CLK33
Class Type	Individual Nets
Topology	Series Terminated Point to Point
Reference Plane	Ground Referenced
Single Ended Trace Impedance (Zo)	55 Ω ± 15%
Nominal Inner Layer Trace Width	4.0 mils
Nominal Outer Layer Trace Width	5.0 mils (pin escapes only)
Minimum Spacing (see exceptions below))	20 mils
Serpentine Spacing	20 mils
Maximum Via Count	4
Series Termination Resistor Value	33 Ω ± 5 %
Trace Length Limits – L1	Up to 500mils
Trace Length Limits – L2	4.0” to 8.5”
Total Length Range – L1 + L2	CLK66 Length
Length Matching Required	Yes (Pin to Pin)
Clock to Clock Matching	± 100 mils CLK33 to CLK33 to CLK66
Breakout Region Exceptions	5 mil trace with 5 mil space on outers 4 mil trace with 4 mil space in inners Maximum breakout length is 0.3”

11.2.4. PCI Clock Group

The PCI clocks are series terminated and routed point to point as on the motherboard between the CK408 and the PCI connectors with dedicated buffers for of the three slots. These clocks are synchronous to the CLK33 clocks and are length tuned to compensate for the segment on the PCI daughter card.

Figure 110. PCI Clock Group Topology

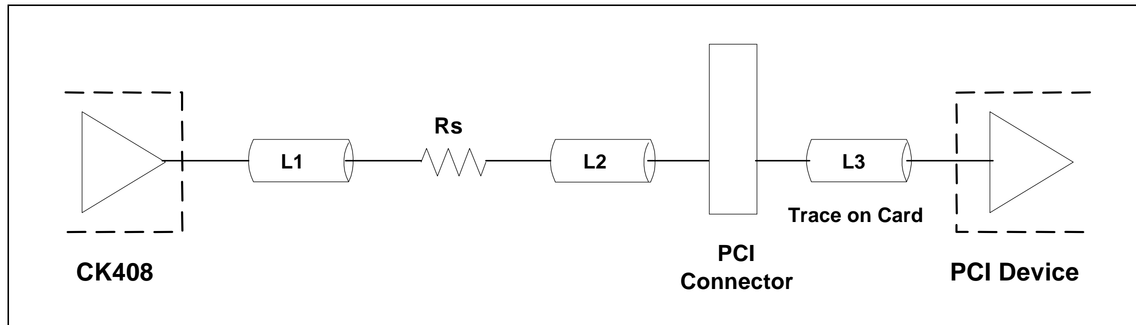


Table 83. PCICLK Clock Group Routing Constraints

Parameter	Definition
Class Name	PCICLK
Class Type	Individual Nets
Topology	Series Terminated Point to Point
Reference Plane	Ground Referenced
Single Ended Trace Impedance (Zo)	55 Ω ± 15%
Nominal Inner Layer Trace Width	4.0 mils
Nominal Outer Layer Trace Width	5.0 mils (pin escapes only)
Minimum Spacing (see exceptions below))	20 mils
Serpentine Spacing	20 mils
Maximum Via Count	4
Series Termination Resistor Value	33 Ω ± 5 %
Trace Length Limits – L1	Up to 500 mils (breakout segment)
Trace Length Limits – L2	1.5” to 8.0”
Trace Length Limits – L3	2.5” (as per PCI specification)
Total Length Range – L1 + L2 + L3	CLK33 – 2.5” (for nominal matching)
Length Matching Required	Yes (Pin to Pin)
Clock to Clock Length Matching	± 2.0” PCICLK to PCICLK to (CLK33 – 2.5”)
Breakout Region Exceptions	5 mil trace with 5 mil space on outers 4 mil trace with 4 mil space in inners Maximum breakout length is 0.3”

11.2.5. CLK14 Clock Group

The 14-MHz clocks are series terminated and routed point to point on the motherboard. A single clock output is shared between the two loads. These clocks are length tuned to each other but are not synchronous with any other clocks.

Figure 111. CLK14 Clock Group Topology

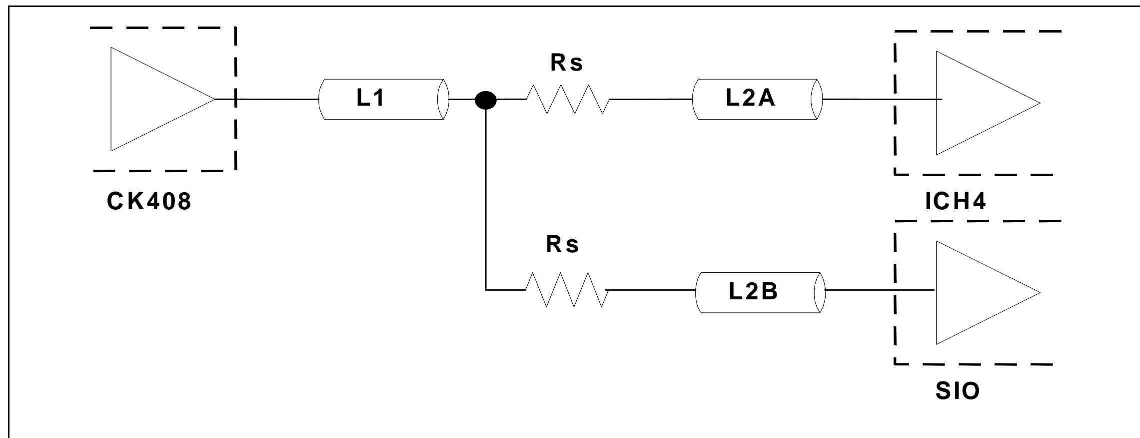


Table 84. CLK14 Clock Group Routing Constraints

Parameter	Definition
Class Name	CLK14
Class Type	Individual Nets
Topology	Dual Series Terminated Point to Point
Reference Plane	Ground Referenced
Single Ended Trace Impedance (Zo)	55 Ω ± 15%
Nominal Inner Layer Trace Width	4.0 mils
Nominal Outer Layer Trace Width	5.0 mils (pin escapes only)
Minimum Spacing (see exceptions below)	20 mils
Serpentine Spacing	20 mils
Maximum Via Count	4 (per driver/receiver path)
Series Termination Resistor Value	33 Ω ± 5 %
Trace Length Limits – L1	Up to 500 mils
Trace Length Limits – L2A, L2B	2.0” to 8.5”
Total Length Range – L1 + L2A & L1 + L2B	2.0” to 9.0”
Length Matching Required	Yes (Pin to Pin)
Clock to Clock Length Matching	± 500 mils CLK14A to CLK14B
Breakout Region Exceptions	5 mil trace with 5 mil space on outers 4 mil trace with 4 mil space in inners Maximum breakout length is 0.3”

11.2.6. DOTCLK Clock Group

The 48-MHz DOTCLK is series terminated and routed point to point on the motherboard. This clock operates independently and is not length tuned to any other clock.

Figure 112. DOTCLK Clock Topology

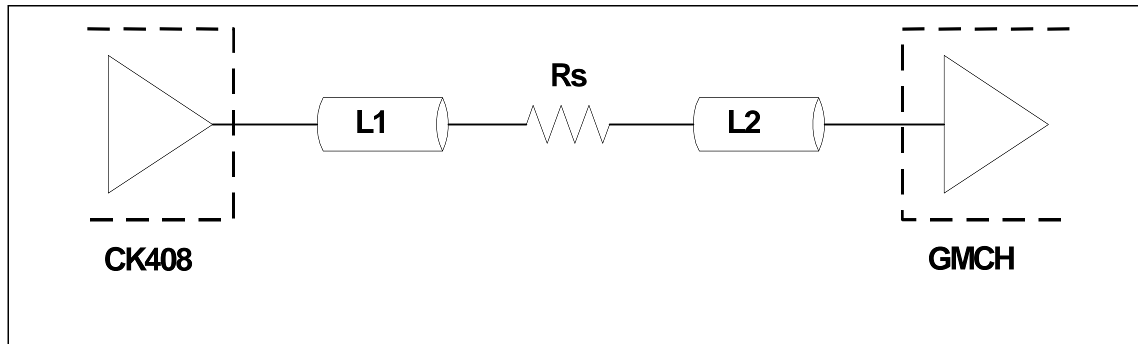


Table 85. DOTCLK Clock Routing Constraints

Parameter	Definition
Class Name	DOTCLK
Class Type	Individual Net
Topology	Series Terminated Point to Point
Reference Plane	Ground Referenced
Single Ended Trace Impedance (Zo)	55 Ω ± 15%
Nominal Inner Layer Trace Width	4.0 mils
Nominal Outer Layer Trace Width	5.0 mils (pin escapes only)
Minimum Spacing (see exceptions below)	25 mils
Maximum Via Count	4
Series Termination Resistor Value	33 Ω ± 5 %
Trace Length Limits – L1	Up to 500 mils
Trace Length Limits – L2	2.0” to 8.0”
Total Length Range – L1 + L2	2.0” to 8.5”
Length Matching Required	No
Breakout Exceptions	5 mil trace with 5 mil space on outers 4 mil trace with 4 mil space in inners Maximum breakout length is 0.3”

NOTE: The DOTCLK is used internally by the GMCH to generate the pixel clock and must exhibit very low jitter. Care should be taken to avoid routing through noisy areas and spacing rules should be observed. Guard traces may be employed if necessary with ground stake vias on no less than 0.5- inch intervals.

11.2.7. SSCCLK Clock Group

The 48/66-MHz SSCCLK operates independently and is not length tuned to any other clock. This clock employs a spread-spectrum device in its path to reduce EMI. The overall clock path is divided into two segments as shown in Figure 113, with each segment series terminated and routed point to point.

Figure 113. SSCCLK Clock Topology

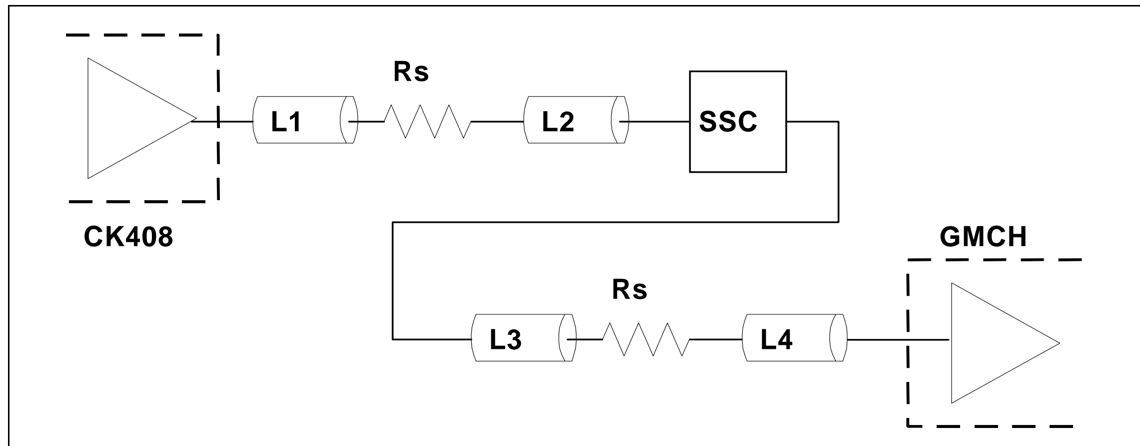


Table 86. SSCCLK Clock Routing Constraints

Parameter	Definition
Class Name	SSCCLK
Class Type	Individual Net
Topology	Series Terminated Point to Point
Reference Plane	Ground Referenced
Single Ended Trace Impedance (Zo)	55 Ω ±15%
Nominal Inner Layer Trace Width	4.0 mils
Nominal Outer Layer Trace Width	5.0 mils (pin escapes only)
Minimum Spacing (see exceptions below)	20 mils
Maximum Via Count	4 (per driver/receiver path)
Series Termination Resistor Value	33 Ω ± 5 %
Trace Length Limits – L1	Up to 500 mils
Trace Length Limits – L2	1.0” to 4.0”
Trace Length Limits – L3	Up to 500 mils
Trace Length Limits – L4	1.0” to 7.0”
Total Length Range – L1 + L2 + L3 + L4	3.0” to 8.5”
Length Matching Required	No
Breakout Exceptions	5 mil trace with 5 mil space on outers 4 mil trace with 4 mil space in inners Maximum breakout length is 0.3”

11.2.8. USBCLK Clock Group

The 48-MHz USBCLK is series terminated and routed point to point on the motherboard. This clock operates independently and is not length tuned to any other clock.

Figure 114. USBCLK Clock Topology

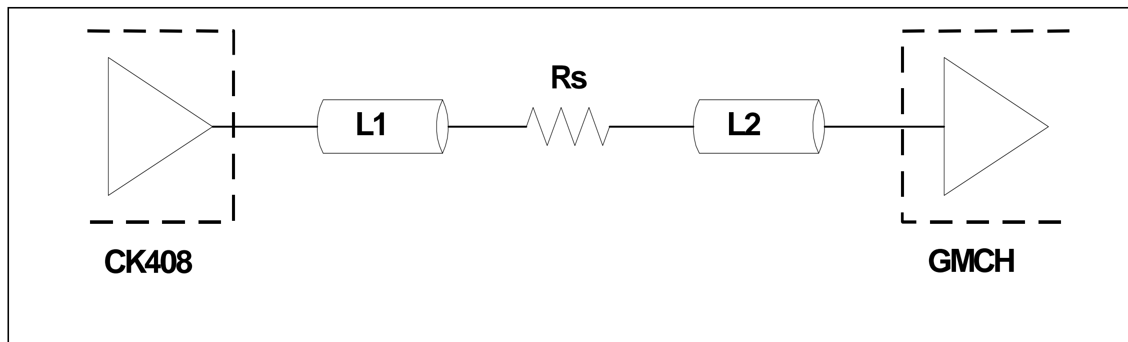


Table 87. USBCLK Clock Routing Constraints

Parameter	Definition
Class Name	USBCLK
Class Type	Individual Net
Topology	Series Terminated Point to Point
Reference Plane	Ground Referenced
Single Ended Trace Impedance (Zo)	55 Ω ± 15%
Nominal Inner Layer Trace Width	4.0 mils
Nominal Outer Layer Trace Width	5.0 mils (pin escapes only)
Minimum Spacing (see exceptions below)	20 mils
Maximum Via Count	4
Series Termination Resistor Value	33 Ω ± 5 %
Trace Length Limits – L1	Up to 500 mils
Trace Length Limits – L2	3.0” to 12.0”
Total Length Range – L1 + L2	3.0” to 12.5”
Length Matching Required	No
Breakout Exceptions	5 mil trace with 5 mil space on outers 4 mil trace with 4 mil space in inners Maximum breakout length is 0.3”

11.3. CK-408 Clock Updates for Intel Celeron M Processor Platforms

To maximize the power savings on Intel Celeron M processor / Intel 852GM Chipset based systems, additional control registers have been added to the CK-408 clock generator to allow option to tri-state the CPU[2:0] host clocks during CPU_STOP# or PWRDWN assertion. The option to have CPU[2:0] driven (default) or tri-stated can be programmed via the serial I2C bus interface to the CK-408 clock driver. If the tri-state feature on the CPU[2:0] signals is chosen, it is recommended that the STP_CPU# signal from the Intel ICH4-M drive the CK-408's CPU_STOP# signal. Also, it is recommended that the ICH4-M's DPSLP# signal be connected to the DPSLP# pin of the processor and GMCH. Functionally, the ICH4-M's STP_CPU# and DPSLP# signals are equivalent. However, STP_CPU# is powered by the main I/O well (3.3 V) and is sent to the CK-408 whereas DPSLP# is driven to the processor interface voltage (1.05 V).

11.4. CK-408 PWRDWN# Signal Connections

For systems that support the S1M state, the PWRDWN# input of the CK-408 clock chip is **required** to be driven by **both** the SLP_S1# and SLP_S3# signals from the ICH4-M, i.e. the PWRDWN# pin of the CK-408 should be driven by the output of the logical AND of the SLP_S1# and SLP_S3# signals. This configuration best allows CPU[2:0] to be tri-stated during Deep Sleep (C3), Deeper Sleep, and S1-M or lower (numerically higher) states.

For systems that do not support S1M but do support the S3 state, the PWRDWN# input of the CK-408 clock chip should be connected to the SLP_S3# output of the ICH4-M. It is **not** recommended that PWRDWN# be pulled-up to the CK-408's 3.3-V power supply if the S3 state is the second highest, power consuming state supported by the platform (i.e. S1M and S2 not supported). The advantage of using SLP_S3# rather than the 3.3-V supply to qualify PWRDWN# is that it reduces the likelihood of the CK-408 clocks driving into unpowered components and potentially damaging the clock input buffers. Also SLP_S3# can help reduce power consumption because it will be asserted before the 3.3-V supply will be shut off, thus minimizing the amount of time that the clocks will be left toggling.

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12. Intel 852GM Platform Power Delivery Guidelines

12.1. Definitions

Table 88. Power Delivery Definitions

Term	Definition
S0/Full-On operation:	In the S0 state, all components on the motherboard are powered and the system is fully functional.
S1M/Power-On-Suspend (POS, Mobile):	In the mobile implementation of the S1M state, the outputs of the clock chip are stopped in order to save power. All components remain powered but may or may not be in a low power state.
S3/Suspend-To-RAM (STR):	In the S3 state, the system state is stored in main memory and all unnecessary system logic is turned off. Only main memory and logic required to wake the system remain powered.
S4/Suspend-To-Disk (STD):	In the S4 state, the system state is stored in non-volatile secondary storage (e.g. a hard disk) and all unnecessary system logic is turned off. Only logic required to wake the system remain powered. Standby power rails may or may not be powered depending on system design and the presence of AC or battery power.
S5/Soft-Off:	The S5 state corresponds to the G2 state. Restart is only possible with the power button.
Full-Power operation:	During Full-Power operation, all components remain powered. Full-power operation includes both S0 and the S1-M (CPU Stop-Grant state).
Suspend operation:	Intel 852GM chipset-based systems can be designed to support a number of suspend states such as Power-On-Suspend (S1M), Suspend-to-RAM (S3), Suspend-to-Disk (S4), and Soft-Off (S5). During suspend operation, with exception of S1M, power is removed from some components on the motherboard.
Core power rail:	A power rail that is only on during full-power operation.
Standby power rail:	A power rail that is on during a suspend operation (S3, S4 or S5). The rail is also on during full-power operation.
Derived power rail:	A derived power rail is any power rail that is generated from another power rail using an on-board voltage regulator. For example, 3.3 V_{SB} is usually derived (on the motherboard) from 5 V_{SB} using a voltage regulator.

12.2. Platform Power Requirements

The following figure shows the power delivery architecture for an example of the Intel 852GM chipset platform. To ensure that enough power is available during S3, a thorough power budget should be completed. The power requirements should include each device's power requirements, S0 – S5. The power requirements should be compared against the power budget supplied by the power supply.

The solutions given in this document are only examples. There are many power distribution methods that achieve similar results. It is critical, when deviating from these examples, to consider the effect of the change.

12.2.1. Platform Power Delivery Architectural Block Diagram

Figure 115. Platform Power Delivery Map

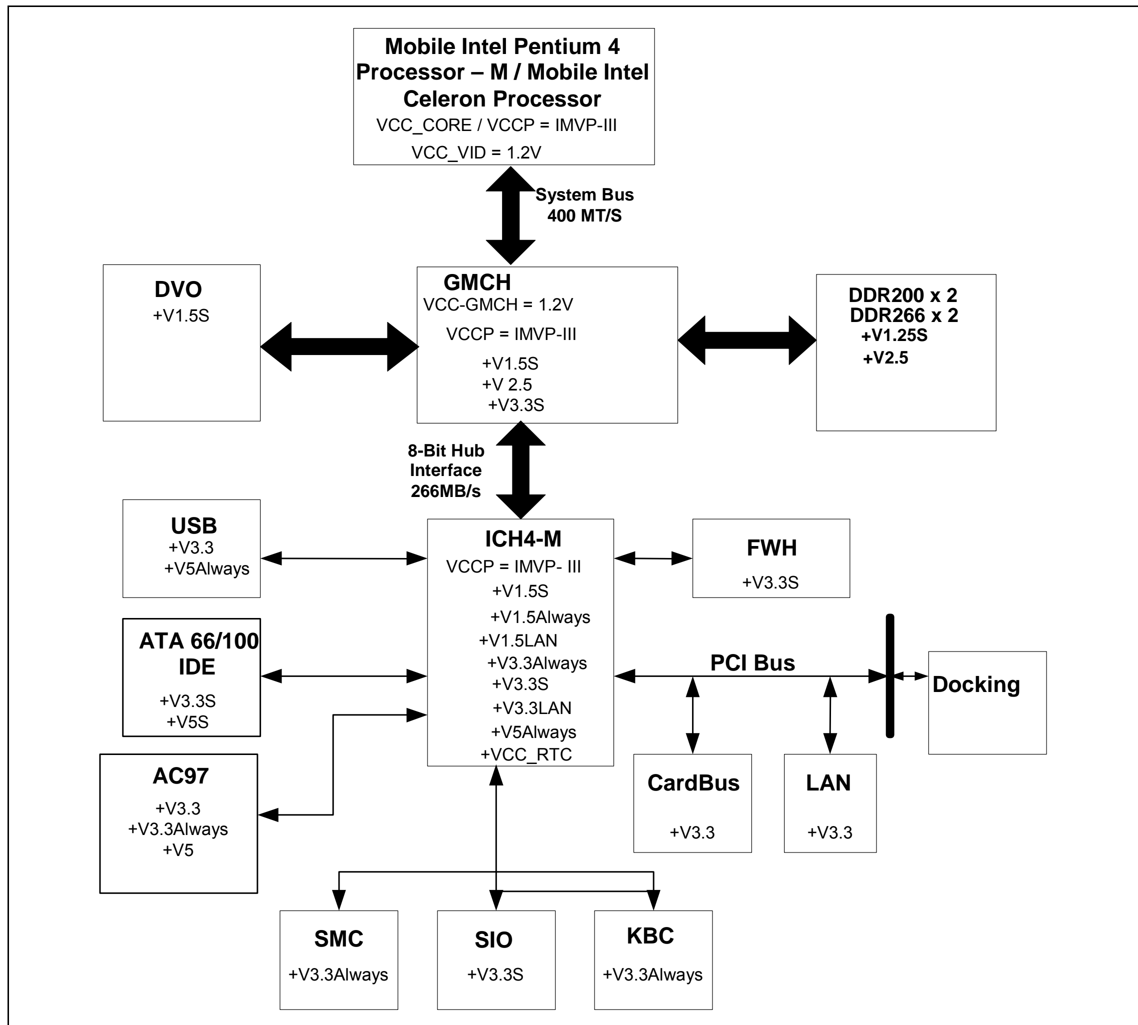
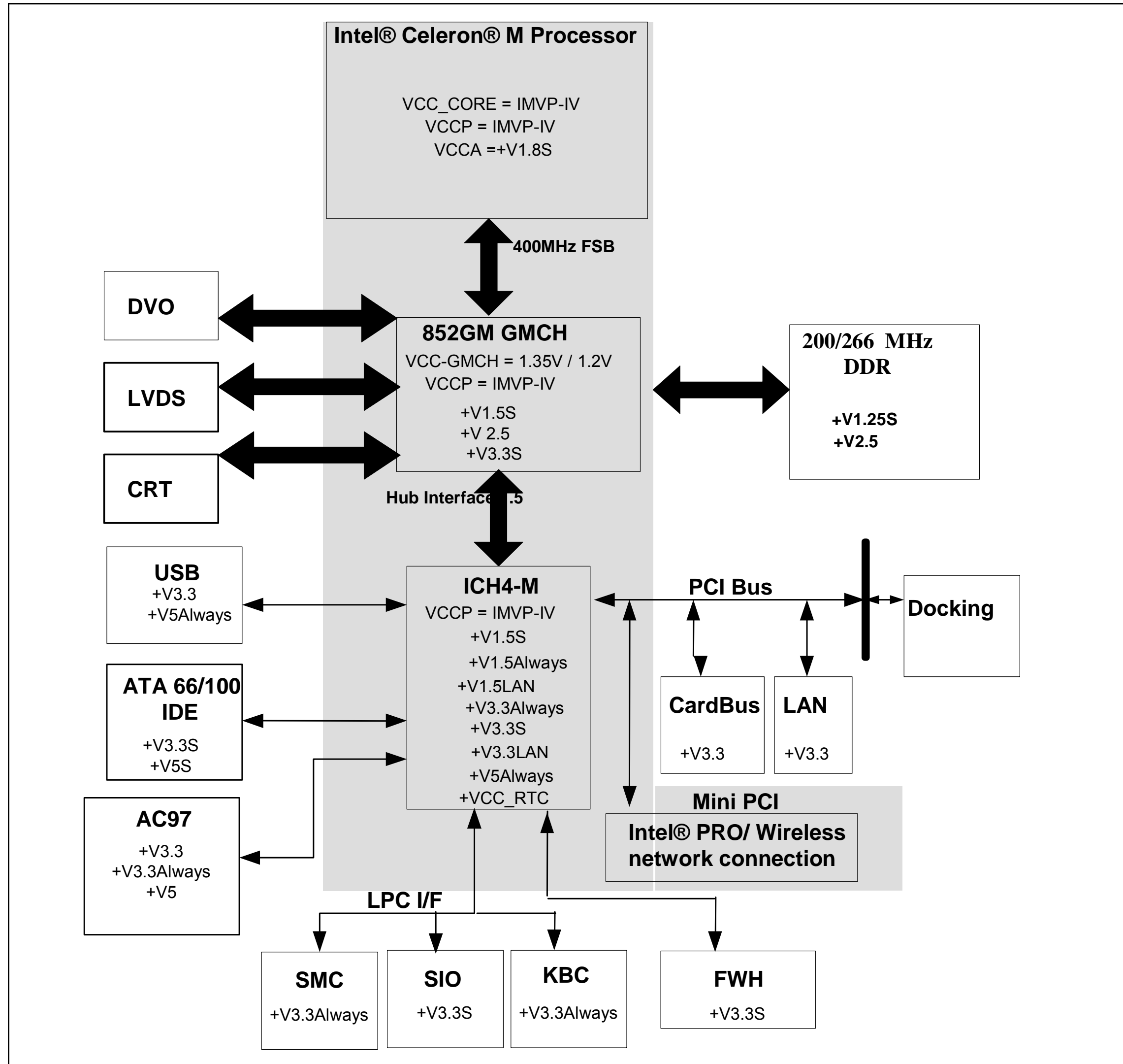


Figure 116. Platform Power Delivery Map for Intel Celeron M Processor



12.3. Voltage Supply

12.3.1. Power Management States

Table 89. Power Management States on Intel Reference Board

Signal	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALW	+V*	+V*S	Clocks
S0 (ON)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1M (POS)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (STR)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (STD)	LOW	LOW	LOW	HIGH	ON	ON/OFF	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

12.3.2. Power Supply Rail Descriptions

Table 90. Power Supply Rail Descriptions on Intel Reference Board

Signal Names	Voltage (V)	Current (A)	Tolerance	Enable	Description
+V1_25S	1.25	0.01	± 3.2%	SLP_S3#	GMCH, DDR Termination
				SLP_S4#	DDR Reference (VREF)
+V1_5	1.5	0.03	± 5%	SLP_S4# - HIGH	LAN logic
+V1_5S	1.5	1.35	± 5%	SLP_S3# - HIGH	GMCHDVO-Core, GMCH DLVDS, GMCH DAC, GMCH ALVDS, ICH4-M core, ICH4-M VCCHL
+V1_5ALWAYS	1.5	0.1	± 5%	+V3ALWAYS	ICH4-M Resume
+V1_2S	1.2	1.8	± 5%	SLP_S3# - HIGH	GMCH Core, GMCH HL, GMCH DPLL, GMCH HPLL, GMCH GPLL, GMCH VCCASM
+V2_5	2.5	8.12	± 5%	SLP_S4# - HIGH	GMCH DDR I/O, DDR SO-DIMM, GMCH TXLVDS[1]
+V3ALWAYS	3.3	0.4	± 5%	+VDC_ON	ICH4-M Resume, SMC/KBC, AC'97
+V3	3.3	0.9	± 5%	SLP_S4# - HIGH	ICH4-M LAN I/O, AC'97, RS232
+V3S	3.3	7.0	± 5%	SLP_S3# - HIGH	GMCH GPIO, ICH4-M I/O, CK-408, FWH, SIO,PCI
+V5	5	9.0	± 5%	SLP_S4# - HIGH	AC'97,

Signal Names	Voltage (V)	Current (A)	Tolerance	Enable	Description
+V5S	5	1.0	± 5%	SLP_S3# - HIGH	ICH4-M VREF, MSE/KBD, FDD, IDE, PCI
+V5ALWAYS	5	3.0	± 5%	+VDC	ICH4-M VREFSUS, USB Supply
+V12S	12	0.2	± 5%	SLP_S3# - HIGH	PCI, IDE
+VCC_CORE / +VCCP Mobile Intel Pentium 4 processor-M	1.2 / 1.3	40.0	See IMVP-III	+VCC_VID -HIGH	Mobile Intel Pentium 4 processor-M I/O core and I/O voltage by IMVP-III VR
+VCC_CORE Intel Celeron M processor	1.356 (Standard) 1.004 (Ultra Low Voltage)	32	± 5%	VID+	Intel Celeron M processor core voltage by IMVP – IV VR ± 10mV (ripple & transient)
+VCCP Intel Celeron M processor	1.05	2.4	± 5%	VR_ON	Intel Celeron M processor I/O voltage by IMVP-IV VR
+VCC_VID	1.2	0.300	+ 5% DC + 9% AC	VR_ON	Reference voltage for Mobile Intel Pentium 4 processor-M PLL and VID circuitry.

NOTE: GMCH VREF, DDR memory VREF, DDR termination, and GMCH TXLVDS can be turned off during S3.

12.4. Intel 852GM Platform Power-Up Sequence

The following sections describe the power-up timing sequence for Intel 852GM GMCH based platforms.

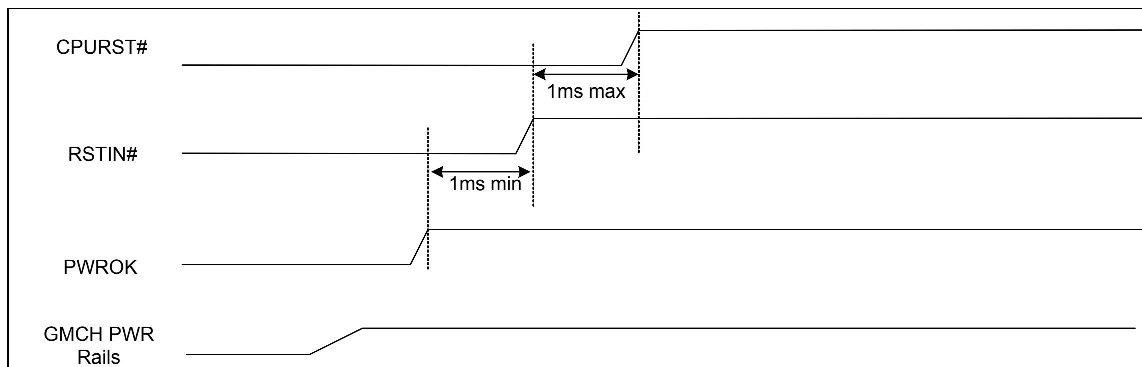
12.4.1. Processor Power Sequence Requirement

Contact your Intel Field Representative for details on the Mobile Intel Pentium 4 Processor-M with IMVP-III voltage regulator or Intel Celeron M processor with IMVP-IV voltage regulator.

12.4.2. GMCH Power Sequencing Requirements

All GMCH power rails should be stable before PWROK is asserted. The power rails can be brought up in any order desired. **However, good design practice would have all GMCH power rails come up as close in time as practical, with the core voltage (1.2 V) coming up first.** RSTIN#, which brings GMCH out of reset, should be deasserted only after PWROK has been active for 1 ms. Once GMCH is out of reset, it will deassert CPURST# within 1 ms.

Figure 117. GMCH Power-Up Sequence

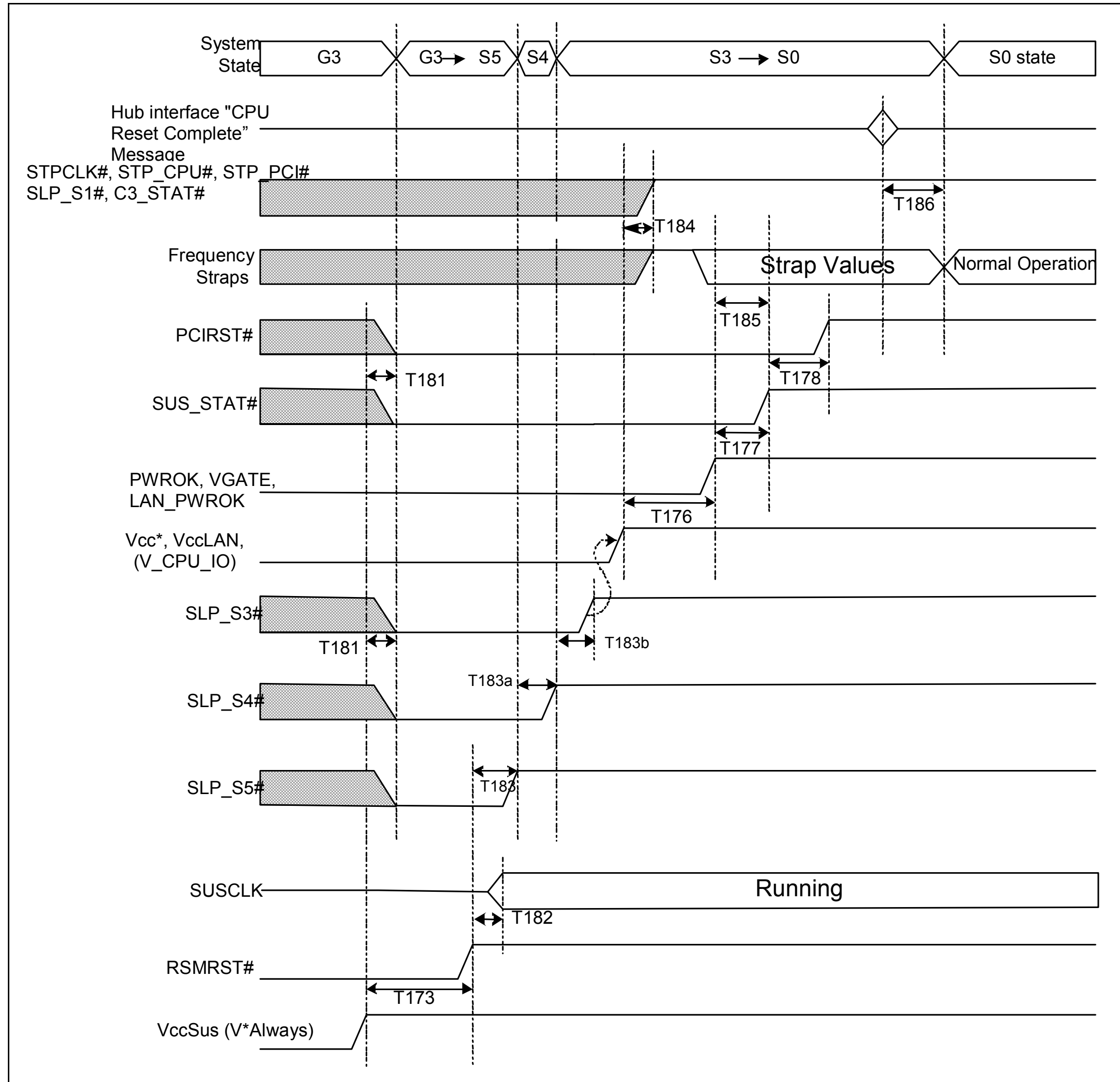


12.4.3. ICH4-M Power Sequencing Requirements

The following figure describes the power-up timing sequence for ICH4-M. The VGATE input should be connected to the processor voltage regulator PWRGD output. When both PWROK and VGATE are asserted, it indicates that core power and system power are stable and PCIRST# will be de-asserted a minimum of 1 ms later. It is the responsibility of the system designer to ensure that the power and timing requirements for the processor and GMCH are met.

Note: Please refer to ICH4-M datasheet for more details.

Figure 118. ICH4-M Power-Up Sequence



Note: It is not necessary for PWROK to be asserted before or after PM_VGATE is asserted. However, if PWROK is asserted after PM_VGATE, it must be delayed 3-10 ms from PWRGD from the VR (which enables clock). Similarly, if PM_VGATE is asserted after PWROK, it must be delayed 3-10 ms from PWRGD from the VR (which enables clock).

Table 91. Timing Sequence Parameters for Figure 118

Sym	Description	Min	Max	Units	Notes
T173	VccSus supplies active to RSMRST# inactive	10	-	ms	
T176	Vcc1.5, Vcc3.3, VccHI, V_CPU_IO supplies active to PWROK, VGATE active	10	-	ms	
T177	PWROK and VGATE active and SYS_RESET# inactive to SUS_STAT# inactive	32	38	RTCCLK	2
T178	SUS_STAT# inactive to PCIRST# inactive	1	3	RTCCLK	2
T181	VccSus active to SLP_S5#, SUS_STAT# and PCIRST# active		50	ns	
T182/T183	RSMRST# inactive to SUSCLK running, SLP_S5# inactive		110	ms	1
T183a	SLP_S5# inactive to SLP_S4# inactive	1	2	RTCCLK	2
T183b	SLP_S4# inactive to SLP_S3# inactive	1	2	RTCCLK	2
T184	V_CPU_IO active to STPCLK#, CPUSLP#, STP_CPU#, STP_PCI#, SLP_S1#, C3_STAT# inactive, and CPU Frequency Strap signals high		50	ns	
T185	PWROK and VGATE active and SYS_RESET# inactive to SUS_STAT# inactive and CPU Frequency Straps latched to strap values	32	38	RTCCLK	2
T186	CPU Reset Complete to Frequency Straps signals unlatched from strap values	7	9	CLK66	3

NOTES:

1. If there is no RTC battery in the system, so VccRTC and the VccSus supplies come up together, the delay from RTCRST# and the RSMRST# inactive to SUSCLK toggling may be as much as 1000 ms.
2. These transitions are clocked off the internal RTC. 1 RTC clock is approximately 32 µs.
3. This transition is clocked off the 66-MHz CLK66. 1CLK66 is approximately 15 ns.

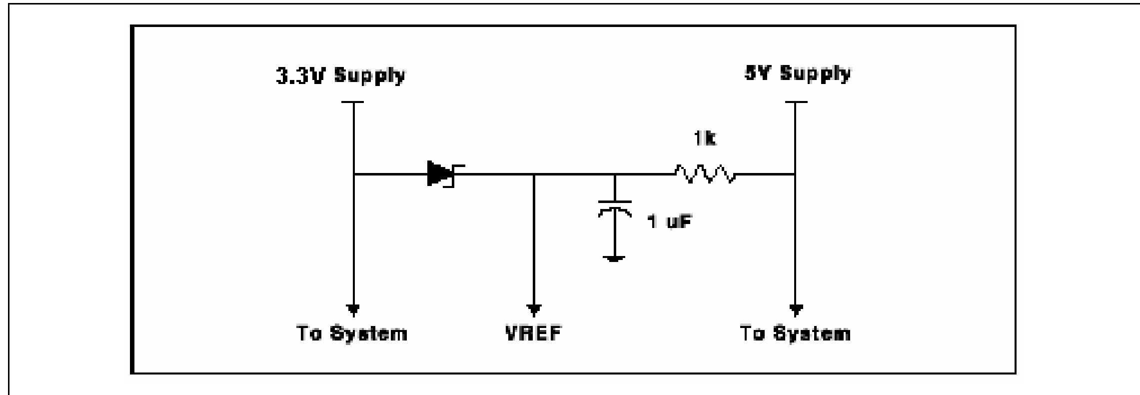
12.4.3.1. 3.3 V/1.5 V Power Sequencing

No power sequencing requirements exist for the associated 3.3 V/1.5 V rail of the ICH4-M chip. It is generally good design practice to power up the core before or at the same time as the other rails.

12.4.3.2. V_{5REF} Sequencing

V_{5REF} is the reference voltage for 5-V tolerance on inputs to the Intel ICH4-M. V_{5REF} must be powered up before V_{CC3_3}, or after V_{CC3_3} within 0.7 V. Also, V_{5REF} must power down after V_{CC3_3}, or before V_{CC3_3} within 0.7 V. These rules must be followed in order to ensure the safety of the Intel ICH4-M. If the rule is violated, internal diodes will attempt to draw power sufficient to damage the diodes from the V_{CC3_3} rail. Figure 119 shows a sample implementation of how to satisfy the V_{5REF}/ 3.3 V sequencing rule.

Figure 119. Example V_{5REF} / $V_{5REFSUS}$ Sequencing Circuitry



12.4.3.3. $V_{5REFSUS}$ Design Guidelines

The same rule for V_{5REF} also applies for V_{5REF_SUS}. However, in most platforms, the V_{CCSUS3_3} rail is derived from the V_{CCSUS5} and therefore, the V_{CCSUS3_3} rail will always come up after the V_{CCSUS5} rail. As a result, V_{5REF_SUS} will always be powered up before V_{CCSUS3_3}. In platforms that do not derive the V_{CCSUS3_3} rail from the V_{CCSUS5} rail, this rule must be comprehended in the platform design.

In order to meet reliability and testing requirements for the USB interface, the following design recommendations for the V_{5REF_SUS} pins of the ICH4-M should be followed. There are changes to the USB specification regarding continuous short conditions must be addressed. The USB 1.1 specification requires host controllers to withstand a continuous short between the USB 5-V connector supply and a USB signal at the connector. However, the duration is unspecified. The USB 2.0 specification requires this duration to be at least 24 hours. This in turn requires that the $V_{5REFSUS}$ pin be at 5 V as long as the attached USB devices are powered. The recommendation is to provide a +V5ALWAYS (active S0-S5) supply to the $V_{5REFSUS}$ pin if available as shown in Figure 120. However, if support for wake on USB from S3 and support for self-powered USB devices are not required, then option shown in Figure 121 can be used. $V_{5REFSUS}$ can be supplied by combination of +V5S (active in S0 only) and +V3ALWAYS (active S0-S5).

Figure 120. V5REFSUS With +V5ALWAYS Connection Option

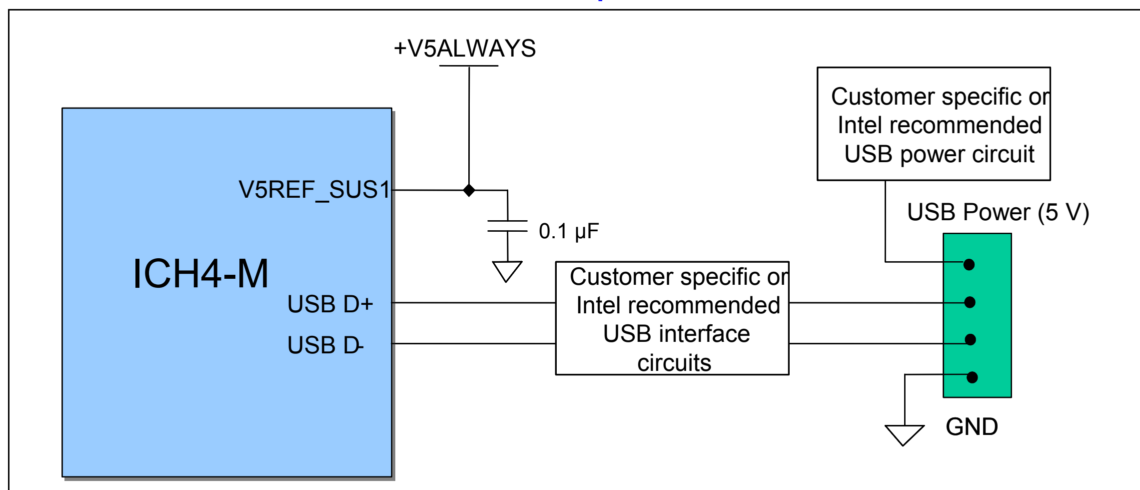
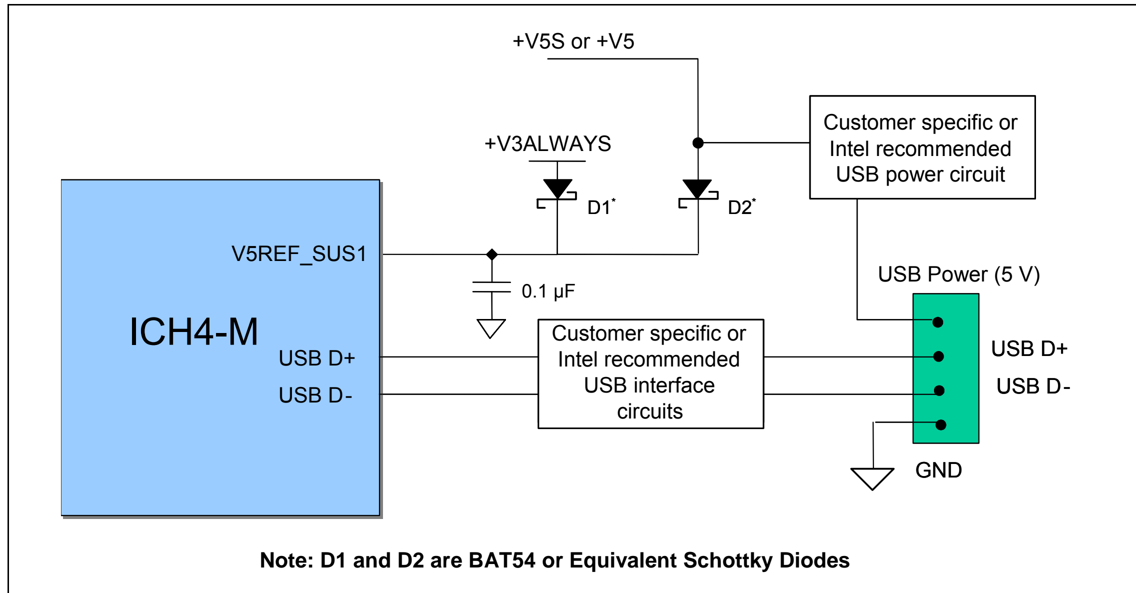


Figure 121. V5REFSUS With +V3ALWAYS and +V5S or +V5 Connection Option



12.4.4. DDR Memory Power Sequencing Requirements

No DDR-SDRAM power sequencing requirements are specified during power-up or power-down if the following criteria are met:

- VDD and VDDQ to memory devices are driven from a single power converter output.
- VTT is limited to 1.44 V (reflecting VDDQ(max)/2 + 50 mV VREF variation + 40 mV VTT variation)
- VREF tracks VDDQ/2
- A minimum resistance of 42 Ω (22-Ω series resistor + 22-Ω parallel resistor ± 5% tolerance) limits the input current from the VTT supply into any pin.

If the above criteria cannot be met by the system design, then the following Table 92 must be adhered to during power-up. Refer to *Intel® DDR 200 JEDEC Spec Addendum* for more details.

Table 92. DDR Power-Up Initialization Sequence

Voltage Description	Sequencing	Voltage Relationship to Avoid Latch-up
VDDQ	After or with VDD	< VDD + 0.3 V
VTT	After or with VDDQ	< VDDQ + 0.3 V
VREF	After or with VDDQ	< VDQ + 0.3 V

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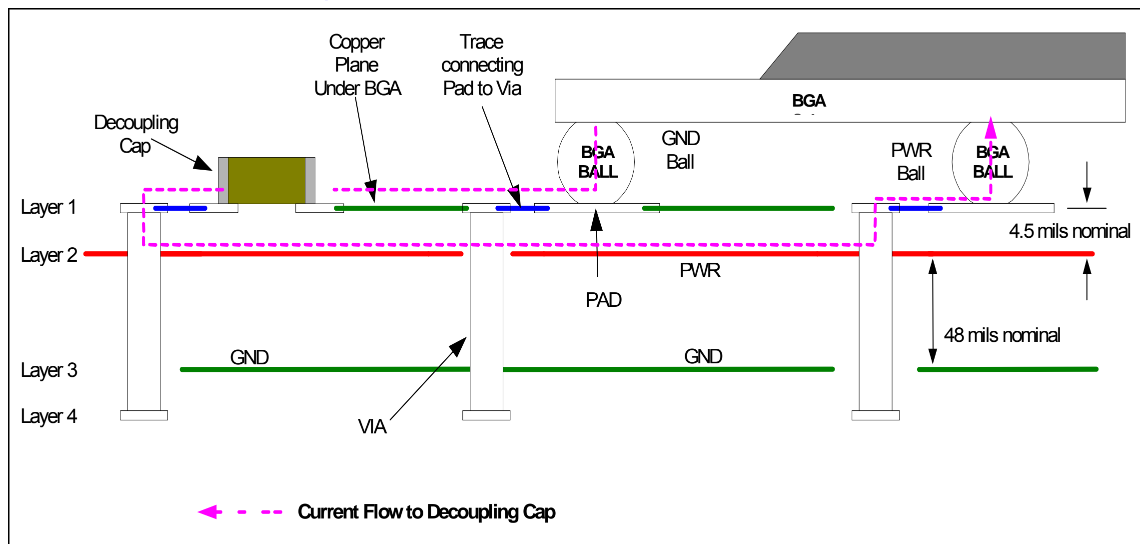
12.5. Intel 852GM Platform Power Delivery Guidelines

Each component is capable of generating large current swings when switching between logic high and logic low. This condition could cause the component voltage rails to drop below specified limits. To avoid this type of situation, ensure that the appropriate amount of bulk capacitance is added in parallel to the voltage input pins. Intel recommends that the developer use the amount of decoupling capacitors specified in this document to ensure the component maintains stable supply voltages. The capacitors should be placed as close to the package as possible. Rotate caps that set over power planes so that the loop inductance is minimized (see Figure 122). The basic theory for minimizing loop inductance is to consider which voltage is on Layer 2 (power or ground) and spin the decoupling cap with the opposite voltage towards the BGA (Ball Grid Array). This greatly minimizes the total loop inductance. Intel recommends that for prototype board designs, the designer should include pads for extra power plane decoupling caps.

Figure 122. Example for Minimizing Loop Inductance



12.5.1. Processor Decoupling / Power Delivery Guidelines

Contact your Intel Field Representative for details on Mobile Intel Pentium 4 Processor-M with IMVP-III voltage regulator or Intel Celeron M processor with IMVP-IV voltage regulator.

12.5.2. Intel 852GM Decoupling Guidelines

Decoupling in Table 93 is based on voltage regulator solution used on the customer reference board design.

Table 93. GMCH Decoupling Recommendations

Pin Name	Configuration	F	Qty	TYPE	Notes
VCC	Connect to VCC1_2S	0.1 µF 10 µF 150 µF	4 1 2	XR7, 0603, 16 V, 10% XR5, 1206, 6.3 V, 20% SPC, E, 6.3 V, 20%	1 X 0.1 µF within 200 mils 3 X 0.1 µF on bottom side
VTTLF	Connect to VCCP	0.1 µF 10 µF 150 µF	2 1 1	XR7, 0603, 16 V, 10% XR5, 1206, 6.3 V, 20% SPC, E, 6.3 V, 20%	2 X 0.1 µF on bottom side
VTTHF	Connect to caps directly	0.1 µF	5	XR7, 0603, 16 V, 10%	
VCCHL	Connect to VCC1_2S	0.1 µF 10 µF	2 1	XR7, 0603, 16 V, 10% XR5, 1206, 6.3 V, 20%	1 X 0.1 µF within 200 mils 1 X 0.1 µF on bottom side
VCCSM	Connect to VCCSus2_5	0.1 µF 150 µF	11 2	XR7, 0603, 16 V, 10% TANT, D, 10 V, 20%	See section 1.5.2.1
VCCDVO	Connect to VCC1_5S	0.1 µF 10 µF 150 µF	2 1 1	XR7, 0603, 16 V, 10% XR5, 1206, 6.3 V, 20% SPC, E, 6.3 V, 20%	1 X 0.1 µF within 200 mils 1 X 0.1 µF on bottom side
VCCDLVDS	Connect to VCC1_5S	0.1 µF 22 µF 47 µF	1 1 1	XR7, 0603, 16 V, 10% TANT, B, 10 V, 20% TANT, D, 10 V, 20%	1 X 0.1 µF within 200 mils
VCCTXLVDS	Connect to VCCSus2_5	0.1 µF 22 µf 47 µF	3 1 1	XR7, 0603, 16 V, 10% TANT, B, 10 V, 20% TANT, D, 10 V, 20%	1 X 0.1 µF within 200 mils 2 X 0.1 µF on bottom side
VCCGPIO	Connect to Vcc3_3S	0.1 µF 10 µF	1 1	XR7, 0603, 16 V, 10% XR5, 1206, 6.3 V, 20%	
SMVREF		0.1 µF	1	XR7, 0603, 16 V, 10%	1 X 0.1 µF on bottom side

12.5.2.1. GMCH VCCSM Decoupling

For the VCCSM pins of the GMCH, a minimum of eleven, 0603 form factor, 0.1-µF, high frequency capacitors is required and must be placed within 150 mils of the GMCH package. The capacitors should be evenly distributed along the GMCH DDR system memory interface and must be placed perpendicular to the GMCH with the power (2.5 V) side of the capacitors facing the GMCH.

- Every GMCH ground and VCCSM power ball in the system memory interface should have its own via.
- Each capacitor should also have its own 2.5-V via within 25 mils of the capacitor pad for connecting to a 2.5-V copper flood. The traces from the capacitors should also be wide and connect to the outer row of balls on the GMCH.
- The ground end of each capacitor must connect to the ground flood and to the ground plane through a via. Each via should be as close to the associated capacitor pad as possible, within 25 mils and with as thick a trace as possible.

12.5.2.2. DDR SDRAM VDD Decoupling

Discontinuities in the DDR signal return paths will occur when the signals transition between the motherboard and the SO-DIMMs. To account for this ground to 2.5-V discontinuity, a minimum of nine 0603 form factor 0.1-µF high frequency bypass capacitors is required between the SO-DIMMs to help minimize any anticipated return path discontinuities that will be created. The capacitors should be distributed as evenly as possible between the two SO-DIMMs.

- Wide ground trace from each capacitor should be connect to a via that transitions to the ground plane. Each ground via should be placed as close to the ground pad as possible.
- Wide 2.5-V trace from each capacitor should connect to a via that transitions to the 2.5-V copper flood. Each via should be placed as close to the capacitor pad as possible. Each capacitor pad should also connect to the closet 2.5-V SO-DIMM pin on either the first or second SO-DIMM connector with a wide trace.

12.5.2.3. DDR VTT Decoupling Placement and Layout Guidelines

The VTT termination rail must be decoupled using high-speed bypass capacitors, one, 0603 form factor, 0.1-µF capacitor and one, 0603 form factor, 0.01-µF capacitor per four DDR signals. They must be place more than 100 mils from the termination resistors.

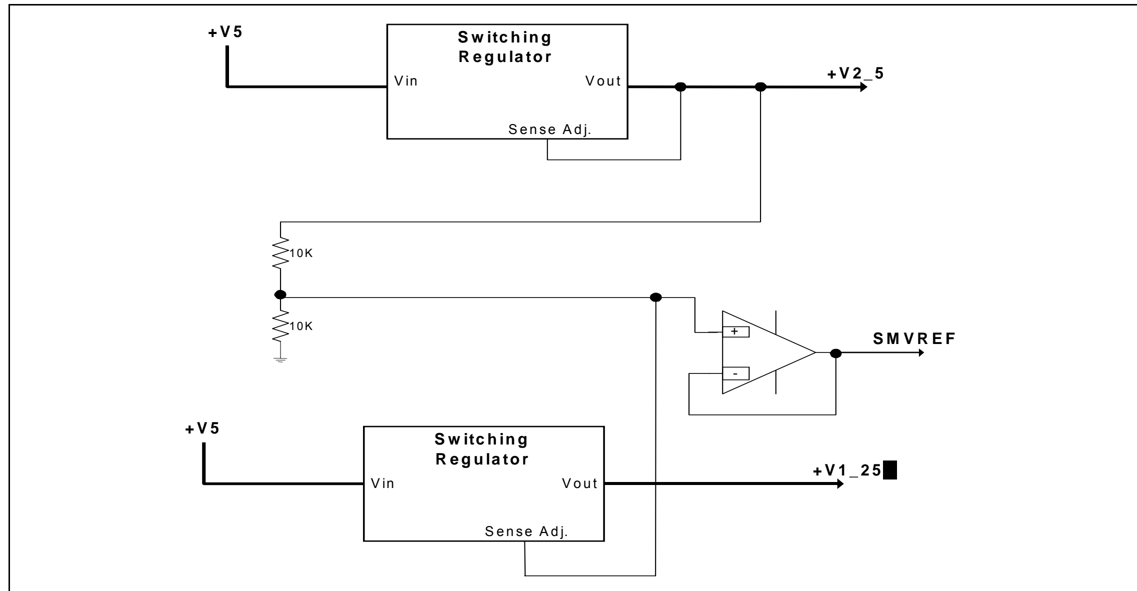
- A VTT copper flood must be used. The decoupling capacitors must be spread out across the termination island so that all the parallel termination resistors are near high frequency capacitors.
- Each capacitor ground via should be as close to the capacitor pad as possible, within 25 mils with as thick a trace as possible.

12.5.3. DDR Memory Power Delivery Design Guidelines

The main focus of these GMCH guidelines is to minimize signal integrity problems and improve the power delivery to the GMCH system memory interface and the DDR memory SO-DIMMs. This section discusses the DDR memory system voltage and current requirements as of publishing for this document. This document is not the original source for these specifications. Figure 123 shows the implementation 2.5 V, 1.25 V and SMVREF on the CRB only as an example. It is the responsibility of the system designer to ensure that the power requirements for the DDR and GMCH are met. Refer to the following documents for the latest details on voltage and current requirements found in this design guide.

- *JEDEC Standard, JESD79 (Release 2), Double Data Rate (DDR) SDRAM Specification*
- *Intel DDR 266 JEDEC Spec Addendum* Rev 1.0 or later

Figure 123. DDR Power Delivery Block Diagram



Note: SMVREF and +V1.25 can optionally be on the switch rail and turned off in either S3 or S4. This is only a block diagram. It is the responsibility of the system designer to ensure that the timing requirements for the DDR memory devices and GMCH are met.

12.5.3.1. 2.5-V Power Delivery Guidelines

The 2.5-V power for the GMCH system memory interface and the DDR SO-DIMMs is delivered around the DDR command, control, and clock signals. Special attention must be paid to the 2.5-V copper flooding to ensure proper GMCH and SO-DIMM power delivery. This 2.5-V flood must extend from the GMCH 2.5-V power vias all the way to the 2.5-V DDR voltage regulator and its bulk capacitors. The 2.5-V DDR voltage regulator must connect to the 2.5-V flood with a minimum of six vias. The SO-DIMM connector 2.5-V pins as well as the GMCH 2.5-V power vias must connect to the 2.5-V copper flood.

In the areas where the copper flooding necks down around the GMCH make sure to keep these neck down lengths as short as possible. The 2.5-V copper flooding under the SO-DIMM connectors must encompass all the SO-DIMM 2.5-V pins and must be solid except for the small areas where the clocks are routed within the SO-DIMM pin field to their specified SO-DIMM pins.

Note: A minimum of 12-mil isolation spacing should be maintained between the copper flooding and any signals on the same layer.

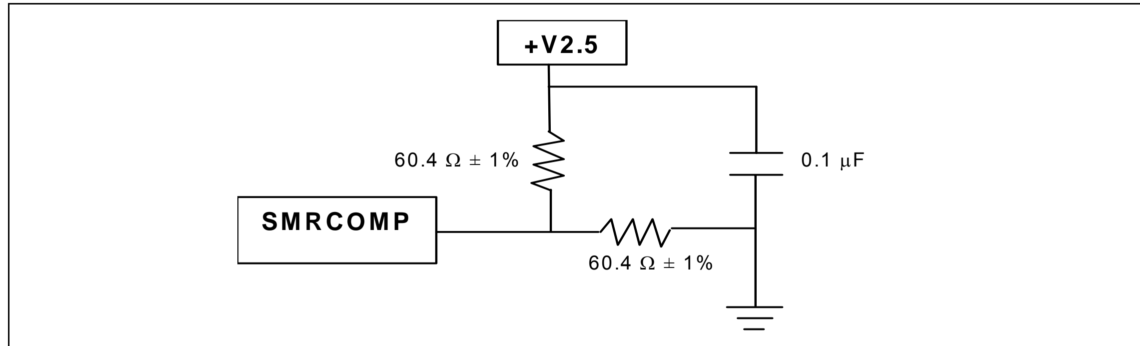
12.5.3.2. GMCH and DDR SMVREF Design Recommendations

There is one SMVREF pin on the GMCH that are used to set the reference voltage level for the DDR system memory signals (SMVREF). The voltage level that needs to be supplied to these pins must be equal to VCCSM/2. As shown in Figure 123 an OpAmp buffer is recommended to generate SMVREF from the 2.5-V supply. This should be used as the “VREF” signals to both the DDR memory devices and the SMVREF signal to the GMCH. **A resistor divider is not a recommended solution since SMVREF has a tight tolerance of ± 2%.**

12.5.3.3. DDR SMRCOMP Resistive Compensation

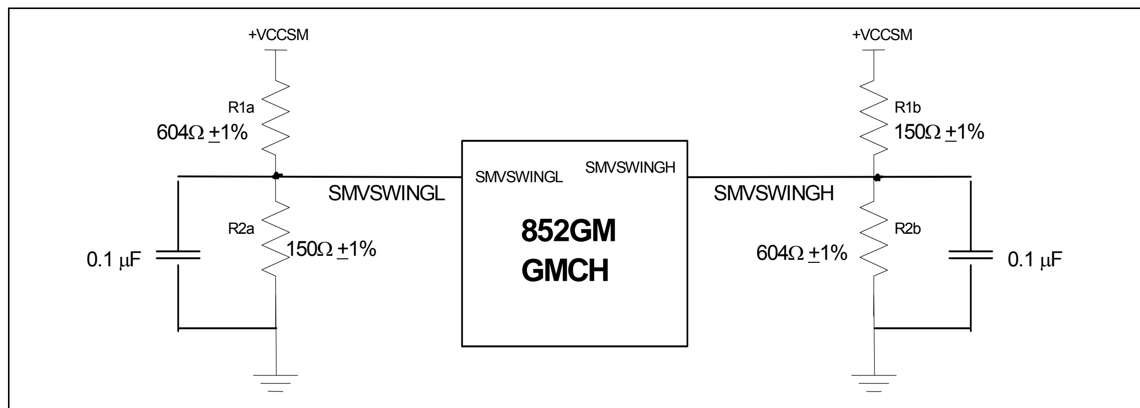
The GMCH requires a system memory compensation resistor, SMRCOMP, to adjust buffer characteristics to specific board and operation environment characteristics. Refer to the *RS – Intel® 852GM GMCH Chipset Datasheet* and Figure 124 for details on resistive compensation. The SMRCOMP signal should be routed with as wide a trace as possible. It should be a minimum of 12 mils wide and be isolated from other signals with a minimum of 10 mils spacing.

Figure 124. GMCH SMRCOMP Resistive Compensation



The GMCH's system memory resistive compensation mechanism also requires the generation of reference voltages to the SMVSWINGL and SMVSWINGH pins. The schematic for SMVSWINGL and SMVSWINGH voltage generation is illustrated in Figure 125. Two resistive dividers with R1b = R2a = 150 Ω ± 1% and R1a = R2b = 604 Ω ± 1% generate the SMVSWINGL and SMVSWINGH voltages. SMVSWINGL and SMVSWINGH components should be placed within 0.5 inches of their respective pins and connected with a 15-mil wide trace. To avoid coupling with any other signals, maintain a minimum of 25 mils of separation to other signals.

Figure 125. GMCH System Memory Reference Voltage Generation Circuit



12.5.3.4. DDR VTT Termination

The recommended topology for DDR-SDRAM Data, Control, and Command signal groups requires that all these signals to be terminated to a 1.25-V source, VTT, at then end of the memory channel opposite the GMCH. Intel recommends that this VTT be generated from the same source as used for VCCSM, and not be used for GMCH and DDR SMVREF. This is because SMVREF has a much tighter tolerance and VTT can vary more easily depending on signal states. A solid 1.25-V termination island should be used to for this purpose and be placed on the surface signal layer, just beyond the last SO-DIMM connector and must be at least 50 mils wide.

The Data and Command signals should be terminated using one resistor per signal. Resistor packs and ± 5% tolerant resistors are acceptable for this application. Only signals from the same DDR signal group can share a resistor pack. See Chapter 6 for system memory guidelines.

12.5.3.5. DDR SMRCOMP, SMVREF, and VTT 1.25-V Supply Disable in S3/Suspend

Regardless of how these 1.25-V supplies for GMCH are generated, they can be disabled during the S3 suspend state to further save power on the platform. This is possible because the GMCH does not require a valid reference voltage nor does it require the enabling of resistive compensation during suspend. **However, some DDR memory devices may require a valid reference voltage during suspend.** It is the responsibility of the system designer to ensure that requirements of the DDR memory devices are met. Note that the 2.5-V VCCSM power pins of the MCH-M and the VDD power pins of the DDR memory devices do need to be on in S3 state.

12.5.4. Other GMCH Reference Voltage and Analog Power Delivery

12.5.4.1. GMCH GTLVREF

For GMCH, the GTLREF generation circuit has been broken down into three separate voltage references; host data reference voltage (HDVREF[2:0]), host address reference voltage (HAVREF) and host common clock reference voltage (HCCVREF). Maximum length from pin to voltage divider for each reference voltage should be less than 0.5 inches. 10-mil wide traces are recommended. GMCH VREF can be maintained as individual voltage dividers as shown in Figure 126, Figure 127, and Figure 128.

Figure 126. GMCH HDVREF[2:0] Reference Voltage Generation Circuit

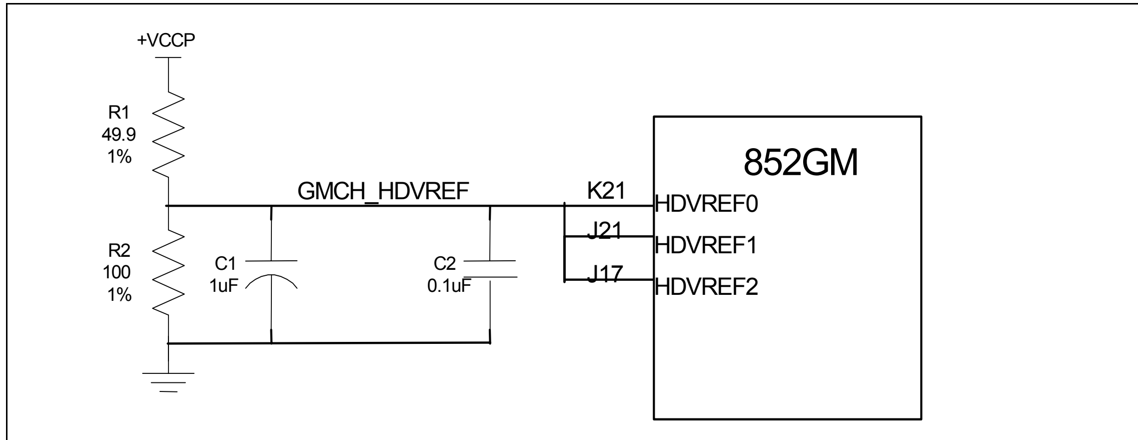


Figure 127. GMCH HAVREF Reference Voltage Generation Circuit

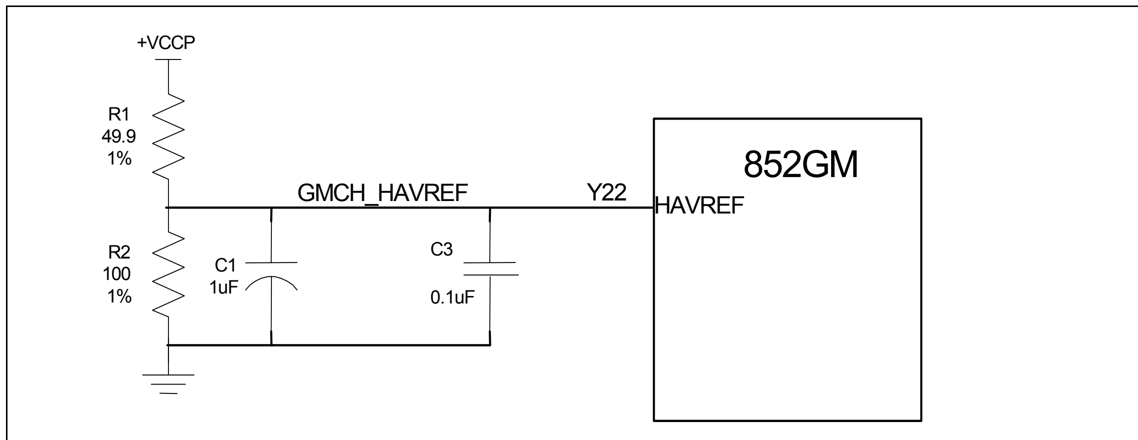
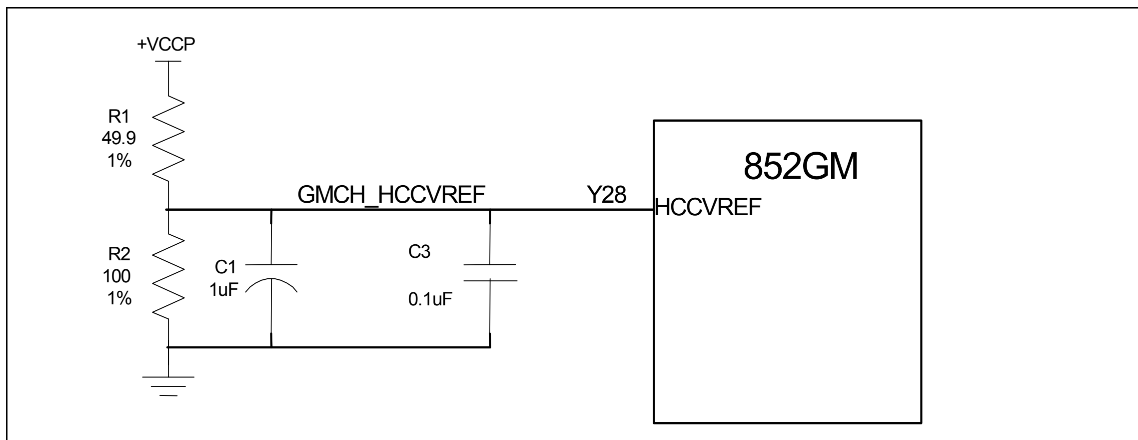


Figure 128. GMCH HCCVREF Reference Voltage Generation Circuit



Sample layout for GMCH VREF generation is shown in Figure 129 and Figure 130.

Figure 129. Primary Side of the Motherboard Layout

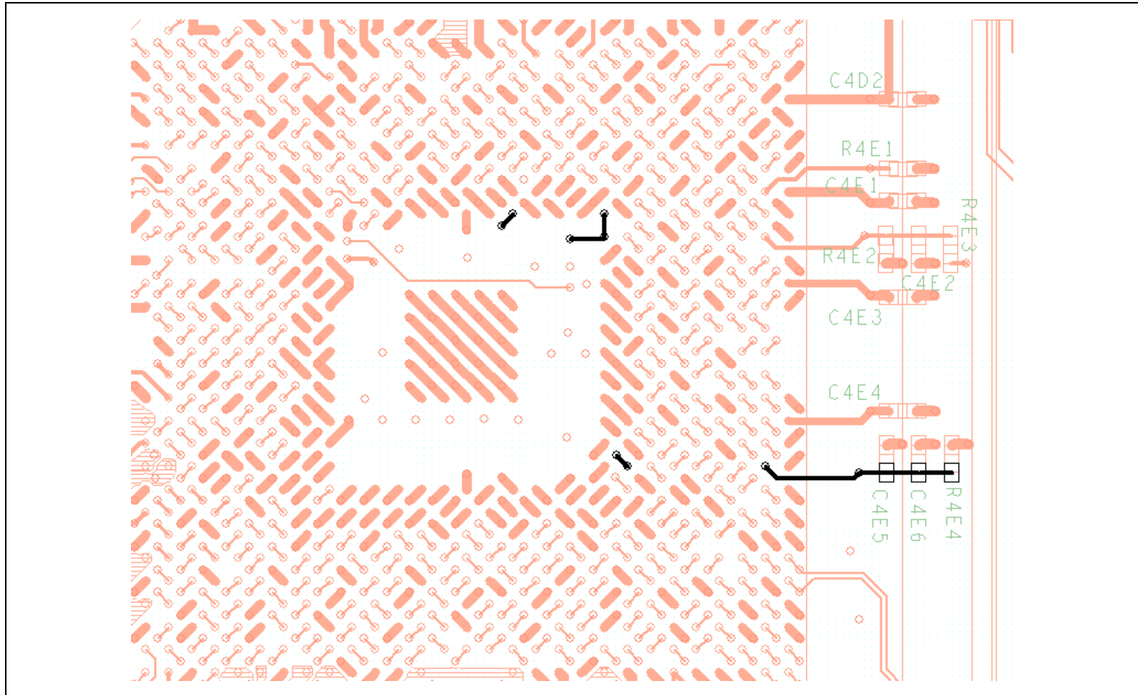
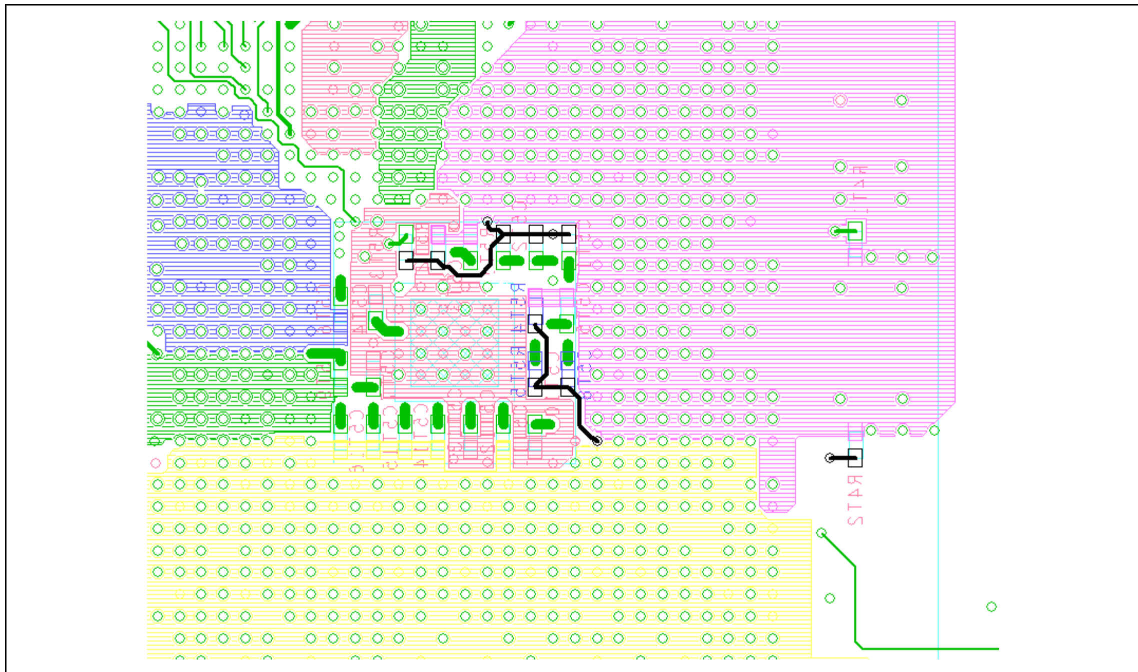


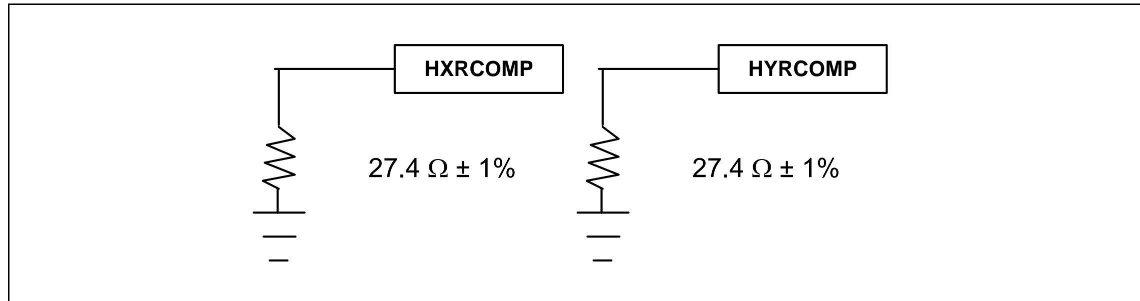
Figure 130. Secondary Side of the Motherboard Layout



12.5.4.2. GMCH AGTL+ I/O Buffer Compensation

The HXRCOMP and HYRCOMP pins of the GMCH should each be pulled-down to ground with a 27.4 Ω ± 1% resistor. See Figure 131. The maximum trace length from pin to resistor should be less than 0.5 inches and should be 18-mil wide to achieve the Zo = 27.4 Ω target. Also, the routing for HRCOMP should be at least 25 mils away from any switching signal.

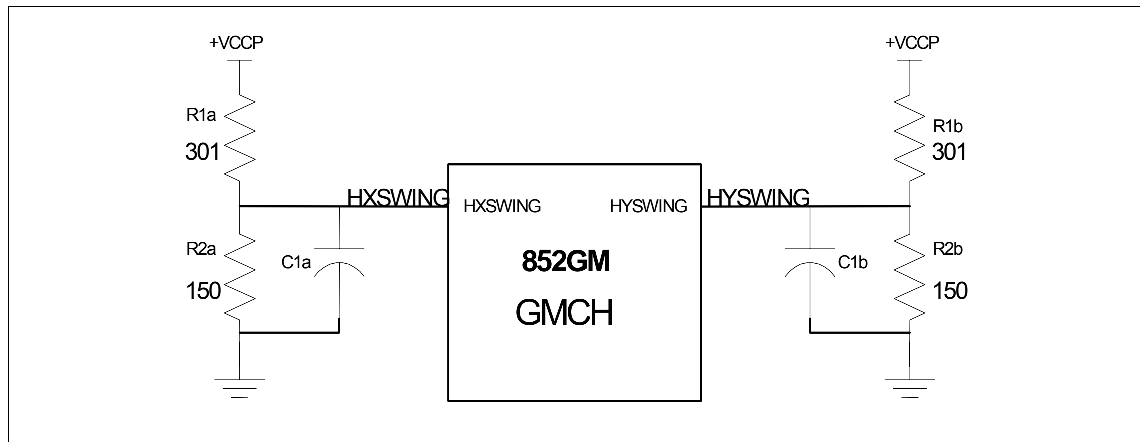
Figure 131. GMCH HXRCOMP and HYRCOMP Resistive Compensation



12.5.4.3. GMCH AGTL+ Reference Voltage

The GMCH's AGTL+ I/O buffer resistive compensation mechanism also requires the generation of reference voltages to the HXSWING and HYSWING pins with a value of 1/3*VCCP. Implementations for HXSWING and HYSWING voltage generation are illustrated in Figure 132. Two resistive dividers with R1a = R1b = 301 Ω ± 1% and R2a = R2b = 150 Ω ± 1% generate the HXSWING and HYSWING voltages. C1a = C1b = 0.1 µF act as decoupling capacitors and connect HXSWING and HYSWING to VCC_CORE. HSWING components should be placed within 0.5 inches of their respective pins and connected with a 15-mil wide trace. To avoid coupling with any other signals, maintain a minimum of 25 mils of separation to other signals.

Figure 132. GMCH HXSWING and HYSWING Reference Voltage Generation Circuit



12.5.4.4. GMCH Analog Power

Table 94 summarizes the eight analog circuits that require filtered supplies on the GMCH. They are: VCCASM, VCCQSM, VCCAHPLL, VCCADPLLA, VCCADPLLB, VCCADAC, VCCAGPLL, and

VCCALVDS. VCCADAC, VCCAGPLL, and VCCALVDS do not require an RLC filter but do require decoupling capacitors.

Figure 133. Example Analog Supply Filter

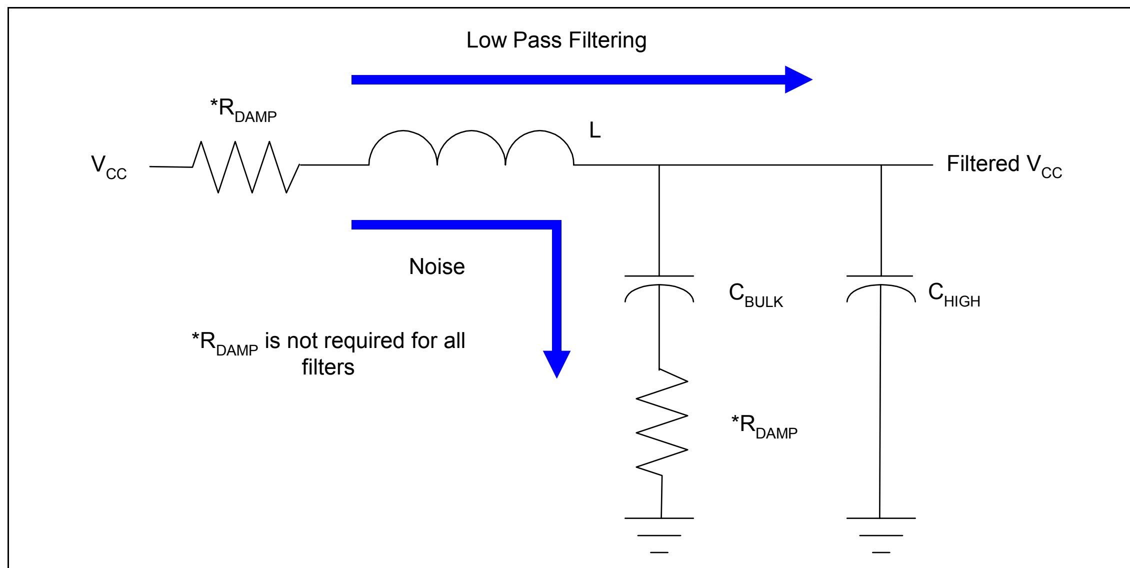


Table 94. Analog Supply Filter Requirements

Required Intel 852GM Filters	Rdamp	Rdamp location	L	Cbulk	Chigh
VCCASM	None	N/A	1210 1.0 μH DCRmax 0.169 Ωs	100 μF	0603 0.1 μF X5R
VCCQSM	1 Ω	In series with Cbulk	0805 0.68 μH DCRmax 0.80 Ωs	1206 4.7 μF X5R	0603 0.1 μF X5R
VCCAHPLL	None	N/A	None		0603 0.1 μF X5R
VCCADPLLA	1 Ω	In series with inductor	0805 0.10 μH	220uF	0603 0.1 μF X5R
VCCADPLLB	1 Ω	In series with inductor	0805 0.10 μH	220 μF	0603 0.1 μF X5R
VCCADAC	None	N/A	None	None	0603 0.1 μF X5R 0603 0.01 μF X5R
VCCAGPLL	None	N/A	None	None	0603 0.1 μF X5R
VCCALVDS	None	N/A	None	None	0603 0.1 μF X5R 0603 0.01 μF X5R

12.5.5. ICH4-M Decoupling / Power Delivery Guidelines

12.5.5.1. ICH4-M Decoupling

The ICH4-M is capable of generating large current swings when switching between logic high and logic low. This condition could cause the component voltage rails to drop below specified limits. To avoid this type of situation, ensure that the appropriate amount of decoupling capacitance is added in parallel to the voltage input pins. Intel recommends that the developer use the amount of high frequency decoupling capacitors specified in table below to ensure that component maintains stable supply voltages. Low frequency decoupling is dependent on layout and system power supply design.

Table 95. ICH4-M Decoupling Requirements

Pin Name	Configuration	F	Qty
VCC3_3	Connect to Vcc3_3S	0.1 µF	6
VCCSUS3_3	Connect to Vcc3_3A	0.1 µF	2
VCCLAN3_3	Connect to Vcc3_3	0.1 µF	2
V_CPU_IO	Connect to Vccp IMVP-IV / III	1 µF 1 µF	1 1
VCC1_5	Connect to Vcc1_5S	0.1 µF	2
VCCSUS1_5	Connect to Vcc1_5A	0.1 µF	2
VCCLAN1_5	Connect to Vcc1_5	0.1 µF	2
V5REF	Connect to Vcc5_Ref	0.1 µF	1
V5REF_SUS	Connect to Vcc5A	0.1 µF	1
VCCRTC	Connect to Vcc_RTC	0.1 µF	1
VCCHI	Connect to Vcc1_5S	0.1 µF	2
VCCPLL	Connect to Vcc1_5S	0.1 µF	1
		0.01 µF	1

NOTE: Capacitors should be placed less than 100 mils from the package.

12.5.6. Hub Interface Decoupling

See Section 9.4 for details.

12.5.7. FWH Decoupling

A 0.1-µF capacitor should be placed between the VCC supply pins and the VSS ground pins to decouple high frequency noise, which may affect the programmability of the device. Value of low frequency bulk decoupling capacitor is dependent on board layout and system power supply design.

12.5.8. General LAN Decoupling

The following are general LAN decoupling recommendations:

- All VCC pins should be connected to the same power supply.
- All VSS pins should be connected to the same ground plane.
- Four to six decoupling capacitors, including two 4.7-µF capacitors are recommended
- Place decoupling as close as possible to power pins.

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13. Reserved, NC, and Test Signals

The processor and Intel 852GM GMCH may have signals listed as "RSVD", "NC", or other name whose functionality is Intel reserved. The following section contains recommendations on how these Intel reserved signals on the processor or GMCH should be handled.

The Mobile Intel Pentium 4 Processor–M has a total of eight NC and nine TESTHI signals that are Intel reserved in the pin-map. For connection recommendations on the TESTHI signals, refer to the latest *Mobile Intel® Pentium® 4 Processor–M Datasheet*. All NC signals must remain unconnected. The location of the Intel reserved signals in the pin-map is listed in Table 96.

Table 96. Processor "Intel Reserved" Signal Pin-Map Locations

Signal Name	Ball Name
NC	A22
NC	A7
NC	AD2
NC	AD3
NC	AE21
NC	AF3
NC	AF24
NC	AF25
TESTHI0	AD24
TESTHI1	AA2
TESTHI2	AC21
TESTHI3	AC20
TESTHI4	AC24
TESTHI5	AC23
TESTHI8	U6
TESTHI9	W4
TESTHI10	Y3

13.1. Intel 852GM GMCH RSVD Signals

Intel 852GM has a total of 32 RSVD and 12 NC signals that are Intel reserved in the pin-map. The recommendation is to provide test points for all RSVD signals. All NC signals should be left as no connects. The location of the Intel reserved signals in the GMCH pin-map is listed in Table 97.

Table 97. Intel 852GM RSVD and NC Signal Pin-Map Locations

Signal Name	Ball Name
NC	AJ29
NC	AH29
NC	B29
NC	A29
NC	AJ28
NC	A28
NC	AA9
NC	AJ4
NC	AJ2
NC	A2
NC	AH1
NC	B1
RSVD	AA22
RSVD	L2
RSVD	P3
RSVD	P4
RSVD	R3
RSVD	R5
RSVD	M1
RSVD	M5
RSVD	R6
RSVD	R4
RSVD	P6
RSVD	P5
RSVD	N5
RSVD	P2
RSVD	N2
RSVD	N3
RSVD	M2
RSVD	T6

Signal Name	Ball Name
RSVD	T5
RSVD	F12
RSVD	D12
RSVD	B12
RSVD	AA5
RSVD	L4
RSVD	F3
RSVD	D3
RSVD	B3
RSVD	F2
RSVD	D2
RSVD	C2
RSVD	B2
RSVD	D7

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14. Platform Design Checklist

The following checklist provides design recommendations and guidance for the mobile Intel Pentium 4 Processor-M, mobile Intel Celeron processor or Intel Celeron M processor systems with the Intel 852GM chipset platform. It should be used to ensure that design recommendations in this design guide have been followed **prior** to schematic reviews. However, this is not a complete list and does not contain detailed layout information.

Note: Unless otherwise specified the default tolerance on resistors is ± 5%. Also note that the (S) reference after power rails such as VCC3_3 (S) indicates a switched rail – one that is powered off during S3-S5.

14.1. General Information

The following section should be filled out by the OEM or Intel field representative.

Processor Min Frequency targeted for this platform	
Processor Max Frequency targeted for this platform	
Voltage Regulator Solution	Part#/Vendor: Target ICC(max):
Target Thermal Envelope (Watts)	
Battery Life	Target:
Form Factor	
Panel Vendor and Size	Part#/Vendor:
Backlight Inverter	Part#/Vendor:
DVO Device	Part#/Vendor:
LOM or mini-PCI LAN?	
Wireless Solution?	
Target FCS (First Customer Ship) Date	

14.2. Customer Implementation of Voltage Rails

Fill in schematic name of voltage rails and mark boxes of when rails are powered on.

Name of Rail	On S0-S1	On S3	On S4	On S5

14.3. Design Checklist Implementation

The voltage rail designations in this checklist are as general as possible. The following table describes the equivalent voltage rails in the Intel reference board schematics.

Checklist Rail	Intel CRB Rail	On S0-S1	On S3	On S4	On S5	Notes
Vcc1_2	+V1.2S_GMCH_CORE, +V1.2S_GMCH_HUB, +V1.2S_GMCH_HGPLL, +V1.2S_GMCH_DPLL, +V1.2S_GMCH_ASM	X				
Vcc1_25	+V1.25S [DDR_Vtt]	X				4
Vcc1_5	+V1.5S_GMCH_DVO, +V1.5S_GMCH_ALVDS, +V1.5S_GMCH_ADAC, +V1.5S_GMCH_DLVDS, +V1.5S_ICH, +V1.5S_ICHHUB	X				
VccSus1_5	+V1.5_ICHLAN	X	X			1,3
V1_5ALWAYS	+V1.5A_ICH	X	X	X	X	
VccSus2_5	+V2.5_GMCH_SM, +V2.5_GMCH_QSM, +V2.5_GMCH_TXLVDS, +V2.5_DDR	X	X			
Vcc3_3	+V3.3S_ICH, +V3.3S_GMCH_GPIO, +V3.3S_CLKRC, +V3.3S_SPD, +V3.3S_LVDS, +V3.3S_FWH	X				
VccSus3_3	+V3.3_ICHLAN, +V3.3_LAN	X				1,2,3
V3ALWAYS	+V3.3ALWAYS_ICH	X	X	X	X	
Vcc5	+V5S_DAC	X				
VccSus5	+V5_USB	X	X			1,3
V5ALWAYS	+V5A_ICH	X	X	X	X	
Vcc12	+V12S	X				
VccRTC	+V_RTC	X	X	X	X	
VCCP	+VCC_IMVP	X				5
VCCA	+VCC_VID	X				6

NOTES:

1. A rail powered in Sx is dependent on implementation.
2. VccLANx rail is powered on in Sx is dependent on implementation.
3. xALWAYS rail can be the SUS rail depending on implementation.
4. Vcc1_25 is the 1.25 V VTT rail for DDR.
5. For the Mobile Intel Pentium 4 Processor-M Front Side Bus, VCCP is the 1.2 V-1.3 V. Note that VCCP is the supply to both the Vtt and Vcore for Mobile Intel Pentium 4 Processor-M.
6. VCC_VID is 1.2 V for processor PLL and VID circuitry.

14.4. Mobile Intel Pentium 4 Processor-M and Mobile Intel Celeron Processor

14.4.1. Resistor Recommendations

Pin Name	System Pull-up/Pull-down	Series Termination	Voltage Translation	Notes	✓
A20M#				Point-to-point connection to ICH4-M.	
BR0#	220 Ω pull-up to VCCP			Point-to-point connection to GMCH, with resistor placed by GMCH.	
COMP[1:0]	51.1 Ω ± 1% pull-down to gnd			Resistor placed within 0.5” of processor pin. Trace should be at least 25 mils from other traces.	
DPSLP#				Connects to GMCH and ICH4	
FERR#	56 Ω pull-up to VCCP			Point-to-point connection to ICH4-M, with resistor placed by ICH4-M.	
GTLREF[3:0]	49.9 Ω ± 1% pull-up to VCCP 100 Ω ± 1% pull-down to gnd			Voltage divider should be placed within 0.5” of processor pin. Place 1-µF cap by the resistor divider, 220 pF by the processor pin.	
GHI#	300 Ω pull-up to VCCP			Point-to-point connection to ICH4-M.	
IERR#	56 Ω pull-up to VCCP			IERR# is a 1.05-V signal. Voltage translation logic may be required if used.	
INIT#			R1 = 2 kΩ R2 = 300 Ω Rs = 300 Ω	Point-to-point connection to ICH4-M. Voltage transition circuit is required if connecting to FWH. Signal is T-split from the ICH4-M to FWH. See Figure 134.	
IGNNE#				Point-to-point connection to ICH4-M.	
LINT0/INTR				Point-to-point connection to ICH4-M.	
LINT1/NMI				Point-to-point connection to ICH4-M.	
PROCHOT#	56 Ω pull up to VCCP		R1 = 1.3 kΩ R2 = 330 Ω Rs = 330 Ω	PROCHOT# is a VCCP signal. This signal is not used on the CRB. So, voltage translation logic may be required if used. **If Voltage Translation is Required**: Driver isolation resistor should be placed at the beginning of the T-split to the system receiver. The receiver at the output of the voltage translation circuit can be any receiver that can function properly with the PROCHOT# signal. See Figure 135.	

Pin Name	System Pull-up/Pull-down	Series Termination	Voltage Translation	Notes	✓
PWRGOOD	300 Ω pull-up to VCCP			Point-to-point connection to ICH4-M, with resistor placed by the processor.	
RESET#	51 Ω pull-up to VCCP			**If ITP700FLEX is Used**: RESET# connects from processor to GMCH and then forks out to ITP700 FLEX, with pull-up and series damping resistor placed next to ITP. Second pull-up may be required at ITP if there is noise issues on the signal.	
SLP#				Point-to-point connection to ICH4-M.	
SMI#				Point-to-point connection to ICH4-M.	
STPCLK#				Point-to-point connection to ICH4-M.	
TESTHI[5:0], TESTHI[10:8]	56 Ω pull up to VCCP				
THERMTRIP#	56 Ω pull-up to VCCP			Point-to-point connection to ICH4-M, with resistor placed by ICH4-M. THERMTRIP# is a VCCP signal. If connecting to other device, voltage translation logic may be required.	
VCC[85:0]	Connect to VCCP				
VCCA, VSSA, VCCIOPLL	Connect to VCCP via filter			See Figure 136.	
VCCSENSE, VSSSENSE	Connect to test vias				
VSS[182:0]	Connect to gnd				

NOTE: Default tolerance for resistors is ± 5% unless otherwise specified.

Figure 134. Routing Illustration for INIT#

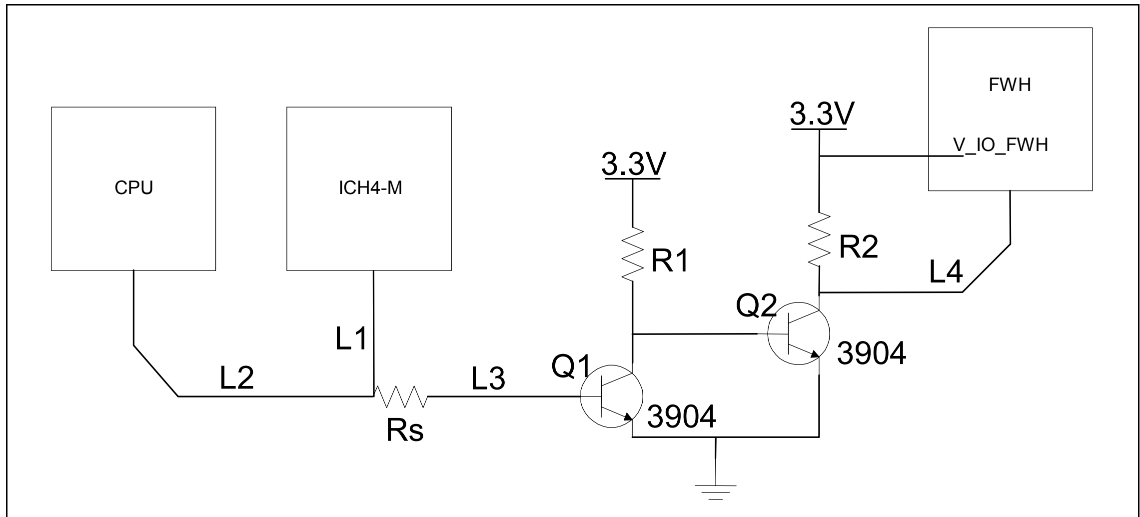


Figure 135. Voltage Translation Circuit for PROCHOT#

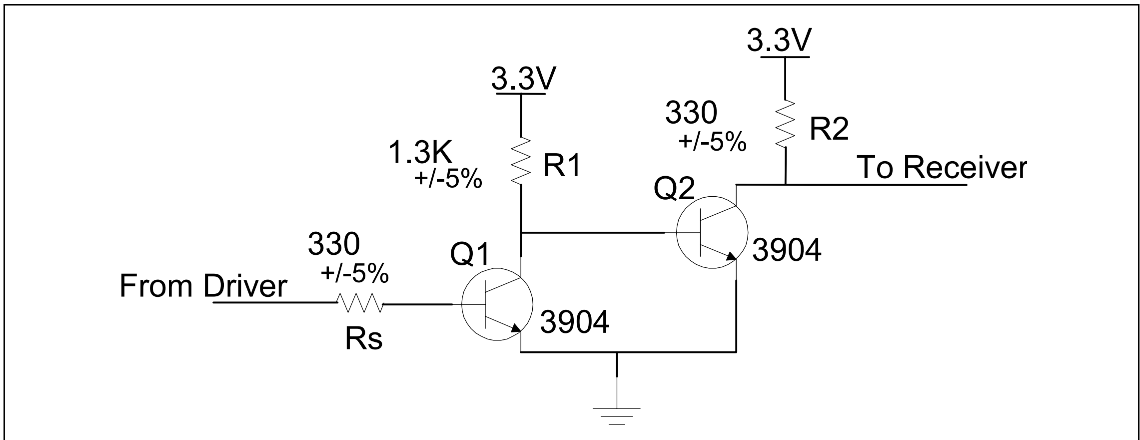
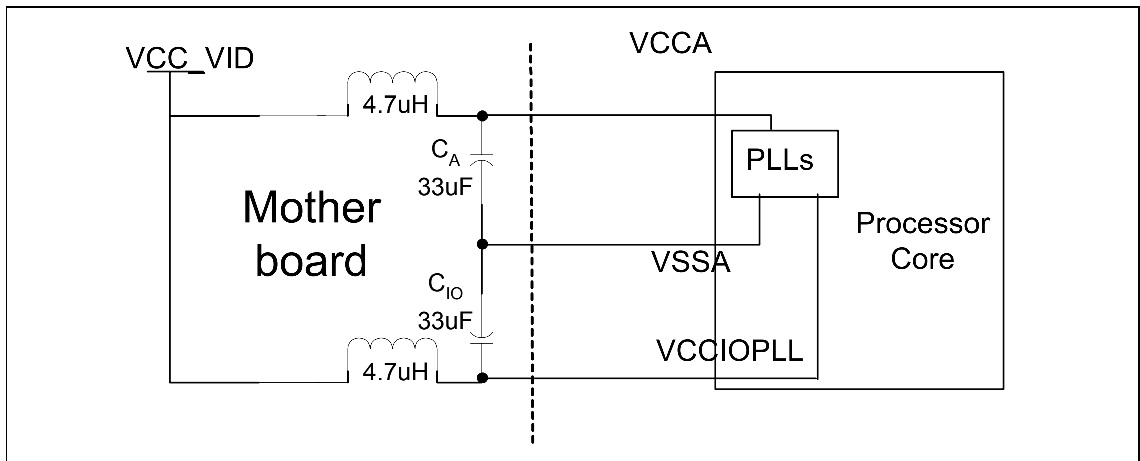


Figure 136. VCCIOPLL, VCCA and VSSA Power Distribution



14.4.2. In Target Probe (ITP)

Pin Name	System Pull-up /Pull-down	Series Termination Resistor (Ω)	Notes	✓
BPM[5:0]#	51 Ω pull-up to VCCP		Connect to processor, with resistors placed by the processor.	
DBR#	150-240 Ω pull-up to V3ALWAYS		If using ITP on interposer card, then DBR# should also be connected to DBRESET pin at the processor.	
RESET#	51 Ω pull-up to VCCP If USING ITP700FLEX	150 Ω from pull-up to ITP700FLEX	See Notes in Section 14.4.1.	
FBO			Connect to TCK pin of processor. .	
TCK	27.4 Ω ± 1% pull-down to gnd		Connect to processor, with resistor placed by ITP.	
TDI	150 Ω pull-up to VCCP		Connect to processor, with resistor placed by ITP.	
TDO	75 Ω pull-up to VCCP		Connect to processor, with resistor placed by ITP. If ITP not used, this signal can be left as NC.	
TMS	39.2 Ω ± 1% pull-up to VCCP		Connect to processor, with resistor placed by ITP.	
TRST#	680 Ω pull-down to gnd		Connect to processor.	
VTAP, VTT[1:0]	Connect to VCCP		One 0.1 µF decoupling cap is required.	

NOTE: The above recommendation is only for ITP700FLEX. If using other ITP, please refer to the appropriate ITP documents.

14.4.3. Decoupling Recommendations

Signal	Configuration	Value	Qty	Notes	✓
VCC[Vcc_core]	Connect to VCCP	10 µF	38	X5R/X7R, 1206 package. Use for high frequency decoupling. Bulk decoupling will depend on the VR solution. The maximum Equivalent Series Resistance should be equal to or less than 2.5 mΩ.	

NOTE: Decoupling guidelines are recommendations based on our reference board design. Customers will need to take layout and PCB board design into consideration when deciding on overall decoupling solution.

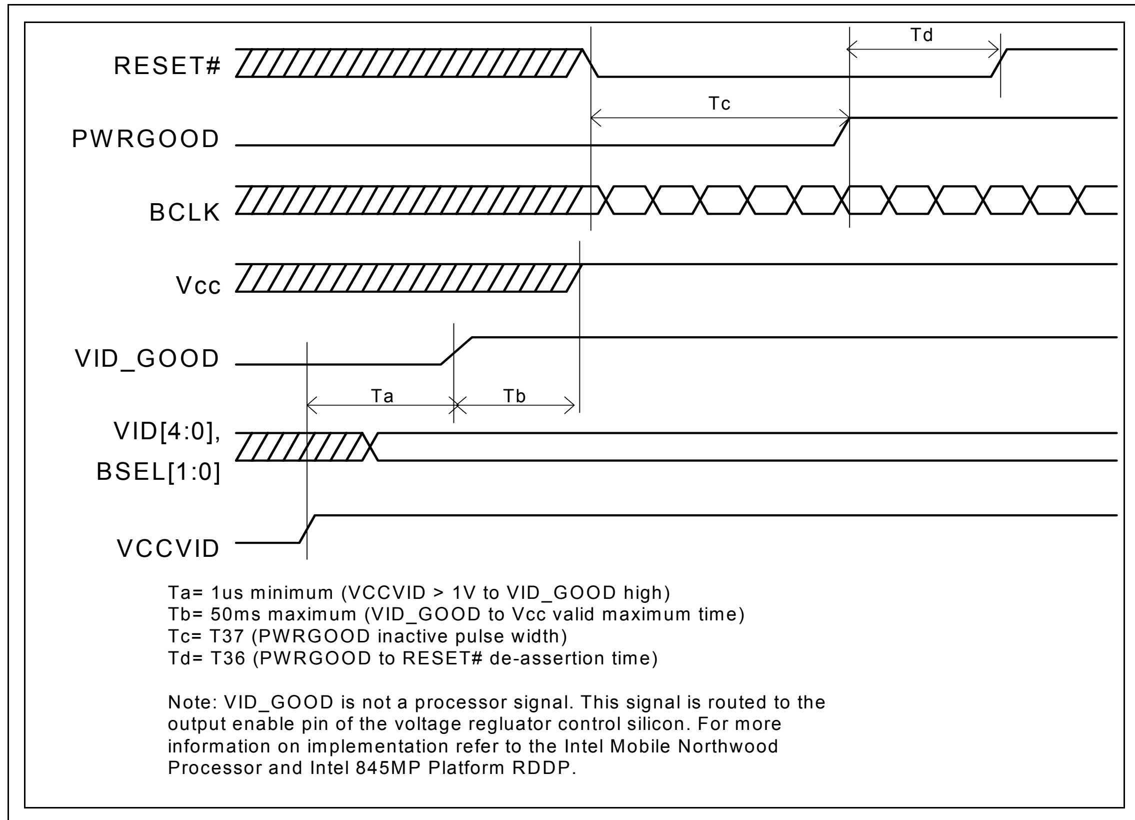
14.4.4. Power-up Sequence

Please refer to processor datasheet for latest information.

Table 98. Mobile Intel Pentium 4 Processor-M Power-up Timing Specifications

Sym	Timing Parameters	Min	Max	Unit	Notes	✓
Ta	VccVID active to VID_GOOD	1		µs	Please refer to the Mobile Intel Pentium 4 Processor-M Datasheet. See Figure 137.	
Tb	VID_GOOD valid to Vcc active		50	ms	Please refer to the Mobile Intel Pentium 4 Processor-M Datasheet. See Figure 137.	
Tc	BCLK stable to PWRGOOD active	10		BCLKs	Please refer to the Mobile Intel Pentium 4 Processor-M Datasheet. See Figure 137.	
Td	PWRGOOD active to RESET# inactive	1	10	ms	Please refer to the Mobile Intel Pentium 4 Processor-M Datasheet. See Figure 137.	

Figure 137. Mobile Intel Pentium 4 Processor-M Power Up Sequence



14.5. Intel Celeron M Processor

14.5.1. Resistor Recommendations

Pin Name	System Pull-up/Pull-down	Series Termination	Voltage Translation	Notes	✓
A20M#				Point-to-point connection to ICH4-M.	
BR0#				Point-to-point connection to GMCH.	
COMP0, COMP2	27.4 Ω ± 1% pull-down to gnd			Resistor placed within 0.5” of processor pin. Trace should be 27.4 Ω ± 15%.	
COMP1, COMP3	54.9 Ω ± 1% pull-down to gnd			Resistor placed within 0.5” of processor pin. Trace should be 55Ω ± 15%.	
DPSLP#				Point-to-point connection to GMCH.	
FER#	56 Ω pull-up to VCCP	56 Ω from pull-up to ICH4-M pin.		Point-to-point connection to ICH4-M, with pull-up resistor and series resistor placed by ICH4-M.	
GTLREF	1 KΩ ± 1% pull-up to VCCP 2 KΩ ± 1% pull-down to gnd			Voltage divider should be placed within 0.5” of processor pin.	

Pin Name	System Pull-up/Pull-down	Series Termination	Voltage Translation	Notes	✓
IERR#	56 Ω pull-up to VCCP			IERR# is a 1.05 V signal. Voltage translation logic and/or series resistor may be required if used.	
INIT#			R1 = 1.3 KΩ R2 = 330 Ω Rs = 330 Ω	Point-to-point connection to ICH4-M. Voltage transition circuit is required if connecting to FWH. Signal is T-split from the ICH4-M to FWH.	
IGNNE#				Point-to-point connection to ICH4-M.	
LINT0/INTR				Point-to-point connection to ICH4-M.	
LINT1/NMI				Point-to-point connection to ICH4-M.	
PROCHOT#	56 Ω pull up to VCCP		R1 = 1.3 KΩ R2 = 330 Ω Rs = 330 Ω	PROCHOT# is a VCCP signal. This signal is not used on the CRB. So, voltage translation logic may be required if used. **If Voltage Translation is Required**: Driver isolation resistor should be placed at the beginning of the T-split to the system receiver.	
PSI#				Can be left as NC, if not used for IMVP.	
PWRGOOD	330 Ω pull-up to VCCP			Point-to-point connection to ICH4-M, with resistor placed by the processor.	
RESET#	54.9 Ω ± 1% pull-up to VCCP If USING ITP700FLEX	22.6 Ω ± 1% from pull-up to ITP700FLEX		**If ITP700FLEX is Not Used**: Point-to-point connection to GMCH. **If ITP700FLEX is Used**: RESET# connects from processor to GMCH and then forks out to ITP700 FLEX, with pull-up and series damping resistor placed next to ITP.	
RSVD (pin AC1, AF7, C3, C14, E26, G1)				Route to test points.	
SLP#				Point-to-point connection to ICH4-M.	
SMI#				Point-to-point connection to ICH4-M.	
STPCLK#				Point-to-point connection to ICH4-M.	
TEST[3:1]	1 KΩ pull-down to gnd (default: no stuff)			For each signal, stuffing option for pull-down should be provided for testing purposes. For normal operation, leave the resistors unpopulated.	
THERMTRIP#	56 Ω pull-up to VCCP	56 Ω from pull-up to ICH4-M pin		Point-to-point connection to ICH4-M, with pull-up and series resistors placed by ICH4-M. THERMTRIP# is a VCCP signal. If connecting to other device, voltage translation logic may be required.	
VCC[71:0]	Connect to VccCORE				
VCCA[3:0]	Connect to Vcc1_8				
VCCP[26:0]	Connect to VCCP				

Pin Name	System Pull-up/Pull-down	Series Termination	Voltage Translation	Notes	✓
VCCSENSE, VSSSENSE	54.9 Ω ± 1% pull-down to gnd (default: no stuff)			For each signal, stuffing option for pull-down should be provided for testing purposes. Also, a test point for differential probe ground should be placed between the two resistors. For normal operation, leave the resistors unpopulated.	
VSS[191:0]	Connect to gnd				

Figure 138. Routing Illustration for INIT# (for Intel Celeron M Processor)

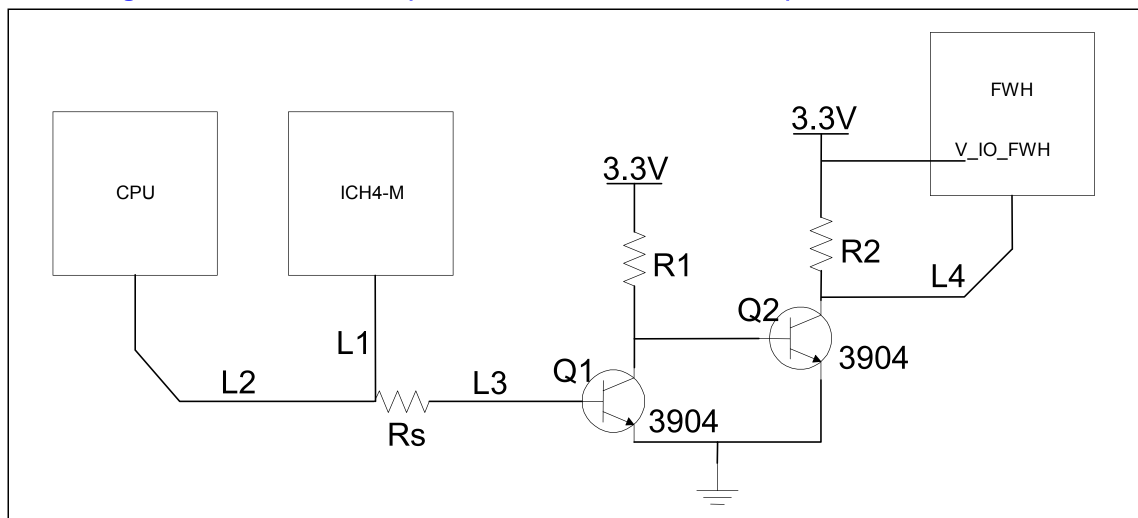
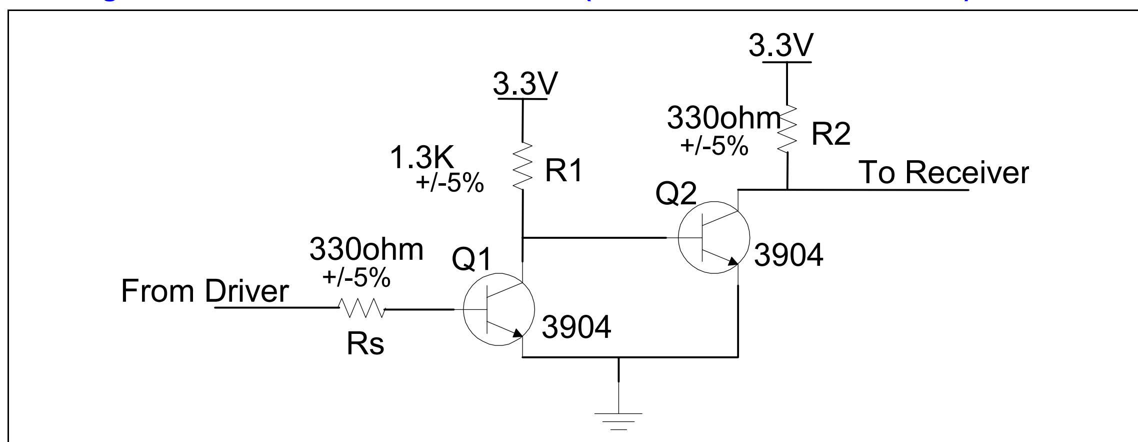


Figure 139. Voltage Translation Circuit for PROCHOT# (for Intel Celeron M Processor)

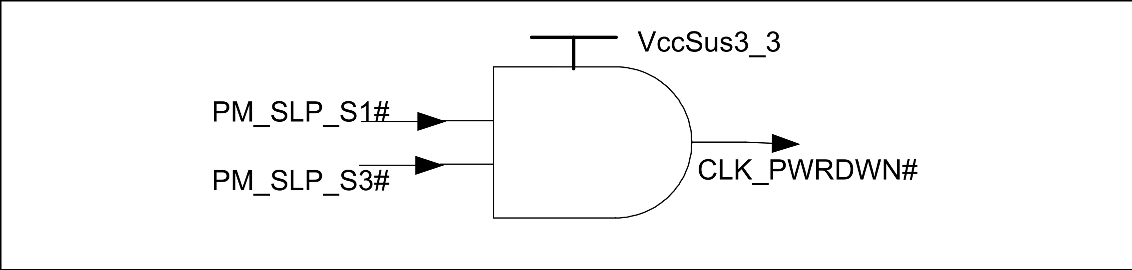


14.6. CK-408 Clock Checklist

14.6.1. Resistor Recommendations

Pin Name	System Pull-up/Pull-down	Series Resistor	Notes	✓
3V66[0] 3V66[1]		33 Ω	If the signal is used, one 33-Ω series resistor is required. If the signal is NOT used, it should be left as NC (Not Connected) or connected to a test point.	
66BUF[2:0]		33 Ω	Use 66BUF[1] (pin 22) for GMCH. Use one of the other two signals for ICH4-M.	
CPU[0], CPU[0]# CPU[1], CPU[1]# CPU[2], CPU[2]#	49.9 Ω ± 1% pull- down to gnd	33 Ω	Use one pair for the processor and another pair for GMCH. If on-board ITP is implemented, the third pair of clock signals is used for the ITP connector. Otherwise, it can be routed to the dedicated ITP clock pins on the processor socket.	
48MDOT		33 Ω	Connect to GMCH's DREFCLK.	
3V66/VCH		33 Ω	Two possible topologies: • Use directly for GMCH's DREFSSCLK. • Use as input to an SSC component and use the SSC component output for GMCH's DREFSSCLK.	
IREF	475 Ω ± 1% pull-down to gnd			
MULT[0]	10 kΩ pull-up to Vcc3_3			
PCI[6:0]		33 Ω	Connect to various PCI devices.	
PCIF[2], PCIF[1], PCIF[0]		33 Ω	Use one clock for ICH4-M. Unused clock pins should be left as NC or connected to a test point.	
PWRDWN#		AND gate	This signal is needed for supporting S1M. It needs to be driven low by both SLP_S1# and SLP_S3# through an AND gate. See Figure 140.	
REF		33 Ω	This is the 14.318MHz clock reference signal for ICH4-M, SIO and LPC. Each receiver requires one 33-Ω series resistor.	
SEL[2:1]	10K-20KΩ pull-down to gnd			
SEL[0]	10K-20KΩ pull- up to Vcc3_3			
48MUSB		33 Ω	Connect to ICH4-M's 48-MHz clock input.	
XTAL_IN, XTAL_OUT			Connect to a 14.318 MHz crystal, placed within 500 mils of CK-408.	
VDD[7:0], VDDA	Connect to Vcc3_3		Refer to clock vendor datasheet for decoupling info.	
VSS[5:0], VSSA	Connect to gnd			
VSSIREF	Connect to gnd			

Figure 140. Clock Power-down Implementation



14.7. Intel 852GM GMCH Checklist

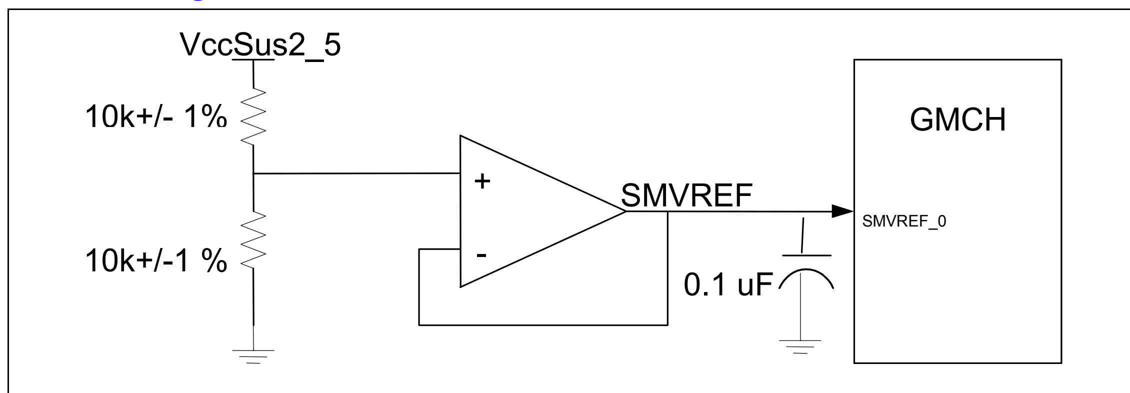
14.7.1. System Memory

14.7.1.1. GMCH System Memory Interface

Pin Name	System Pull-up/Pull-down	Series Resistor	Notes	✓
RCVENIN#			This signal should be routed to a via next to ball and left as a NC (No Connect).	
RCVENOUT#			This signal should be routed to via next to ball and left as a NC (No Connect).	
SBA[1:0], SCAS#, SRAS#, SWE#	56 Ω pull-up to Vcc1_25	10 Ω	Three topologies available for routing these signals.	
SCKE[3:0], SCS#[3:0]	56 Ω pull-up to Vcc1_25			
SDQ[63:0], SDM[7:0], SDQS[7:0]	56 Ω pull-up to Vcc1_25	10 Ω		
SDQ[71:64], SDM8, SDQS8	56 Ω pull-up to Vcc1_25	10 Ω	ECC detection is not supported. These signals should be left as NC.	
SMA[12:6,3,0]	56 Ω pull-up to Vcc1_25	10 Ω	Three topologies available for routing these signals.	
SMA[5,4,2,1] SMAB[5,4,2,1]	56 Ω pull-up to Vcc1_25		Use SMA[5,4,2,1] for one SO-DIMM connector; use SMAB[5,4,2,1] for the other SO-DIMM connector.	
SCK0, SCK0# SCK1, SCK1#			These clock signals connect to SO-DIMM 0.	
SCK2, SCK2#			ECC detection is not supported and these clock signals should be left as NC.	
SCK3, SCK3# SCK4, SCK4#			These clock signals connect to SO-DIMM 1.	
SCK5, SCK5#			ECC detection is not supported and these clock signals should be left as NC.	
SMVREF	10 kΩ 1% pull-up to VccSus2_5 10 kΩ 1% pull-down to gnd		Signal voltage level = VccSus2_5/ 2. Note that a buffer is used to provide the necessary current and reference voltage to SMVREF. Place a 0.1 μF cap by GMCH. See Figure 141. This signal may be optionally connected to Vcc2_5 and powered off in S3.	
SMVSWINGL	604 Ω 1% pull-up to VccSus2_5 150 Ω 1% pull-down to gnd		Signal voltage level = 1/5 * VccSus2_5. Need 0.1 μF cap at pin. This signal may be optionally connected to Vcc2_5 and powered off in S3.	
SMVSWINGH	150 Ω 1% pull-up to VccSus2_5 604 Ω 1% pull-down to gnd		Signal voltage level = 4/5 * VccSus2_5. Need 0.1 μF cap at pin. This signal may be optionally connected to Vcc2_5 and powered off in S3.	
SMRCOMP	60.4 Ω 1% pull-up to		Signal voltage level = 1/2 * VccSus2_5.	

Pin Name	System Pull-up/Pull-down	Series Resistor	Notes	✓
	VccSus2_5 60.4 Ω 1% pull-down to gnd		Need 0.1 µF cap by the voltage divider. This signal may be optionally connected to Vcc2_5 and powered off in S3.	

Figure 141. Reference Voltage Level for SMVREF



14.7.1.2. DDR SO-DIMM Interface

Pin Name	Configuration	Notes	✓
VREF[2:1]		Signal voltage level = VCCSus2_5 / 2.	
VDD[33:1]	Connect to VccSus2_5	Power must be provided during S3.	
VDDSPD	Connect to Vcc3_3		
SA[2:0]	Connect to either VC3_3 or gnd	These lines are used for strapping the SPD address for each SO-DIMM.	
VSS[31:1]	Connect to gnd		
RESET(DU)		Signal can be left as NC ("Not Connected)	
VDDID		Signal can be left as NC ("Not Connected)	
DU[4:1]		Signal can be left as NC ("Not Connected)	
GND[1:0]		Signal can be left as NC ("Not Connected)	

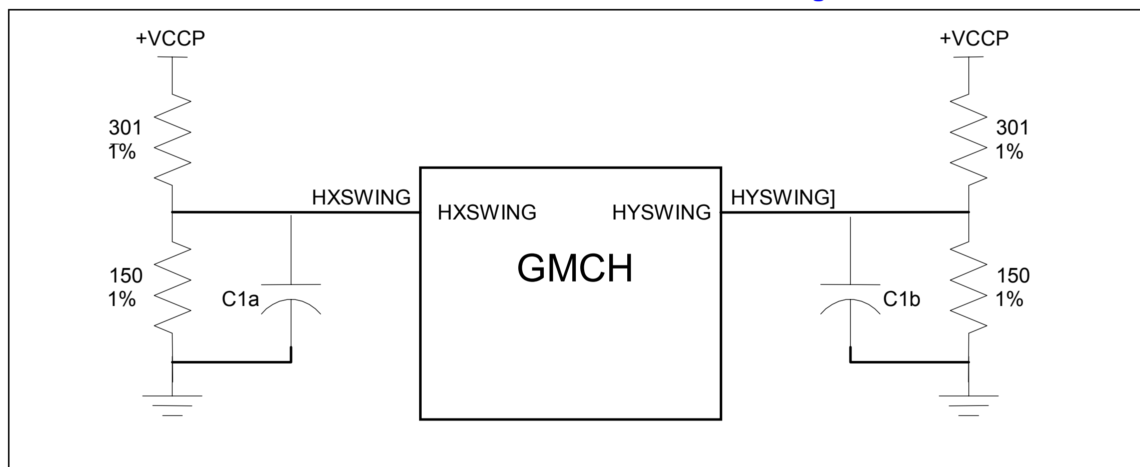
14.7.1.3. SODIMM Decoupling Recommendation

Pin Name	F	Qty	Notes	✓
Vcc1_25	0.1 µF 0.01 µF		Place one 0.1 µF cap and one 0.01 µF close to every 4 pull-up resistors terminated to Vcc1_25 (VTT for DDR signal termination). In S3, Vcc1_25 is powered OFF.	
Vcc2_5Sus	0.1 µF 100-150 µF	9 4	A minimum of 9 high frequency caps are recommeneded to be placed bewteen the SO-DIMMS. A minimum of 4 low frequency caps are required.	

14.7.2. FSB

Pin Name	System Pull-up/Pull-down	Notes	✓
HXSWING, HYSWING	301Ω 1% pull-up to VCCP 150 Ω 1% pull-down to gnd	Signal voltage level = 1/3 of VCCP. C1a=0.1 µF. C1b=0.1 µF. Trace should be 10-mil wide with 20-mil spacing. See Figure 142.	
HXRCOMP, HYRCOMP	27.4 Ω 1% pull down to gnd	One pulled-down resistor per pin. Trace should be 10-mil wide with 20-mil spacing.	
HDVREF[2:0]	49.9 Ω 1% pull-up to VCCP 100 Ω 1% pull-down to gnd	Signal voltage level = 2/3 of VCCP. Need one 0.1 µF cap and one 1 µF cap for voltage divider.	
HAVREF	49.9 Ω 1% pull-up to VCCP 100 Ω 1% pull-down to gnd	Signal voltage level = 2/3 of VCCP. Need one 0.1 µF cap and one 1 µF cap for voltage divider.	
HCCVREF	49.9 Ω 1% pull-up to VCCP 100 Ω 1% pull-down to gnd	Signal voltage level = 2/3 of VCCP. Need one 0.1 µF cap and one 1 µF cap for voltage divider.	

Figure 142. Intel 852GM GMCH HXSWING and HYSWING Reference Voltage Generation Circuit



14.7.3. Hub Interface

Pin Name	System Pull-up/Pull-down	Notes	✓
HLVREF	See Section14.8.9.	Signal voltage level = 0.35 V ± 8%.	
PSWING	See Section14.8.9.	Signal voltage level = 2/3 of VCC1_2 or 0.8 V ± 8%.	
HLZCOMP	27.4 Ω 1% pull-up to Vcc1_2		

14.7.4. Graphics Interfaces

14.7.4.1. LVDS

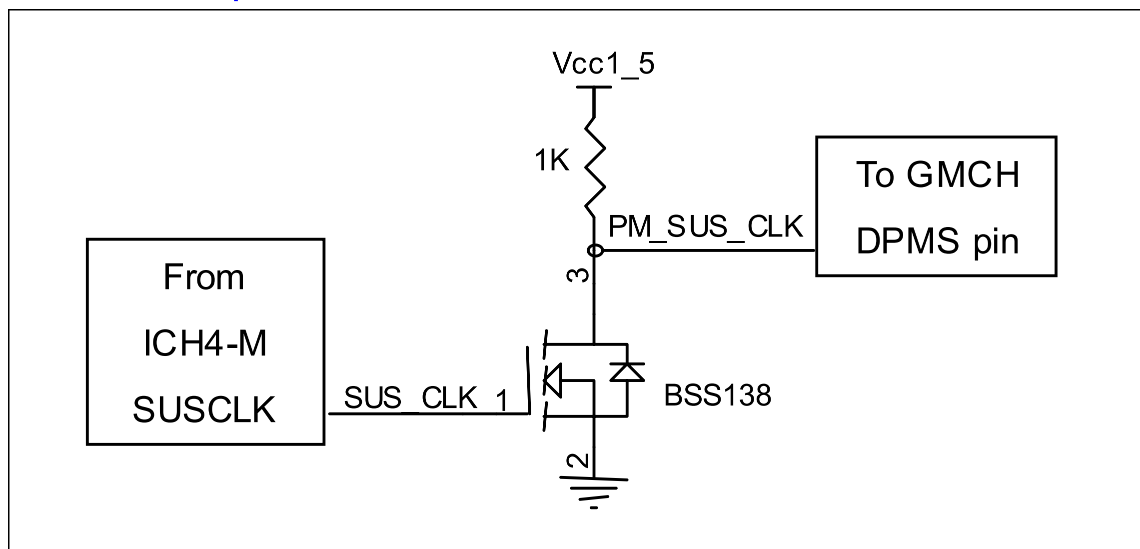
Pin Name	System Pull-up/Pull-down	Notes	✓
LIBG	1.5 kΩ 1% pull-down to gnd		
YAP[3:0]/YAM[3:0] YBP[3:0]/YBM[3:0]		If any of these LVDS data pairs are unused, they can be left as "no connect."	
CLKAP/CLKAM CLKBP/CLKBM		If any of these LVDS clock pairs are not used, they can be left as "no connect."	
LVREFH, LVREFL, LVBG		These signals should be left as NC.	

14.7.4.2. DVO

Pin Name	System Pull-up/Pull-down	Notes	✓
DVORCOMP	40.2 Ω 1% pull-down to gnd	Trace should be 10-mil wide with 20-mil spacing.	
GVREF	1 kΩ 1% pull-up to Vcc1_5 1 kΩ 1% pull-down to gnd	Signal voltage level = 1/2 of Vcc1_5. Need 0.1 µF cap at pin.	
DVOCD[11:0] DVOCCLK DVOCCLK# DVOCHSYNC DVOCVSYNC DVOCBLANK#		If unused, these signals can be left as NC.	
DVOCFLDSTL	100 kΩ pull-down to gnd	Pull-down resistor required only if signal is unused (10 k-100 k). It is up to DVO device to drive this signal.	
DVOBCINTR#	100 kΩ pull-up to Vcc1_5	Pull-up resistor required only if signal is unused (10 k-100 k). It is up to the DVO device to drive this signal.	
DVOBCCLKINT	100 kΩ pull-down to gnd	Pull-down resistor required only if signal is unused (10 k-100 k). It is up to the DVO device to drive this signal.	

Pin Name	System Pull-up/Pull-down	Notes	✓
DVOBD[11:0] DVOBCLK DVOBCLK# DVOBHSYNC DVOBVSYNC DVOBBLANK#		Intel 852GM GMCH supports only one DVO port. So, these signals should be left as NC.	
DVOBFLDSTL (pin M2)	100 kΩ pull-down to gnd	For Intel 852GM GMCH, pull-down resistor required on this signal (10 k-100 k).	
MI2CCLK, MI2CDATA	2.2 kΩ pull-up to Vcc1_5	Pull-up resistor required on each signal even if they are unused (2.2 k-100 k). This signal is 1.5 V tolerant. It may require voltage translation circuit.	
MDVICLK, MDVIDATA	2.2 kΩ pull-up to Vcc1_5	Pull-up resistor required on each signal even if they are unused (2.2 k-100 k). This signal is 1.5 V tolerant. It may require voltage translation circuit.	
MDDCCLK, MDDCDATA	2.2 kΩ pull-up to Vcc1_5	Pull-up resistor required on each signal even if they are unused (2.2 k-100 k). This signal is 1.5 V tolerant. It may require voltage translation circuit.	
ADDID[6:0]		Leave as NC.	
ADDID7	1 kΩ pull-down to gnd if DVO device is onboard	If DVO interface is not used, this signal can be left as "no connect". Otherwise, pull-down is needed.	
DVODETECT	1 kΩ pull-up to Vcc1_5 if DVO interface is unused	If DVO interface is used, leave as NC. This signal has internal pull-down.	
DPMS		Connect to 1.5 V version of ICH4-M's SUSCLK or a clock that runs during S1. See Figure 143.	

Figure 143. DPMS Clock Implementation



14.7.4.3. DAC

Pin Name	System Pull-up /Pull-down	In Series	Notes	✓
REFSET	127 Ω 1% pull-down to gnd			
RED #	Connect to gnd		Need to connect to RED's return path	
BLUE #	Connect to gnd		Need to connect to BLUE's return path	
GREEN#	Connect to gnd		Need to connect to GREEN's return path	
RED	On GMCH side of ferrite bead: 75 Ω 1% pull-down to gnd, 3.3 pF cap to gnd, ESD diode protection for Vcc1_5 On VGA side of ferrite bead: 3.3 pF cap to gnd	Ferrite bead: 75 Ω at 100 MHz	Ferrite bead for EMI suppression between GMCH and VGA connector.	
BLUE	On GMCH side of ferrite bead: 75 Ω 1% pull-down to gnd, 3.3 pF cap to gnd, ESD diode protection for Vcc1_5 On VGA side of ferrite bead: 3.3 pF cap to gnd	Ferrite bead: 75 Ω at 100 MHz	Ferrite bead for EMI suppression between GMCH and VGA connector.	
GREEN	On GMCH side of ferrite bead: 75 Ω 1% pull-down to gnd, 3.3 pF cap to gnd, ESD diode protection for Vcc1_5 On VGA side of ferrite bead: 3.3 pF cap to gnd	Ferrite bead: 75 Ω at 100 MHz	Ferrite bead for EMI suppression between GMCH and VGA connector.	
HSYNC	On VGA side of seires resistor: 33 pF cap to gnd	39 Ω	Use unidirectional buffer to prevent potential electrical overstress and illegal operation of the GMCH.	
VSYNC	On VGA side of series resistor: 33 pF cap to gnd	39 Ω	Use to unidirectional buffer to prevent potential electrical overstress and illegal operation of the GMCH.	

14.7.5. Miscellaneous

Pin Name	System Pull-up/Pull-down	Notes	✓
EXTTS	10 kΩ 1% pull-up to Vcc3_3		
DPWR# (pin AA22)		Connect to DPWR# pin of Intel Celeron M processor. Leave as NC for all other processors.	
LCLKCTLB	1 kΩ pull-up to Vcc3_3 for Intel 852GM GMCH.	Strap option for Mobile Intel® Pentium® 4 Processor-M	
LCLKCTLA		Leave as NC if not used.	
GST1, GST0	Leave as NC or 1 kΩ pull-up to Vcc1_5	These pins have internal pull-down. See Table 99 below for configuration options.	

Table 99. GST[1:0] Configurations

GMCH GST[1:0] Configuration	FSB	DDR	Gfx Core Clock Low	Gfx Core Clock High
00	400	266	N/a	133
10	400	200	N/a	133

14.7.6. GMCH Decoupling Recommendations

Pin Name	Configuration	F	Qty	Notes	✓
VCC	Connect to Vcc1_2	0.1 µF 150 µF 10 µF	4 2 1	Bulk decoupling is based on VR solutions used on CRB design.	
VTTLF	Connect to VCCP	0.1 µF 150 µF 10 µF	2 1 1	Bulk decoupling is based on VR solutions used on CRB design.	
VTTHF		0.1 µF	5	Connect pins directly to caps.	
VCCHL	Connect to Vcc1_2	0.1 µF 10 µF	2 1	Bulk decoupling is based on VR solutions used on CRB design.	
VCCSM	Connect to VccSus2_5	0.1 µF 150 µF	11 2	Bulk decoupling is based on VR solutions used on CRB design.	
VCCQSM	Connect to VccSus2_5 with filter network	0.1 µF 4.7 µF+1Ω	1 1 each	0.68 µH from power supply to GMCH pins. On GMCH side of inductor: one 0.1 µF to GND, 4.7 µF + 1 Ω to GND	
VCCASM	Connect to Vcc1_2 with filter network	0.1 µF 100 µF	1 1	1 µH from power supply to GMCH pins, with caps on GMCH side of inductor.	
VCCDVO	Connect to Vcc1_5	0.1 µF 10 µF 150 µF	2 1 1	Bulk decoupling is based on VR solutions used on CRB design.	
VCCADAC	Connect to Vcc1_5	0.01 µF 0.1 µF 220 µF (no stuff)	1 1 1	Route VSSADAC to other side of the caps, then to ground. A 0-ohm 0805 resisor is recommended between the caps and Vcc1_5. This and the 220 µF cap footprints are there in case there is noise issue with the VGA supply.	
VCCALVDS	Connect to Vcc1_5	0.1 µF 0.01 µF	1 1	Route VSSALVDS to other side of the caps, then to ground.	
VCCDLVDS	Connect to Vcc1_5	0.1 µF 22 µF 47 µF	1 1 1	Bulk decoupling is based on VR solutions used on CRB design.	
VCCTXLVDS	Connect to VccSus2_5	0.1 µF 22 µf 47 µF	3 1 1	Bulk decoupling is based on VR solutions used on CRB design. This power signal may be optionally connected to Vcc2_5 and powered off in S3.	
VCCGPIO	Connect to Vcc3_3	0.1 µF 10 µF	1 1	Bulk decoupling is based on VR solutions used on CRB design.	

Pin Name	Configuration	F	Qty	Notes	✓
VCCAHPLL	Connect to VCC1_2	0.1 µF	1		
VCCAGPLL	Connect to VCC1_2	0.1 µF	1		
VCCADPLLA	Connect to VCC1_2 with filter network	0.1 µF 220 µF	1 1	0.1 µH from power supply to GMCH pins, with caps on GMCH side of inductor.	
VCCADPLLB	Connect to VCC1_2 with filter network	0.1 µF 220 µF	1 1	0.1 µH from power supply to GMCH pins, with caps on GMCH side of inductor.	

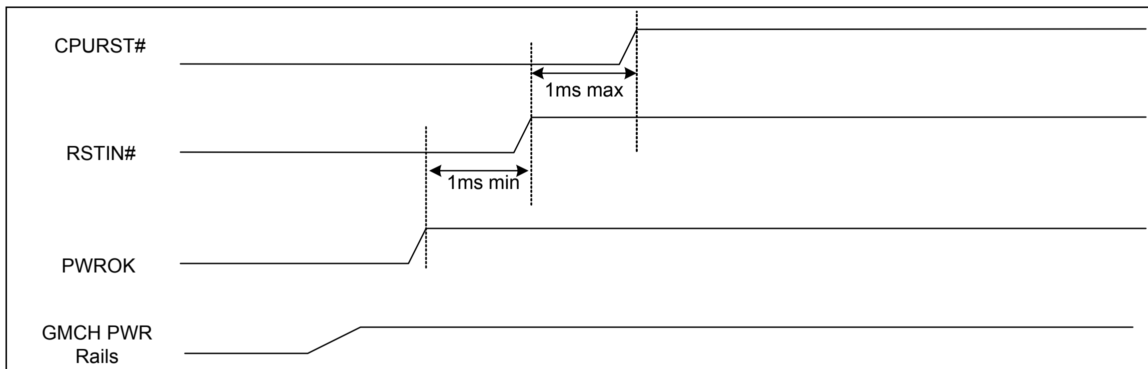
NOTE: Decoupling guidelines are recommendations based on our reference board design. Customers will need to take layout and PCB board design into consideration when deciding on overall decoupling solution.

14.7.7. GMCH Power-up Sequence

Table 100. Intel 852GM GMCH Power-up Timing Specifications

Timing Parameters	Min	Max	Unit	Notes	✓
PWROK active to RSTIN# inactive.	1		ms	See Figure 144	
RSTIN# inactive to CPURST# inactive.		1	ms	See Figure 144	

Figure 144. Intel 852GM GMCH Power-up Sequence



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14.8. ICH4-M Checklist

Note: All inputs to the ICH4-M must not be left floating. Many GPIO signals are fixed inputs that must be pulled up to different sources.

14.8.1. PCI Interface and Interrupts

Pin Name	System Pull-up /Pull-down	Notes	✓
PCI_DEVSEL#	8.2 kΩ pull-up to Vcc3_3		
PCI_FRAME#	8.2 kΩ pull-up to Vcc3_3		
PCI_GPIO0 / REQA# PCI_GPIO1 / REQB_L/REQ5#	8.2 kΩ pull-up to Vcc3_3	Each signal requires a pull-up resistor.	
PCI_GPIO16 / GNTA#		GNTA is also used as a strap for “top block swap”. It is sampled on the rising edge of PWROK. By default, this signal is HIGH (strap function DISABLED). It can be enabled by a pull-down to gnd through a 1-kΩ resistor.	
PCI_IRDY#	8.2 KΩ pull-up to Vcc3_3		
PCI_LOCK#	8.2 KΩ pull-up to Vcc3_3		
PCI_PERR#	8.2 KΩ pull-up to Vcc3_3		
PCI_SERR#	8.2 KΩ pull-up to Vcc3_3		
PCI_STOP#	8.2 KΩ pull-up to Vcc3_3		
PCI_TRDY#	8.2 KΩ pull-up to Vcc3_3		
PCI_REQ[4:0]#	8.2 KΩ pull-up to Vcc3_3	Each signal requires a pull-up resistor.	
PCI_PME#		ICH4-M has internal pull-up to VccSus3_3.	
PCI_RST#, PAR, GNT[4:0]#, GNTA#, GNTB#	None		
APICCLK	0 Ω to gnd	Can also be connected directly to ground.	
APICD[1:0]	10 kΩ pull-down to gnd	If XOR chain testing is **NOT** used: Pull down the signals through a shared 10 kΩ resistor. If XOR chain testing is used: Each signal requires a separate 10 kΩ pull-down resistor.	
INT_IRQ[15:14]	8.2 kΩ pull-up to Vcc3_3	Each signal requires a pull-up resistor.	
INT_PIRQ#[A:D] INT_PIRQE#/GPIO2 INT_PIRQF#/GPIO3 INT_PIRQG#/GPIO4 INT_PIRQH#/GPIO5	8.2 kΩ pull-up to Vcc3_3	Extneral pull up is required for INT_PIRQ#[A:D]. External pull up is required when muxed signal (INT_PIRQ[E:H]#/ GPIO[2:5]) is implemented as PIRQ.	
INT_SERIRQ	8.2 kΩ pull-up to Vcc3_3		

14.8.2. GPIO

Note: Ensure ALL unconnected signals are OUTPUTS ONLY. Only GPIO[7:0] are 5-V tolerant.

Recommendations	✓
GPIO[7] & [5:0]: • These pins are in the Main Power Well. Pull-ups must use the V_{CC}3_3 plane. • Unused core well inputs must be pulled up to V_{CC}3_3. • GPIO[1:0] can be used as REQ[B:A]#. • GPIO[1] can be used as PCI REQ[5]#. • GPIO[5:2] can be used as PIRQ[H:E]#. • These signals are 5 V tolerant. • These pins are inputs.	
GPIO[8] & [13:11]: • These pins are in the Resume Power Well. Pull-ups go to V_{CC}Sus3_3 plane. • Unused resume well inputs must be pulled up to V_{CC}Sus3_3. • These are the only GPIs that can be used as ACPI compliant wake events. • These signals are not 5 V tolerant. • GPIO[8] can be used as SMC_EXTSMI# • GPIO[11] can be used as SMBALERT#. • GPIO[13] can be used as SMC_WAKE_SCI# • These pins are inputs	
GPIO[23:16]: • Fixed as output only. Can be left NC. • In Main Power Well (V_{CC}3_3). • GPIO[17:16] can be used as GNT[B:A]#. • GPIO[17] can be used as PCI GNT[5]#. • STP_PCI#/GPIO[18] – used in mobile as STP_PCI# only. • SLP_S1#/GPIO[19] - used in mobile as SLP_S1# only. • STP_CPU#/GPIO[20] - used in mobile as STP_CPU# only. • C3_STAT#/GPIO[21] - used in mobile as C3_STAT# only. • CPUPERF#/GPIO[22] - open drain signal. Used in mobile as CPUPERF# only. • SSMUXSEL/GPIO[23] - used in mobile as SSMUXSEL only.	
GPIO[28,27,25,24]: • I/O pins. Default as outputs. Can be left as NC. • These pins are in the Resume Power Well. • CLKRUN#/GPIO[24] (Note: use V_{CC}3_3 if signal is required to be pulled-up) • GPIO[28, 27, 25] From resume power well (V_{CC}Sus3_3). (Note: use V_{CC}3_3 if this signal is required to be pulled-up) • These signals are NOT 5-V tolerant.	

Recommendations	✓
• GPIO[25] can be used as AUDIO_PWRDN.	
GPIO[43:32]: • I/O pins. From main power well (V_{CC}3_3). • Default as outputs when enabled as GPIOs. • These signals are **NOT** 5-V tolerant. • GPIO[32] can be used as AGP_SUSPEND#. • GPIO[33] can be used as KSC_VPPEN#. • GPIO[34] can be used as SER_EN. • GPIO[35] can be used as FWH_WP#. • GPIO[36] can be used as FWH_TBL#. • GPIO[40] can be used as IDE_PATADET. • GPIO[41] can be used as IDE_SATADET.	

14.8.3. AGP_BUSY# Design Requirement

Signal	System Pull-up/Pull-down	Notes	✓
AGPBUSY#	10 KΩ pull-up to Vcc3_3	This ICH4-M signal requires a pull-up to the switched 3.3-V rail (powered OFF during S3). This ICH4-M signal must be connected to the AGP_BUSY# output of GMCH.	

NOTE: Please also consult Intel for the latest AGP Busy and Stop signal implementation.

14.8.4. (SMBus) System Management Interface

Pin Name	System Pull-up/Pull-down	Notes	✓
SM_INTRUDER#	100 kΩ pull-up to VccRTC	RTC well input requires pull-up (10 k-100 k) to reduce leakage from coin cell battery in G3.	
SMB_ALERT#/ GPIO[11]	10 kΩ pull-up to V3ALWAYS		
SMBCLK, SMBDATA, SMLINK[1:0]	Pull-up to V3ALWAYS	Require external pull-up resistors. Pull up value is determined by bus characteristics. CRB schematics use 10 kΩ pull-up resistors. The SMBus and SMLink signals must be connected together externally in S0 for SMBus 2.0 compliance: SMBCLK connected to SMLink[0] and SMBDATA connected to SMLink[1].	

14.8.5. AC ’97 Interface

Pin Name	System Pull-up/Pull-down	Series Termination Resistor	Notes	✓
AC_BIT_CLK	None	33-47 Ω	The internal pull-down resistor is controlled by the AC’97 Global Control Register, ACLINK Shut Off bit: 1 = enabled; 0 = disabled When no AC'97 devices are connected to the link, BIOS must set the ACLINK Shut Off bit for the internal keeper resistors to be ENABLED. At that point, pull-ups/pull-downs are NOT needed on ANY of the link signals.	
AC_SDATAIN[2:0]	None	33-47 Ω	A series termination resistor is required for the PRIMARY CODEC. A series termination resistor is required for the SECONDARY and TERTIARY CODEC if the resistor is not found on CODEC.	
AC_SDATAOUT	None	33-47 Ω	A series termination resistor is required for the PRIMARY CODEC. One series termination resistor is required for the SECONDARY/ TERTIARY CODEC connector card if the resistor is not found on the connector card.	
AC_SYNC	None	33-47 Ω	A series termination resistor is required for the PRIMARY CODEC. One series termination resistor is required for the SECONDARY/ TERTIARY CODEC connector card if the resistor is not found on the connector card.	

14.8.6. ICH4-M Power Management Interface

Pin Name	System Pull-up/Pull-down	Notes	✓
PM_DPRSLPVR		Signal has integrated pull-down in ICH4-M.	
PM_SLP_S1#/GPIO19 PM_SLP_S3#, PM_SLP_S4#, PM_SLP_S5#		Signals driven by ICH4-M.	
PM_BATLOW#	10 kΩ pull-up to V3ALWAYS IF NOT USED	Pull up is not required if it is used. However, signal must not float if it is NOT being used	
PM_CLKRUN#	10 kΩ pull-up to Vcc3_3		
PM_PWRBTN#		Has integrated pull-up of 18 kΩ – 42 kΩ.	
PM_PWROK	Weak pull-down to gnd	RTC well input requires pull-down to reduce leakage from coin cell battery in G3. Input must not float in G3. This signal should be connected to power monitoring logic and should go high no sooner than 10 ms after both Vcc3_3 and Vcc1_5 have reached their nominal voltages. CRB uses 100 kΩ pull-down.	
PM_RI#	8.2 kΩ-10 kΩ pull-up to V3ALWAYS	If this signal is enabled as a wake event, it needs to be powered during a power loss event. If this signal goes low (active), when power returns the RI_STS bit will be set and the system will interpret that as a wake event.	
PM_RSMRST#	Weak pull-down to gnd	RSMRST# is a RTC well input and requires pull-down to reduce leakage from coin cell battery in G3. Input must not float in G3. This signal should be connected to power monitoring logic and should go high no sooner than 10 ms after both Vcc3_3 and Vcc1_5 have reached their nominal voltages. CRB uses 100 kΩ pull-down. Timing Requirement: See LAN_RST#.	
PM_THRM#	8.2 kΩ Pull-up to Vcc3_3 If TEMP SENSOR not sued	External pull-up not required if connecting to temperature sensor.	
PM_SYSRST#	10 kΩ pull-up to V3ALWAYS if not actively driven.	This signal to ICH4-M should not float. It needs to be at valid level all the time.	

14.8.7. FWH/LPC Interface

Pin Name	System Pull-up/Pull-down	Notes	✓
LPC_AD[3:0]		No extra pull-ups required. Connect straight to FWH/LPC.	

14.8.8. USB Interface

Pin Name	System Pull-up/Pull-down	Notes	✓
USB_OC[5:0]#	10 kΩ pull-up to V3ALWAYS if not driven	No pull-up is required if signalsl are driven.. Signals must NOT float if they are not being used.	
USBRBIAS, USBRBIAS#	22.6 Ω ± 1% pull-down to gnd	Connect signals together and pull down through a common resistor, placed within 500 mils of the ICH4-M. Avoid routing next to clock pin.	

14.8.9. Hub Interface

Pin Name	System Pull-up/Pull-down	Notes	✓
HUB_RCOMP	48.7 Ω 1% pull-up to to Vcc1_5	Place resistor within 0.5" of ICH4-M pad using a thick trace.	
HUB_VREF, HUB_VSWING	See Figure 145 and Figure 146.	HUB_VREF signal voltage level = 0.35 V ± 8%. HUB_VSWING signal voltage level = 0.80 V ± 8%. Three options are available for generating these references.	
HUB_PD11	56 Ω pull-down to gnd		

Figure 145. Single or Locally Generated GMCH & ICH4-M HIVREF/HI_VSWING Circuit

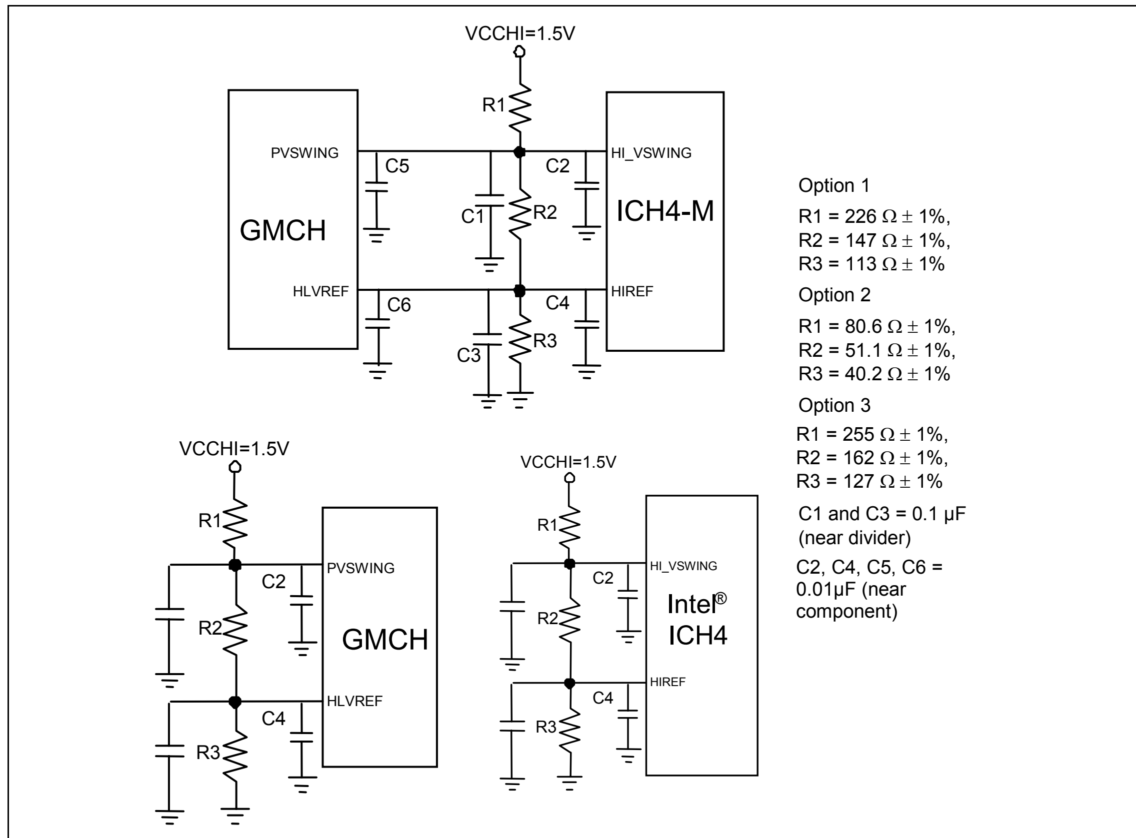
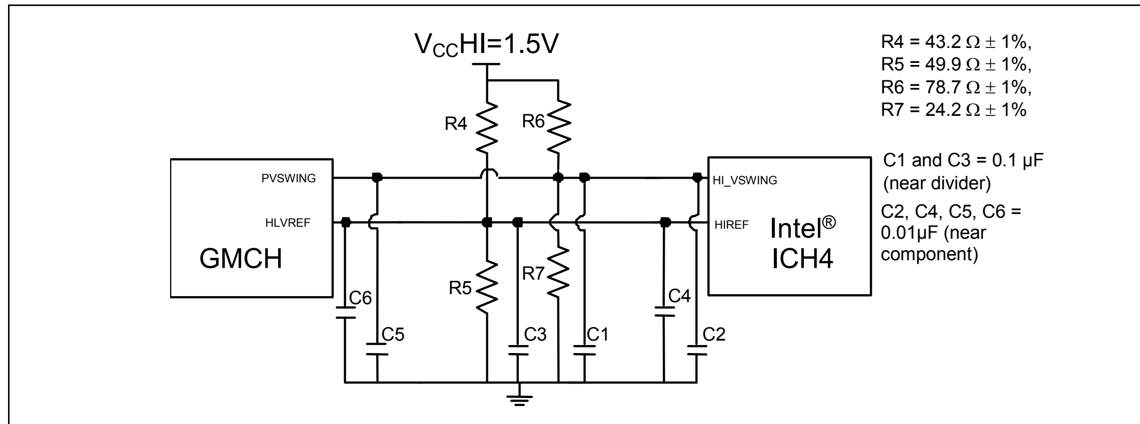


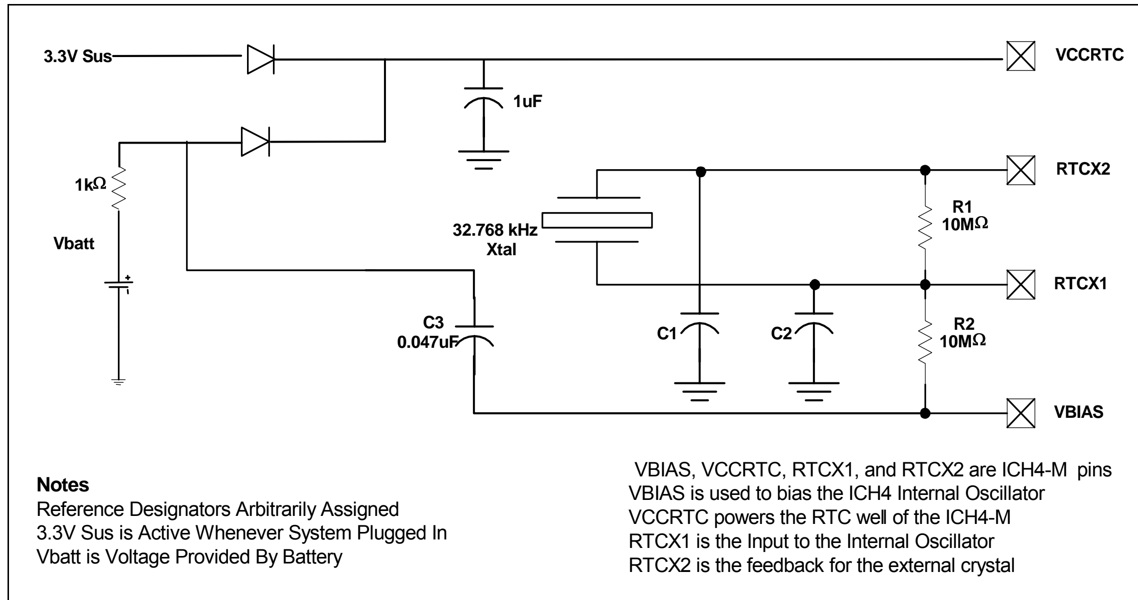
Figure 146. Single Generated GMCH & ICH4-M VSWING/VREF Reference Voltage/ Local Voltage Divider Circuit for VSWING/VREF



14.8.10. RTC Circuitry

Pin Name	System Pull-up/Pull-down	In Series	Notes	✓
RTCRST#	180 kΩ pull-up to VccRTC		RTCRST# requires 18-25 ms delay. Use a 0.1 µF cap to ground Pull up with 180 kΩ resistor. Any resistor or capacitor combination that yields a time constant is acceptable.	
CLK_RTCX1, CLK_RTCX2			Connect a 32.768 kHZ crystal oscillator across these pins with a 10 MΩ resistor and a decoupling cap at each signal. Values for C1 and C2 are dependent on crystal. See Figure 147.	
CLK_VBIAS		1 KΩ 0.047 µF	Connect to CLK_RTCX1 through a 10 MΩ resistor. Connect to VBATT through a 1 kΩ in series with a 0.047 µF capacitor.	

Figure 147. External Circuitry for the RTC



14.8.11. LAN Interface

Pin Name	System Pull-up/Pull-down	Notes	✓
LAN_JCLK		Connect to LAN_CLK on the platform LAN Connect Device. If LAN interface is not used, leave the signal unconnected (NC).	
LAN_RST#	10 kΩ pull-down to gnd If ICH4-M LAN not used	Timing Requirement: Signal should be connected to power monitoring logic, and should go high no sooner than 10 ms after both VccSus3_3 and VccSus1_5 have reached their nominal voltages. **NOTE**: If ICH4-M LAN controller is NOT used, pull LAN_RST# down through a 10 kΩ resistor.	
LAN_RXD[2:0], LAN_TXD[2:0]		Connect to LAN_RXD on the platform LAN Connect Device. If LAN interface is not used, leave the signal unconnected (NC)	
LAN_RSTYSNC		Connect to LAN_RSTSYNC on Platform LAN Connect Devce. If LAN interface is not used, leave the signal unconnected (NC).	

14.8.12. Primary IDE Interface

Pin Name	System Pull-up/Pull-down	Series Damping	Notes	✓
IDE_PDD[15:0]			These signals have integrated series resistors.	
IDE_PDA[2:0], IDE_PDCS1#, IDE_PDCS3#, IDE_PDDACK#, IDE_PDIOW#, IDE_PDIOR#			These signals have integrated series resistors. Pads for series resistors can be implemented should the system designer have signal integrity concerns.	
IDE_PDDREQ			These signals have integrated series resistors and pull-down resistors in ICH4-M.	
IDE_PIORDY	4.7 kΩ pull-up to Vcc3_3		This signal has integrated series resistor in ICH4-M.	
IDE_PRST#		22-47 Ω	The signal must be buffered to provide IDE_RST# for improved signal integrity.	

14.8.13. Secondary IDE Interface

Pin Name	System Pull-up/Pull-down	Series Damping	Notes	✓
IDE_SDD[15:0]			These signals have integrated series resistors.	
IDE_SDA[2:0], IDE_SDCS1#, IDE_SDCS3#, IDE_SDDACK#, IDE_SDIOW#, IDE_SDIOR#			These signals have integrated series resistors. Pads for series resistors can be implemented should the system designer have signal integrity concerns.	
IDE_SDDREQ			These signals have integrated series resistors and pull-down resistors in ICH4-M.	
IDE_SIORDY	4.7 kΩ pull-up to Vcc3_3		This signal has integrated series resistor in ICH4-M.	
IDE_SRST#		22-47 Ω	The signal must be buffered to provide IDE_RST# for improved signal integrity..	

14.8.14. Miscellaneous Signals

Pin Name	System Pull-up/Pull-down	Notes	✓
SPKR		SPKR is a strapping option for the TCO Timer Reboot function and is sampled on the rising edge of PWROK. An integrated weak pull-down is enabled only at boot/reset. Status of strap is readable via the NO_REBOOT bit (D31:F0, Offset D4h, bit 1). 1 = disabled 0 = enabled (normal operation) To disable, a jumper can be populated to pull SPKR high. Value of pull-up must be such that the voltage divider output caused by the pull-up, effective impedance of speaker and codec circuit, and internal pull-down will be read as logic high (0.5 * Vcc3_3 to Vcc3_3 + 0.5).	

14.8.15. ICH4-M Decoupling Recommendations

Pin Name	Configuration	Value	Q	Notes	✓
VCC1.5	Connect to Vcc1_5	0.1 µF	2	Low frequency decoupling is dependent on layout and power supply design. CRB uses one 22 µF and one 100 µF.	
VCC3.3	Connect to Vcc3_3	0.1 µF	6	Low frequency decoupling is dependent on layout and power supply design. CRB uses two 22 µF.	
VCCSUS1.5	Connect to V1_5ALWAYS	0.1 µF	2	Low frequency decoupling is dependent on layout and power supply design. CRB uses one 10 µF.	
VCCSUS3.3	Connect to V3ALWAYS	0.1 µF	2	Low frequency decoupling is dependent on layout and power supply design. CRB uses one 22 µF.	
VCCLAN1.5	Connect to VccSus1_5	0.1 µF	2	Low frequency decoupling is dependent on layout and power supply design. CRB uses one 22 µF.	
VCCLAN3.3	Connect to VccSus3_3	0.1 µF 4.7 µF	2 1	Low frequency decoupling is dependent on layout and power supply design. CRB uses one 22 µF.	
VCC5REF	Connect to Vcc5 through 1KΩ	0.1 µF 1 µF	1 1	Caps from VCC5REF to ground. Also connect diode from VCC5REF to Vcc3_3.	
VCC5REFSUS	Connect to V5ALWAYS through 1KΩ	0.1 µF 1 µF	1 1	Caps from VCC5REFSUS to ground. Also connect diode from VCC5REFSUS to V3ALWAYS.	
VCC_CPU_IO	Connect to VCCP	0.1 µF 1 µF	1 1		
VCCPLL	Connect to Vcc1_5	0.1 µF 0.01 µF	1 1		
VCCRTC	Connect to VccRTC	0.1 µF	1		
VCCHI	Connect to Vcc1_5	0.1 µF	2	Low frequency decoupling is dependent on layout and power supply design. CRB uses one 22 µF.	

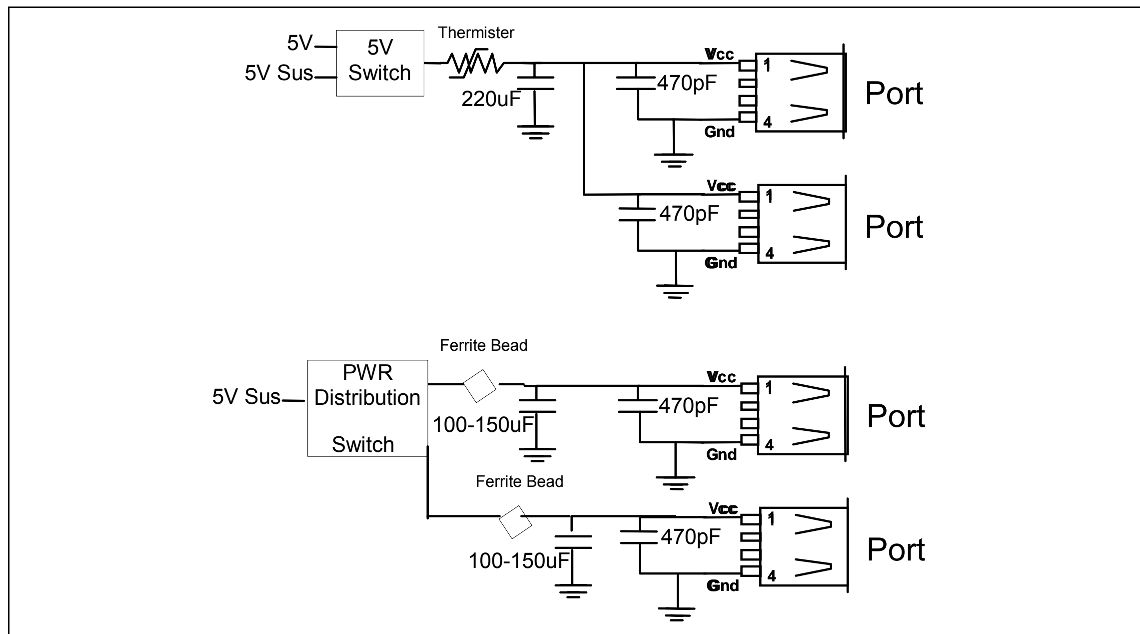
NOTE: All decoupling guidelines are recommendations based on our reference board design. Customers will need to take their layout and PCB board design into consideration when deciding on their overall decoupling solution. Capacitors should be place less than 100 mils from the package.

14.9. USB Power Checklist

14.9.1. Downstream Power Connection

Pin Name	Notes	✓
USB_VCC[E:A]	One 220 µF and two 470 pF are recommended for every two power lines. Either a thermister or a power distribution switch (with short circuit and thermal protection) is required. See Figure 148.	

Figure 148. Good Downstream Power Connection



14.10. FWH Checklist

14.10.1. Resistor Recommendations

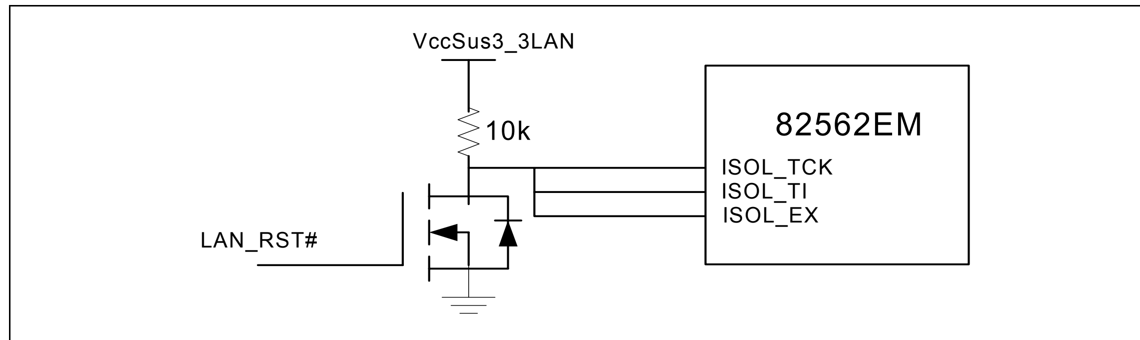
Pin Name	System Pull-up/Pull-down	Series Damping	Notes	✓
FGPI[4:0]	100 Ω pull-down to gnd		Each signal requires a 100 Ω pull-down resistor.	
IC	10 kΩ pull-down to gnd			
RST#		100 Ω		
ID[3:0]			Signals are recommended to be connected to test points.	
RSVD[5:1]			Signals are recommended to be connected to test points.	
NC[8:1]			The signals should be left as NC ("Not Connected")	

14.11. LAN / HomePNA Checklist

14.11.1. Resistor Recommendations (for 82562ET / 82562EM)

Pin Name	System Pull-up/Pull-down	Term Resistor	Notes	✓
ISOL_EX, ISOL_TCK, ISOL_TI	10 kΩ pull-up to VccSus3_3LAN		If LAN is enabled, all three signals needs to be pulled up to VccSus3_3LAN through a common 10 KΩ pull-up resistor. See Figure 149.	
RBIAS10	549 Ω ± 1%pull-down to gnd			
RBIAS100	619 Ω ± 1%pull-down to gnd			
RDP, RDN		121 Ω ±1%	Connect 121-ohm resistor between RDP and RDN.	
TDP, TDN		100 Ω ± 1%	Connect 100-ohm resistor between TDP and TDN.	
TESTEN	100 Ω pull-down to gnd			
X1, X2			Connect a 25-MHz crystal across these two pins. 22pF on each pin to ground.	
LAN_RST#			On CRB, the power monitoring logic waits for PM_PWROK to go high before deasserting this signal to enable the LAN device. It also keeps this signal high during S3. See Figure 149.	

Figure 149. LAN_RST# Design Recommendation



14.11.2. Decoupling Recommendations

Signal Name	Configuration	F	Qty	Notes	✓
VCC[2:1], VCCP[2:1], VCCA[2:1], VCCT[4:1]	Connect to VccSus3_3LAN	0.1 µF 4.7 µF	4 2		
VCCR[2:1]	Connect to VccSus3_3LAN via filter	0.1 µF 4.7 µF	1 1	4.7 uH from power supply to VCCR pins. Caps on VCCR side of the inductor.	

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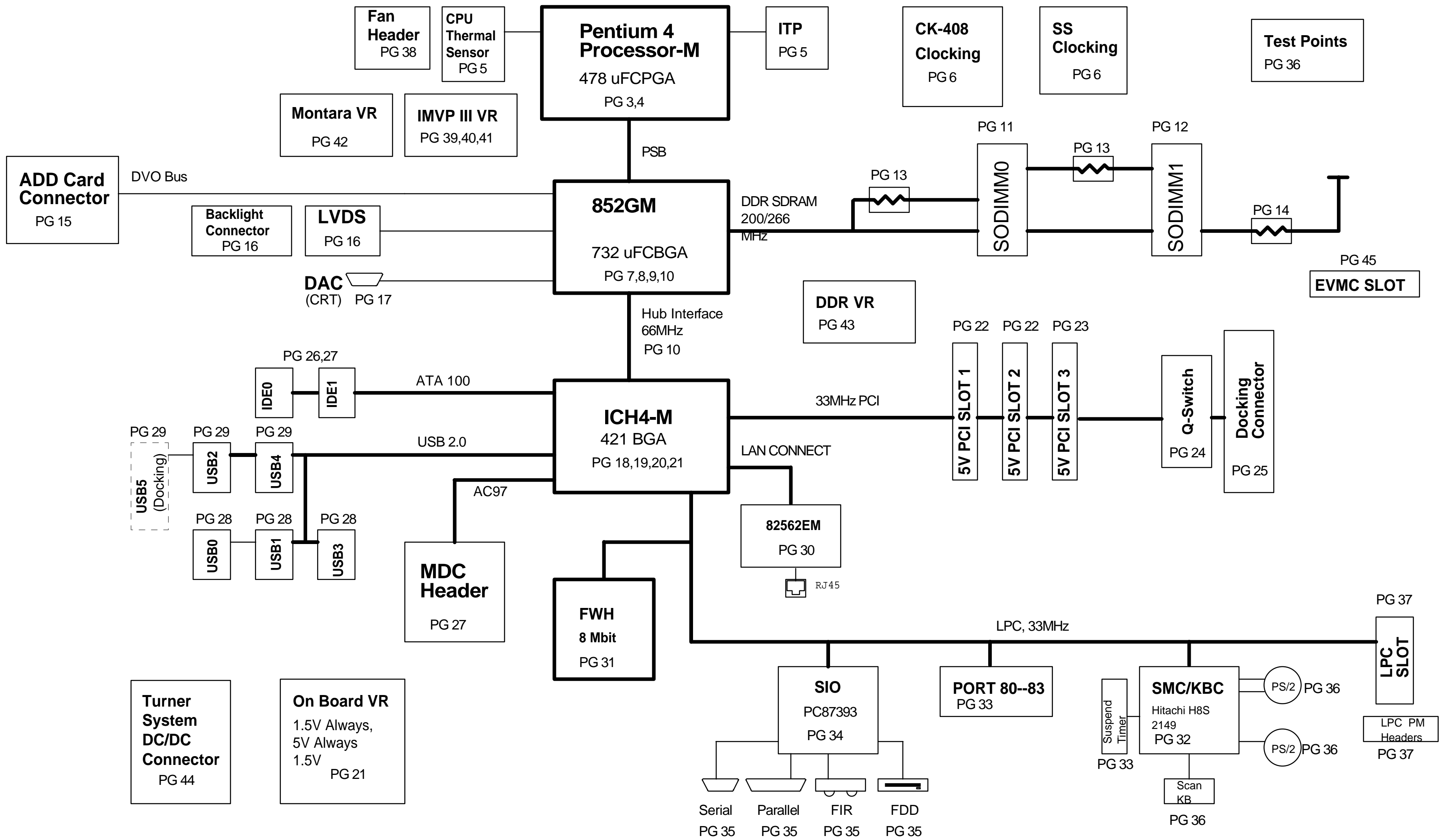
15. Schematics

See the following pages for the reference board schematics.



Title	BLOCK DIAGRAM		
Size A	Project: Intel 852GM CRB	Document Number A#	Rev
		1 of 59	

Intel 852GM CUSTOMER REFERENCE PLATFORM

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails

Rail	Description
+VDC	Primary DC system power supply (10 to 21V)
+VCC_IMVP	Core/VTT voltage for processor & VTT for Montara-GML
+VCC_VID	1.2V for processor PLL and VID circuitry
+V1.2S	1.2V for Montara-GML core/hub interface
+V1.25S	1.25V DDR Termination voltage
+V1.5S	1.5V switched power rail (off in S3-S5)
+V1.5ALWAYS	1.5V always on power rail
+V1.5	1.5V power rail (off in S4-S5)
+V2.5	2.5V power rail for DDR
+V3.3ALWAYS	3.3V always on power rail
+V3.3	3.3V power rail (off in S4-S5)
+V3.3S	3.3V switched power rail (off in S3-S5)
+V5ALWAYS	5.0V for ICH4M's VCC5REFSUS
+V5	5.0V power rail (off in S4-S5)
+V5S	5.0V switched power rail (off in S3-S5)
+V12S	12.0V switched power rail (off in S3-S5)
-V12S	-12.0V switched power rail for PCI (off in S3-S5)

I^2C / SMB Addresses

Device	Address	Hex	Bus
Clock Generator	1101 001x	D2	SMB_ICH_S
Spread Spectrum Clock	1101 010x	D4	SMB_ICH_S
SO-DIMM0	1010 000x	A0	SMB_ICH_S
SO-DIMM1	1010 001x	A2	SMB_ICH_S
Thermal Sensor Header	1001 000x	90	SMB_ICH
LVDS Backlight Inverter	____ ____	__	SMB_ICH
Dock Connector	____ ____	__	SMB_ICH
Smart Battery	0001 011x	16	SMB_SB
Smart Battery Charger	0001 001x	12	SMB_SB
Smart Selector	0001 010x	14	SMB_SB
Bluetooth Header	____ ____	__	SMB_SB
LPC Pwr Mngmnt Header	____ ____	__	SMB_SB
LPC Pwr Mngmnt Header	____ ____	__	SMB_THRM
Thermal Diode	1001 110x	9C	SMB_THRM
EV Support:			
DV0-DV3	0101 0001	51	SMB_ICH
V5-V8	0101 0010	52	SMB_ICH
PV0-PV3	0101 0011	53	SMB_ICH
DV4	0101 0100	54	SMB_ICH
V9-V12	0101 0101	55	SMB_ICH
I1-I4	0101 0110	56	SMB_ICH
EP1-EP4	0101 0111	57	SMB_ICH
PV4	0101 0100	58	SMB_ICH
V1-V4	0101 1001	59	SMB_ICH

Default Jumper Settings

Jumper	Default	Option	Description	Page
J7B1	1-2	1-X	GMCH Strap: PSB Voltage	08
J7B3	1-X	1-2	GMCH Strap: DVO Strap	08
J7B4	1-X	1-2	GMCH Strap: Clock Config	08
J7B5	1-X	1-2	GMCH Strap: Clock Config	08
J7B6	1-X	1-2	GMCH Strap: Clock Config	08
J6E1	2-3	1-2	LVDS EV	08
J2J3	1-X	1-2	CMOS Clear	19
J8J2	2-3	1-2	CRB/SV Detect	19
J9E2	1-2	2-3	Moon ISA Support	23
J9E4	1-2	2-3	Moon ISA Support	23
J9E5	2-3	1-2	Moon ISA Support	23
J9B1	1-X	1-2	SMC/KBC Programming	32
J9A1	1-X	1-2	KBC 60/64 Decode Disable	32
J8A2	1-2	2-3	SMC/KBC Disable	32
J8A1	1-2	1-X	INIT Clock Disable	33
J9H1	1-X	1-2	Port 80-81/82-83 Select	33
J9G2	1-2	2-3	SIO Disable	34
J1F1	1-X	1-2	Manual VID Strap Enable	39
J1G1	1-2	2-3	VID0 Strap	39
J1G2	1-2	2-3	VID1 Strap	39
J1G3	1-2	2-3	VID2 Strap	39
J1G4	1-2	2-3	VID3 Strap	39
J1H1	1-2	2-3	VID4 Strap	39
J3G1	1-X	1-2 or 2-3	DDR EV Support	43
J3G2				

PCI Devices

Device	IDSEL #	REQ/GNT #		Interrupts	PC/PCI
Slot 1	AD16	1	1	F, G, H, E	A
Slot 2	AD17	2	2	G, F, E, H	A
Slot 3	AD18	3	3	C, D, B, A (E, F, G, H optional)	A
Docking	AD28	4	4	D, A, B, C	B
LAN	(AD24 internal)			(E internal)	

LEDs and Switches

LED	Page	Reference
Primary IDE	27	DS2J2
Secondary IDE	27	DS2J1
SMC/KBC Num Lock	32	DS8A1
SMC/KBC Scroll Lock	32	DS8A2
SMC/KBC Caps Lock	32	DS8B1
S0 State	38	DS1H1
S1 State	38	DS1H3
S3 State	38	DS1H2
S4 State	38	DS2H2
S5 State	38	DS2H1
VID0	39	DS1J3
VID1	39	DS1J2
VID2	39	DS1J1
VID3	39	DS2J4
VID4	39	DS2J3

Switch	Page	Reference
Virtual Battery On/Off	32	SW8A1
Lid	32	SW9A1
Power On/Off	44	SW8J1
Reset	44	SW7J1

Wake Events

- RI# (Ring Indicate) from serial port
- PME# (Power Management Event) from PCI/mini-PCI slots, ADD slot, LPC slot
- Jordan I/O from Kinnereth+
- LID switch attached to SMC
- USB
- AC97 wake on ring
- SmLink for AOL II
- Hot Key from the scan matrix keyboard

Net Naming Conventions

Suffix
- # = Active Low signal

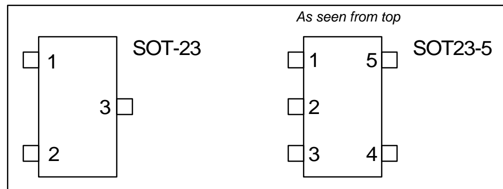
Prefix
- H = Host
- M = DDR Memory

TP = Test Point (does not connect anywhere else)

Power States

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALWAYS	+V*	+V*S	Clocks
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1M (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend To Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 / Soft OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

PCB Footprints



Title	Notes and Annotations		
Size: A	Project: Intel 852GM CRB	Document Number: A#	Rev
		2 of 59	

Note: Host Clock terminations are at the source (CK408)

Trace length: Less than 1.5 inch

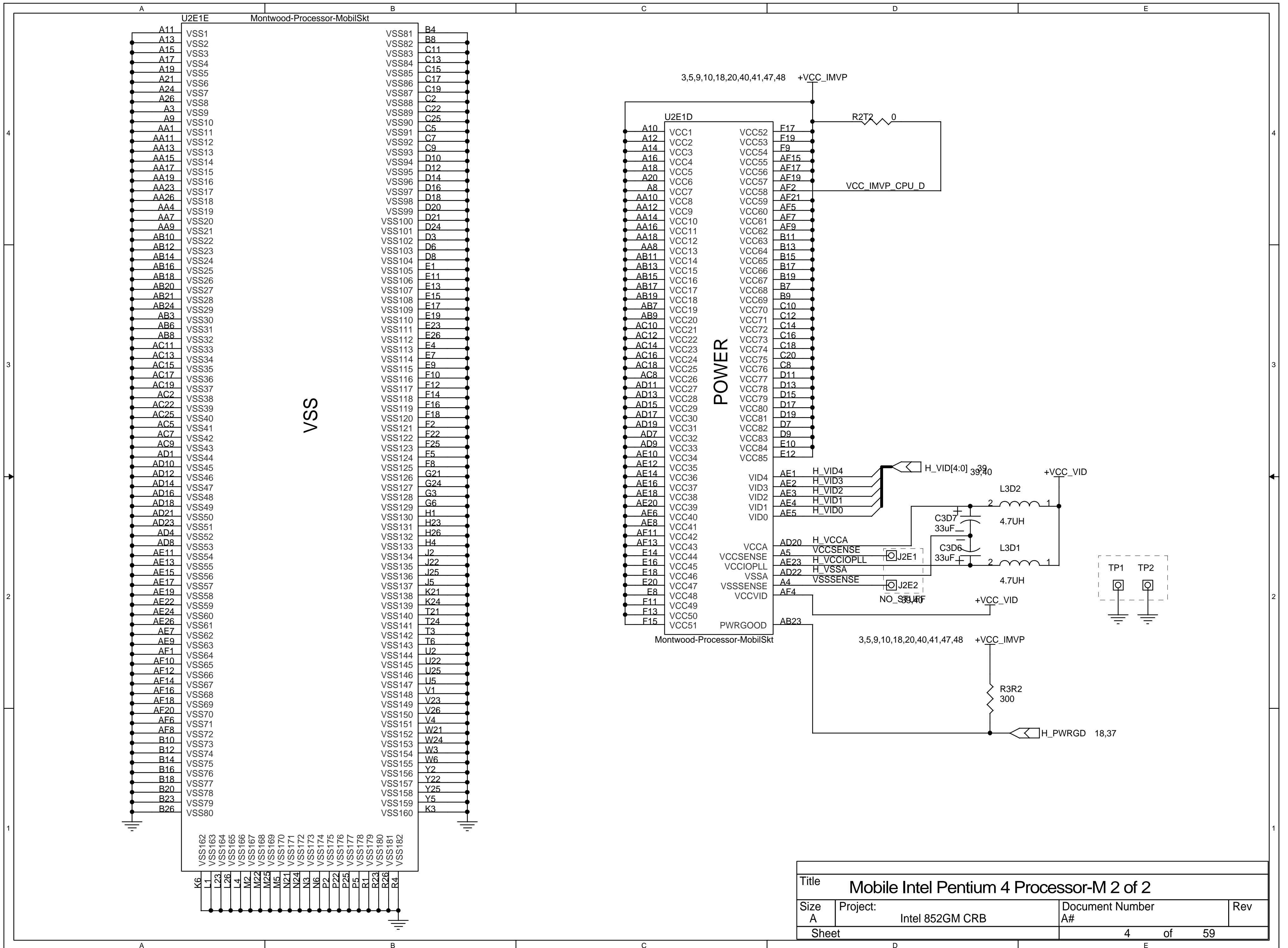
Place 1 GTLREF cap near each pin under processor.

U2E1B — ADDR GROUP 0 / ADDR GROUP 1 / CONTROL — Montwood-Processor-MobilSkt

U2E1A — DATA GRP 0 / DATA GRP 1 / DATA GRP 2 / DATA GRP 3 — Montwood-Processor-MobilSkt

U2E1C — HOST CLK / LEGACY CPU / THERM / REF & COMP / TAP/ITP — Montwood-Processor-MobilSkt

Title	Mobile Intel Pentium 4 Processor-M 1 of 2		
Size	Project: Intel 852GM CRB	Document Number A#	Rev
Sheet		3 of 59	



U2E1E
Montwood-Processor-MobilSkt
VSS
U2E1D
POWER
Montwood-Processor-MobilSkt
3,5,9,10,18,20,40,41,47,48
+VCC_IMVP
R2T2
0
VCC_IMVP_CPU_D
H_VID[4:0]
39,40
H_VID4
H_VID3
H_VID2
H_VID1
H_VID0
+VCC_VID
L3D2
4.7UH
C3D7
33uF
C3D6
33uF
L3D1
4.7UH
H_VCCA
VCCSENSE
H_VCCIOPLL
H_VSSA
VSSSENSE
J2E1
J2E2
NO_STUFF
TP1
TP2
R3R2
300
H_PWRGD
18,37
Title
Mobile Intel Pentium 4 Processor-M 2 of 2
Size
A
Project:
Intel 852GM CRB
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A#
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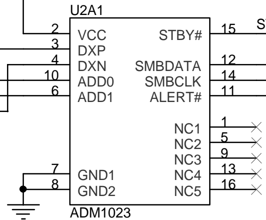
CPU Thermal Sensor

6,8,9,11,15,16,18,20,21,23,26,31,33..36,38..40,42,44,48   +V3.3S

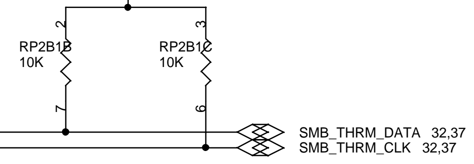
Address Select Straps
Current Address:
1001 110x



3 H_THERMDA

3 H_THERMDC

THRM_ALERT#

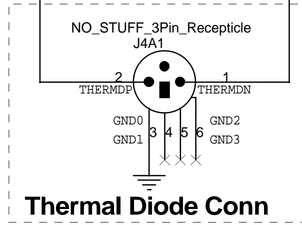


SMB_THRM_DATA 32,37
SMB_THRM_CLK 32,37

R2B2
NO_STUFF_0

PM_THRM# 19,21,32,37

Note: No Stuff for Normal Operation



Thermal Diode Conn

Layout Note:
Route H_THERMDA and H_THERMDC on same layer.
10 mil trace on 10 mil spacing.

Note:
If using Thermal Diode Conn, NO STUFF C2A1 and U2A1.

Place TDO pullup resistor within 2" of ITP.

Place TMS pullup resistor within 1" of ITP.

Place TDI pullup resistor within 2" of ITP.

Place RESET# serial resistor within 0.1" and RESET pullup resistor within 0.3".

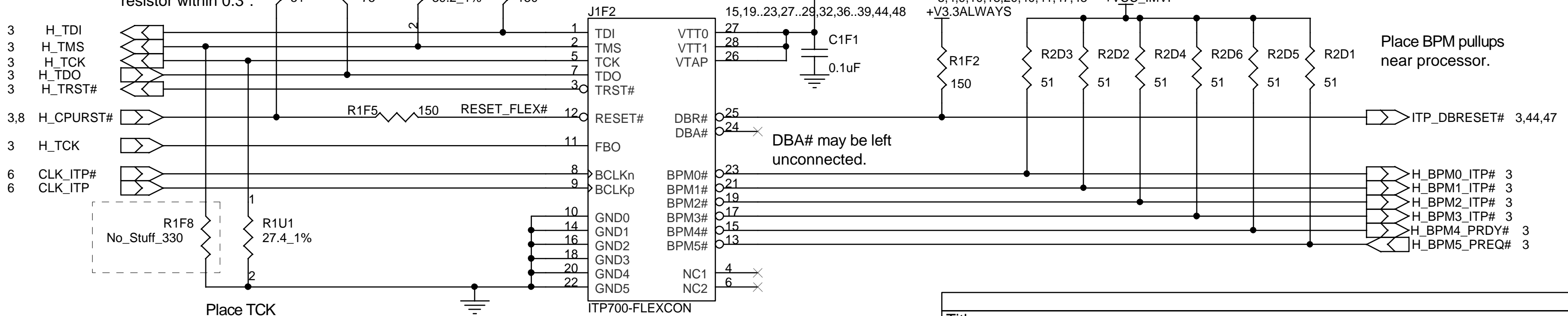
Place 0.1uF cap within 0.1" of VTT pins on ITP.

H_BPM[5:0]* signals should be matched to within 0.25" of each other and not longer than 6.0".

Place BPM pullups near processor.

Run separate H_TCK trace to processor for FBO and TCK pins on ITP.

The ITP should be at the end of the H_CPURST# transmission line but less than 6.0" from the processor.



Place TCK pulldown resistor within 1" of ITP.

Title	CPU Thermal Sensor & ITP		
Size A	Project: Intel 852GM CRB	Document Number A#	Rev
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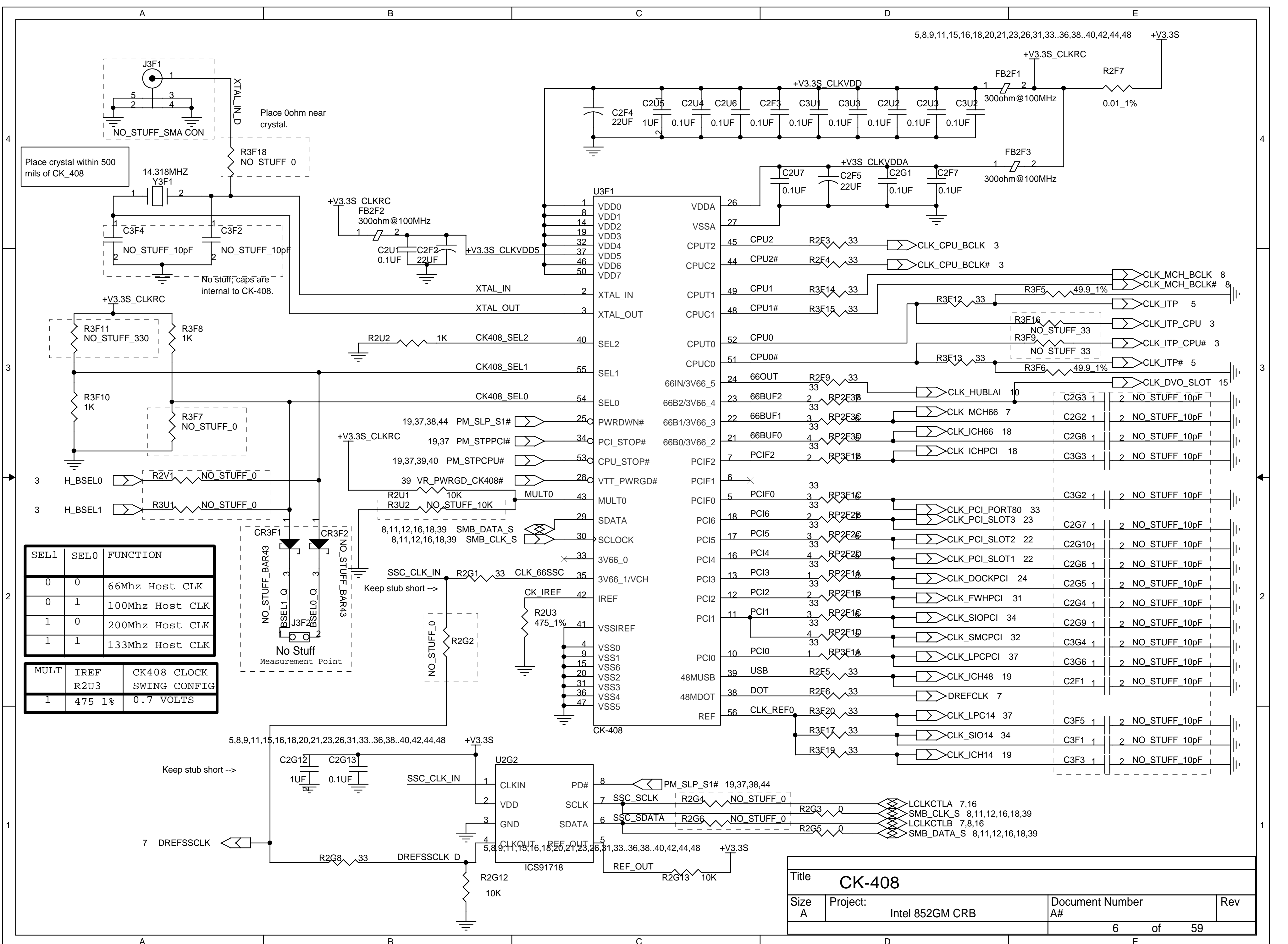
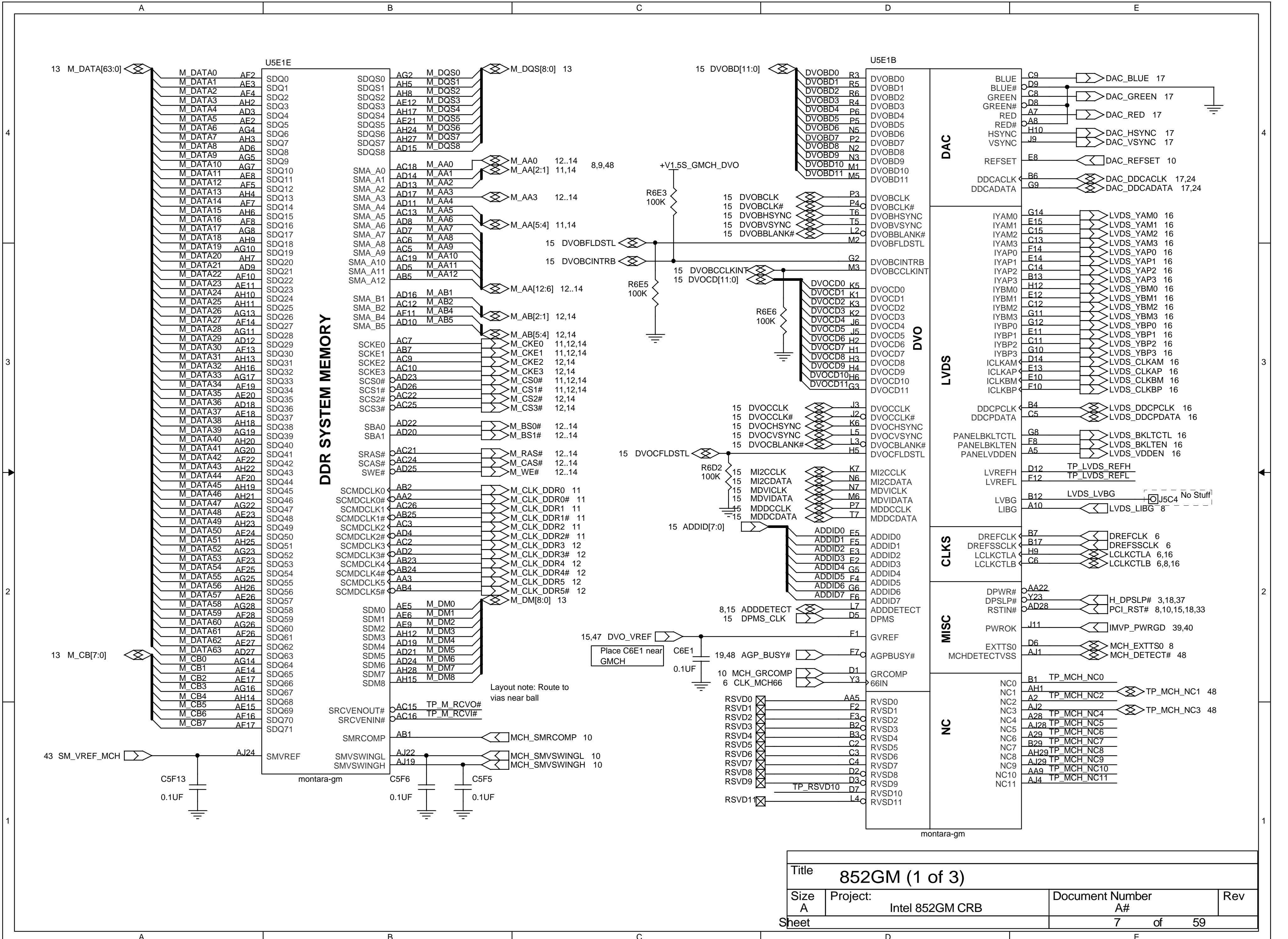


SEL1	SEL0	FUNCTION
0	0	66Mhz Host CLK
0	1	100Mhz Host CLK
1	0	200Mhz Host CLK
1	1	133Mhz Host CLK

MULT	IREF R2U3	CK408 CLOCK SWING CONFIG
1	475 1%	0.7 VOLTS

Title CK-408

Size A | Project: Intel 852GM CRB | Document Number A# | Rev



U5E1E
DDR SYSTEM MEMORY
13 M_DATA[63:0]
M_DQS[8:0] 13
13 M_CB[7:0]
43 SM_VREF_MCH
SMVREF
M_AA0 12..14
M_AA[2:1] 11,14
8,9,48
M_AA3 12..14
M_AA[5:4] 11,14
M_AA[12:6] 12..14
M_AB[2:1] 12,14
M_AB[5:4] 12,14
M_CKE0 11,12,14
M_CKE1 11,12,14
M_CKE2 12,14
M_CKE3 12,14
M_CS0# 11,12,14
M_CS1# 11,12,14
M_CS2# 12,14
M_CS3# 12,14
M_BS0# 12..14
M_BS1# 12..14
M_RAS# 12..14
M_CAS# 12..14
M_WE# 12..14
M_CLK_DDR0 11
M_CLK_DDR0# 11
M_CLK_DDR1 11
M_CLK_DDR1# 11
M_CLK_DDR2 11
M_CLK_DDR2# 11
M_CLK_DDR3 12
M_CLK_DDR3# 12
M_CLK_DDR4 12
M_CLK_DDR4# 12
M_CLK_DDR5 12
M_CLK_DDR5# 12
M_DM[8:0] 13
Layout note: Route to vias near ball
TP_M_RCVO#
TP_M_RCVI#
MCH_SMRCOMP 10
MCH_SMVSWINGL 10
MCH_SMVSWINGH 10
C5F13 0.1UF
C5F6 0.1UF
C5F5 0.1UF
montara-gm
U5E1B
15 DVOBD[11:0]
+V1.5S_GMCH_DVO
R6E3 100K
R6E5 100K
R6E6 100K
R6D2 100K
15 DVOBCLK
15 DVOBCLK#
15 DVOBHSYNC
15 DVOBVSYNC
15 DVOBBLANK#
15 DVOBFLDSTL
15 DVOBCINTRB
15 DVOBCCLKINT
15 DVOCD[11:0]
15 DVOCCLK
15 DVOCCLK#
15 DVOCHSYNC
15 DVOCVSYNC
15 DVOCBLANK#
15 DVOCFLDSTL
15 MI2CCLK
15 MI2CDATA
15 MDVICLK
15 MDVIDATA
15 MDDCCLK
15 MDDCDATA
15 ADDID[7:0]
8,15 ADDDETECT
15 DPMS_CLK
15,47 DVO_VREF
Place C6E1 near GMCH
C6E1 0.1UF
19,48 AGP_BUSY#
10 MCH_GRCOMP
6 CLK_MCH66
TP_RSVD10
DVO
DAC
LVDS
CLKS
MISC
NC
DAC_BLUE 17
DAC_GREEN 17
DAC_RED 17
DAC_HSYNC 17
DAC_VSYNC 17
DAC_REFSET 10
DAC_DDCACLK 17,24
DAC_DDCADATA 17,24
LVDS_YAM0 16
LVDS_YAM1 16
LVDS_YAM2 16
LVDS_YAM3 16
LVDS_YAP0 16
LVDS_YAP1 16
LVDS_YAP2 16
LVDS_YAP3 16
LVDS_YBM0 16
LVDS_YBM1 16
LVDS_YBM2 16
LVDS_YBM3 16
LVDS_YBP0 16
LVDS_YBP1 16
LVDS_YBP2 16
LVDS_YBP3 16
LVDS_CLKAM 16
LVDS_CLKAP 16
LVDS_CLKBM 16
LVDS_CLKBP 16
LVDS_DDCPCLK 16
LVDS_DDCPDATA 16
LVDS_BKLTCTL 16
LVDS_BKLTEN 16
LVDS_VDDEN 16
TP_LVDS_REFH
TP_LVDS_REFL
LVDS_LVBG
J5C4 No Stuff
LVDS_LIBG 8
DREFCLK 6
DREFSSCLK 6
LCLKCTLA 6,16
LCLKCTLB 6,8,16
H_DPSLP# 3,18,37
PCI_RST# 8,10,15,18,33
IMVP_PWRGD 39,40
MCH_EXTTS0 8
MCH_DETECT# 48
TP_MCH_NC0
TP_MCH_NC1 48
TP_MCH_NC2
TP_MCH_NC3 48
TP_MCH_NC4
TP_MCH_NC5
TP_MCH_NC6
TP_MCH_NC7
TP_MCH_NC8
TP_MCH_NC9
TP_MCH_NC10
TP_MCH_NC11
montara-gm
Title 852GM (1 of 3)
Size A
Project: Intel 852GM CRB
Document Number A#
Rev
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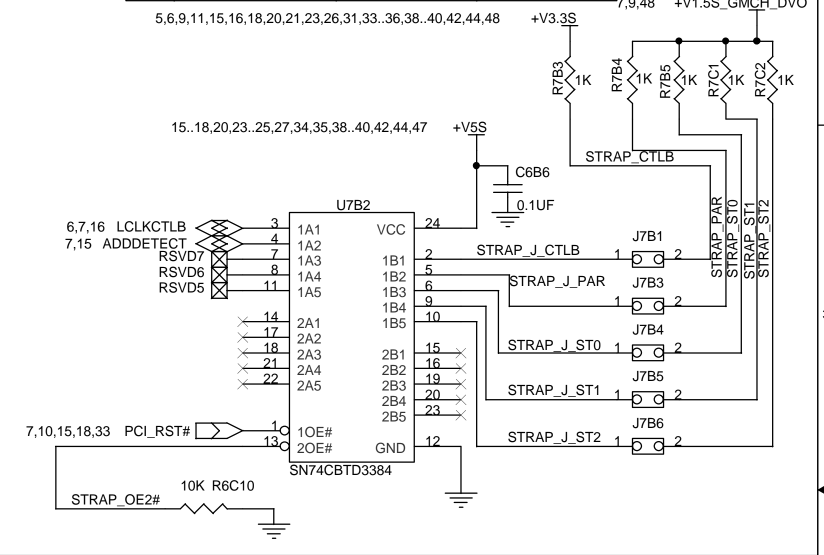
GMCH Strapping Options

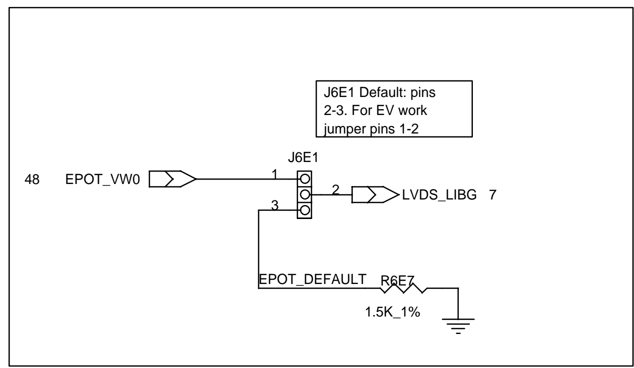
	Function	Board Default	Optional Override
J7B1	PSB Voltage Select	JMP for 1.2V	1.05V
J7B3	DVO Strap	No JMP for DVO	Reserved
J7B4	GST0	No JMP	
J7B5	GST1	No JMP	
J7B6	GST2	No JMP	



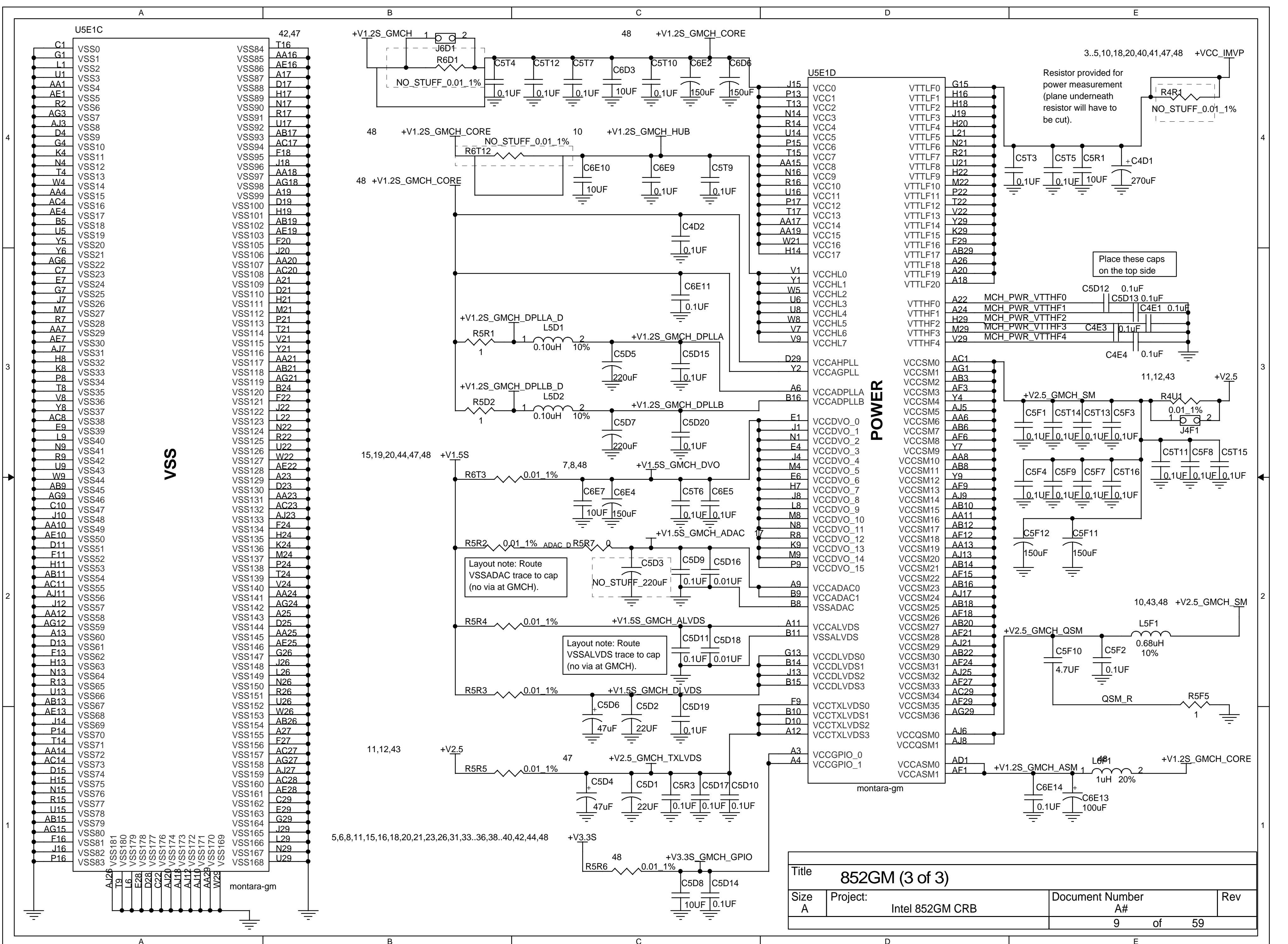
External Thermal Sensor Header

Note: Host Clock terminations are at the source (CK408)

Layout Note: Route MCH_HXSWING, MCH_HYSWING 10 mil trace, 20 mil space



Title	852GM (2 of 3)		
Size A	Project: Intel 852GM CRB	Document Number A#	Rev
Sheet	8 of 59		


U5E1C
VSS
montara-gm
U5E1D
POWER
montara-gm
Resistor provided for power measurement (plane underneath resistor will have to be cut).
Place these caps on the top side
Layout note: Route VSSADAC trace to cap (no via at GMCH).
Layout note: Route VSSALVDS trace to cap (no via at GMCH).
+V1.2S_GMCH
+V1.2S_GMCH_CORE
+VCC_IMVP
+V1.2S_GMCH_HUB
+V1.2S_GMCH_DPLLA_D
+V1.2S_GMCH_DPLLA
+V1.2S_GMCH_DPLLB_D
+V1.2S_GMCH_DPLLB
+V1.5S
+V1.5S_GMCH_DVO
+V1.5S_GMCH_ADAC
+V1.5S_GMCH_ALVDS
+V1.5S_GMCH_DLVDS
+V2.5
+V2.5_GMCH_TXLVDS
+V3.3S
+V3.3S_GMCH_GPIO
+V2.5_GMCH_SM
+V2.5_GMCH_QSM
+V1.2S_GMCH_ASM
QSM_R
MCH_PWR_VTTHF0
MCH_PWR_VTTHF1
MCH_PWR_VTTHF2
MCH_PWR_VTTHF3
MCH_PWR_VTTHF4
NO_STUFF_0.01_1%
NO_STUFF_220uF
Title
852GM (3 of 3)
Size
A
Project:
Intel 852GM CRB
Document Number
A#
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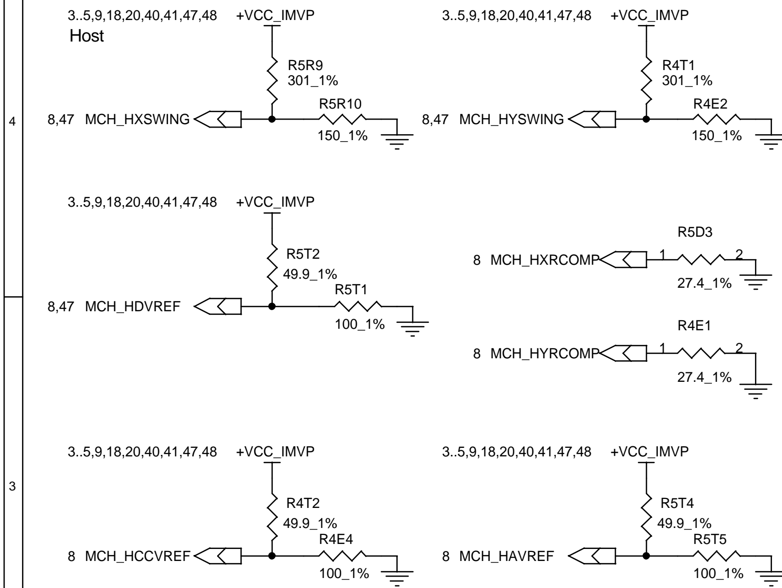
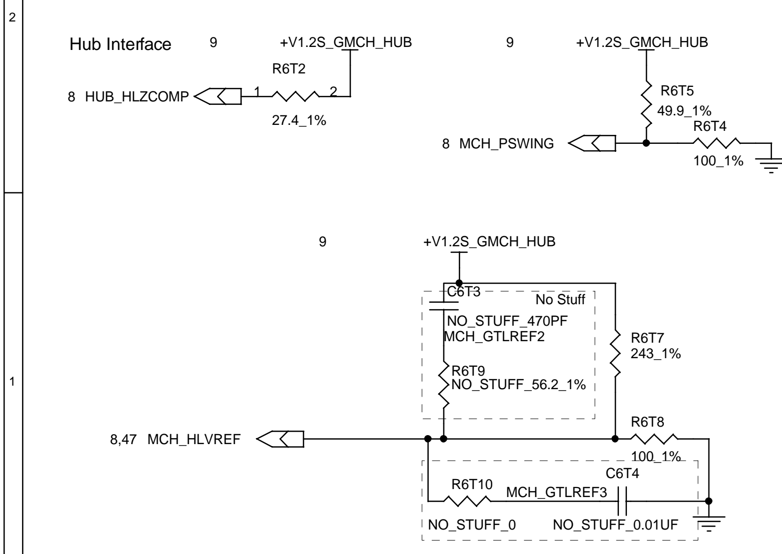
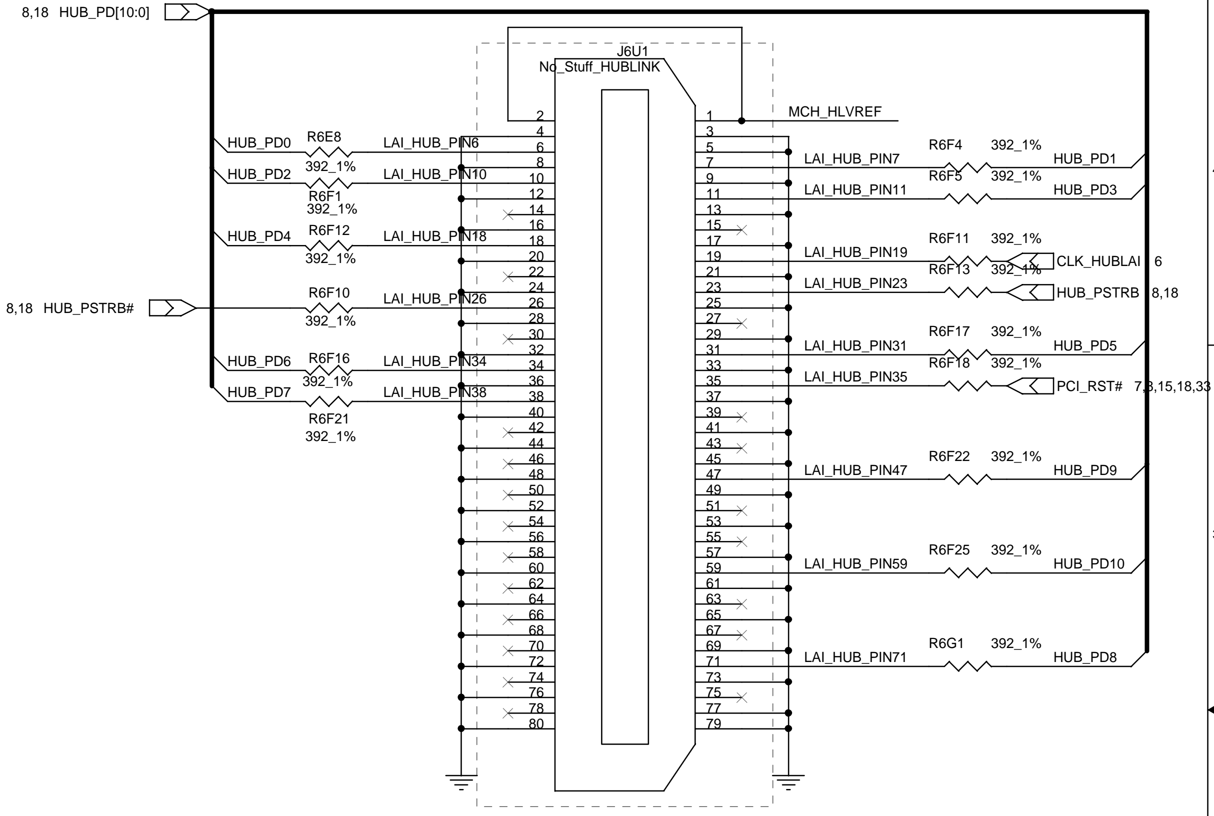
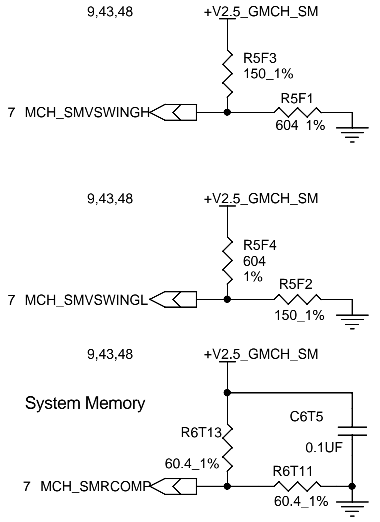
GMCH-GML Compensation & Reference Voltages



To support the Brookdale-G to Montara-G interposer, the following resistor need to be changed to these new values.
R5D3 = 24.9_1% R4E1 = 24.9_1%
R5R8 = 169_1% R6T2 = 68.1_1%







Layout Note:
The following signals should have 10 mil spacing and must be routed 20 mil from any other trace.

MCH_HXSWING
MCH_HYSWING
MCH_HDVREF
MCH_HXRCOMP
MCH_HYRCOMP
MCH_HCCVREF
MCH_HLVREF
MCH_SMVSWINGL
MCH_SMRCOMP
MCH_SMVSWINGH
HUB_HLZCOMP
MCH_PSWING
DAC_REFSET
MCH_GRCOMP
MCH_HAVREF

Title	852GM Circuitry		
Size A	Project: Intel 852GM CRB	Document Number A#	Rev
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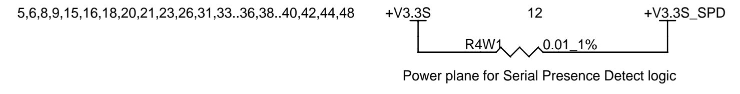
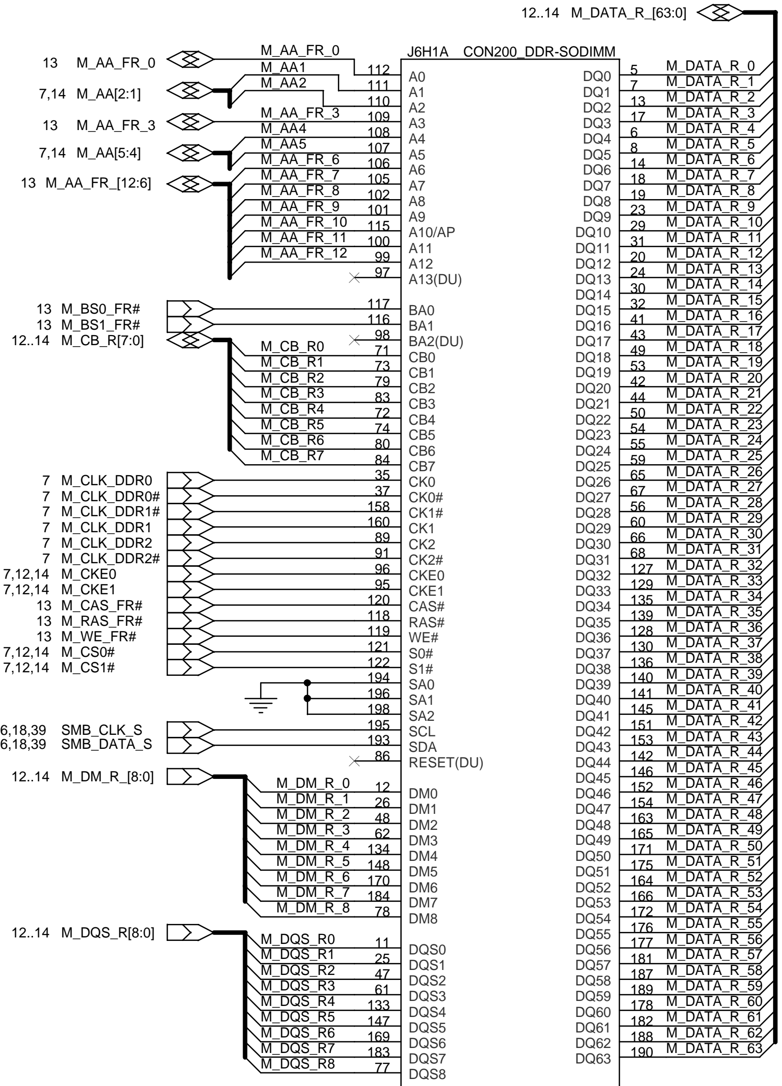
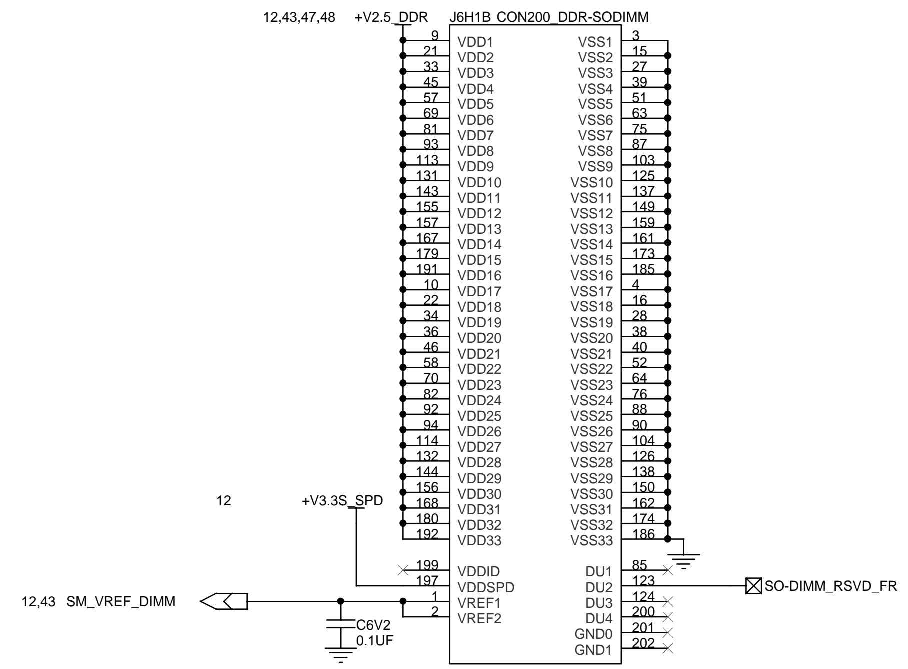
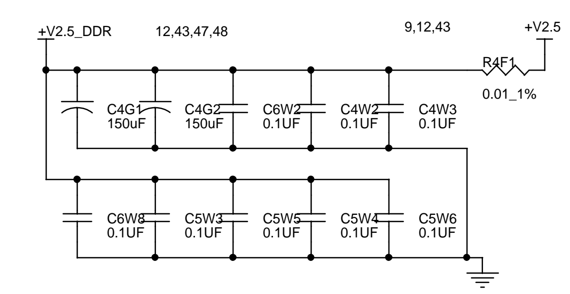




SO-DIMM 0





Layout note: Place capacitors between and near DDR connector if possible

Title	DDR SO-DIMMs (1 of 2)		
Size A	Project: Intel 852GM CRB	Document Number A#	Rev
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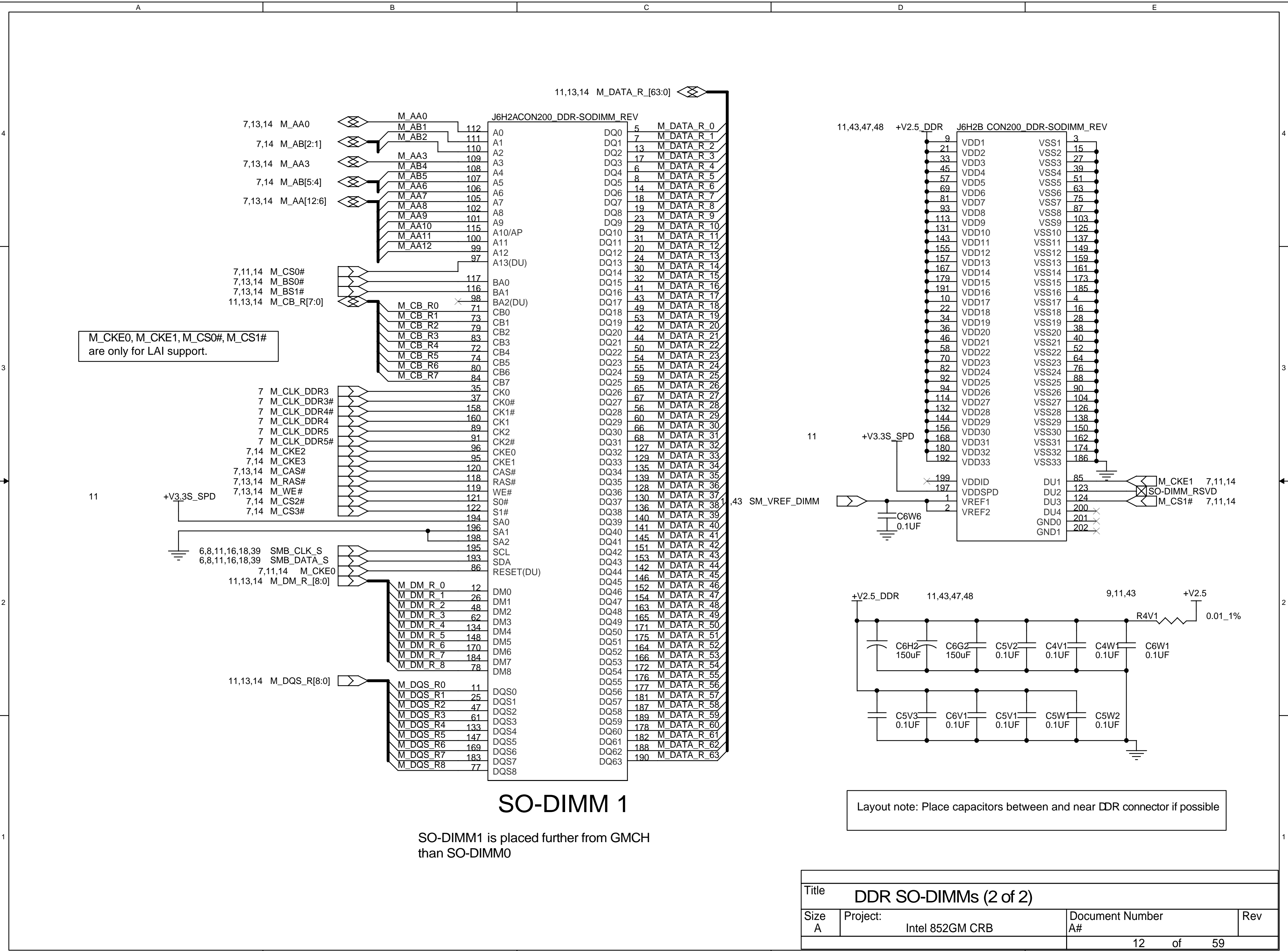

11,13,14 M_DATA_R_[63:0]
J6H2A CON200_DDR-SODIMM_REV
J6H2B CON200_DDR-SODIMM_REV
7,13,14 M_AA0
7,14 M_AB[2:1]
7,13,14 M_AA3
7,14 M_AB[5:4]
7,13,14 M_AA[12:6]
7,11,14 M_CS0#
7,13,14 M_BS0#
7,13,14 M_BS1#
11,13,14 M_CB_R[7:0]
M_CKE0, M_CKE1, M_CS0#, M_CS1#
are only for LAI support.
7 M_CLK_DDR3
7 M_CLK_DDR3#
7 M_CLK_DDR4#
7 M_CLK_DDR4
7 M_CLK_DDR5
7 M_CLK_DDR5#
7,14 M_CKE2
7,14 M_CKE3
7,13,14 M_CAS#
7,13,14 M_RAS#
7,13,14 M_WE#
7,14 M_CS2#
7,14 M_CS3#
11 +V3.3S_SPD
6,8,11,16,18,39 SMB_CLK_S
6,8,11,16,18,39 SMB_DATA_S
7,11,14 M_CKE0
11,13,14 M_DM_R_[8:0]
11,13,14 M_DQS_R[8:0]
11,43,47,48 +V2.5_DDR
11 +V3.3S_SPD
SM_VREF_DIMM
C6W6 0.1UF
M_CKE1 7,11,14
SO-DIMM_RSVD
M_CS1# 7,11,14
+V2.5_DDR 11,43,47,48
9,11,43 +V2.5
R4V1 0.01_1%
C6H2 150uF
C6G2 150uF
C5V2 0.1UF
C4V1 0.1UF
C4W1 0.1UF
C6W1 0.1UF
C5V3 0.1UF
C6V1 0.1UF
C5V1 0.1UF
C5W1 0.1UF
C5W2 0.1UF
SO-DIMM 1
SO-DIMM1 is placed further from GMCH
than SO-DIMM0
Layout note: Place capacitors between and near DDR connector if possible
Title DDR SO-DIMMs (2 of 2)
Size A
Project: Intel 852GM CRB
Document Number A#
Rev
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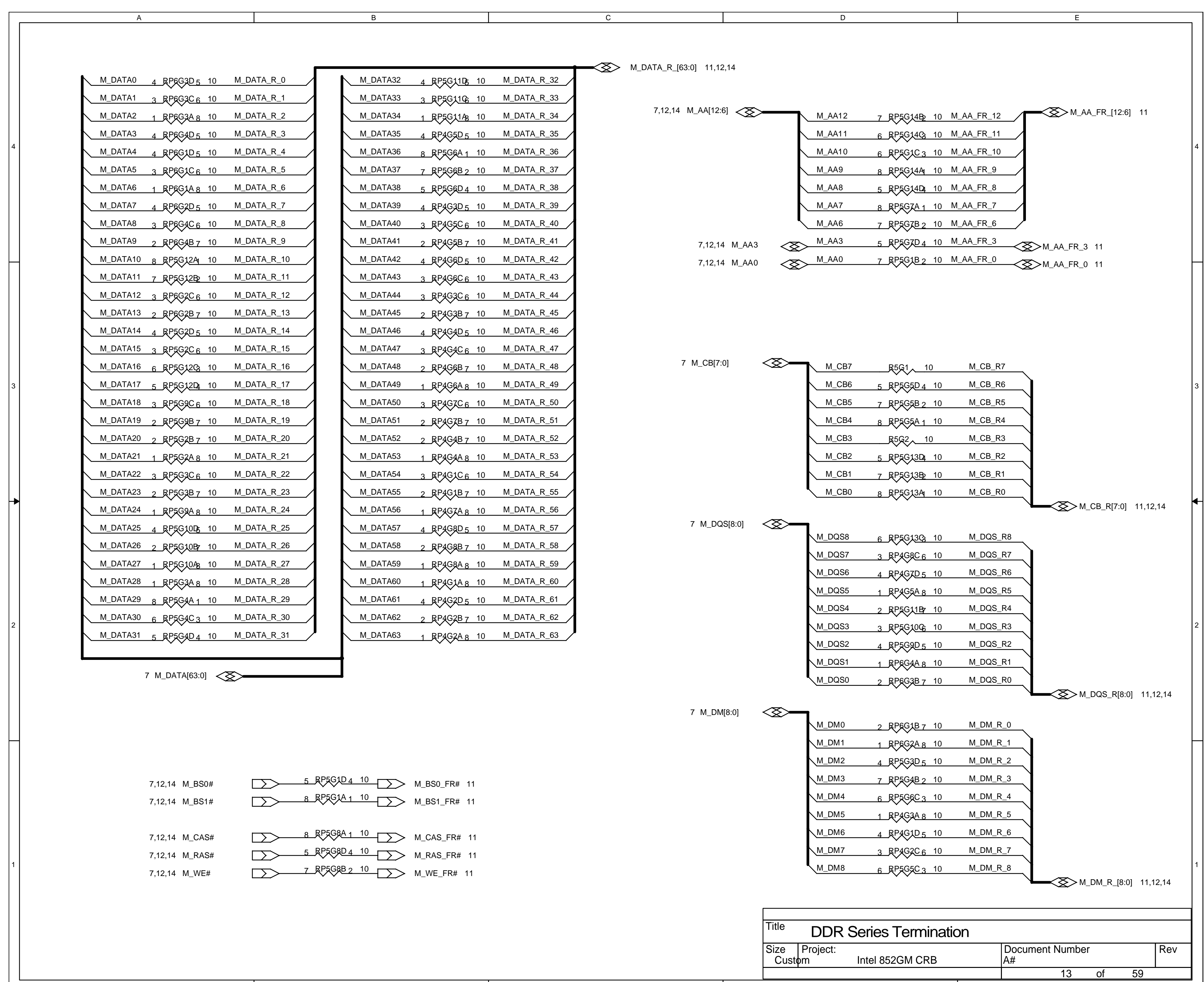

M_DATA_R_[63:0] 11,12,14
7 M_DATA[63:0]
M_DATA0 4 RP6G3D 5 10 M_DATA_R_0
M_DATA1 3 RP6G3C 6 10 M_DATA_R_1
M_DATA2 1 RP6G3A 8 10 M_DATA_R_2
M_DATA3 4 RP6G4D 5 10 M_DATA_R_3
M_DATA4 4 RP6G1D 5 10 M_DATA_R_4
M_DATA5 3 RP6G1C 6 10 M_DATA_R_5
M_DATA6 1 RP6G1A 8 10 M_DATA_R_6
M_DATA7 4 RP6G2D 5 10 M_DATA_R_7
M_DATA8 3 RP6G4C 6 10 M_DATA_R_8
M_DATA9 2 RP6G4B 7 10 M_DATA_R_9
M_DATA10 8 RP5G12A 1 10 M_DATA_R_10
M_DATA11 7 RP5G12B 2 10 M_DATA_R_11
M_DATA12 3 RP6G2C 6 10 M_DATA_R_12
M_DATA13 2 RP6G2B 7 10 M_DATA_R_13
M_DATA14 4 RP5G2D 5 10 M_DATA_R_14
M_DATA15 3 RP5G2C 6 10 M_DATA_R_15
M_DATA16 6 RP5G12C 3 10 M_DATA_R_16
M_DATA17 5 RP5G12D 4 10 M_DATA_R_17
M_DATA18 3 RP5G9C 6 10 M_DATA_R_18
M_DATA19 2 RP5G9B 7 10 M_DATA_R_19
M_DATA20 2 RP5G2B 7 10 M_DATA_R_20
M_DATA21 1 RP5G2A 8 10 M_DATA_R_21
M_DATA22 3 RP5G3C 6 10 M_DATA_R_22
M_DATA23 2 RP5G3B 7 10 M_DATA_R_23
M_DATA24 1 RP5G9A 8 10 M_DATA_R_24
M_DATA25 4 RP5G10D 5 10 M_DATA_R_25
M_DATA26 2 RP5G10B 7 10 M_DATA_R_26
M_DATA27 1 RP5G10A 8 10 M_DATA_R_27
M_DATA28 1 RP5G3A 8 10 M_DATA_R_28
M_DATA29 8 RP5G4A 1 10 M_DATA_R_29
M_DATA30 6 RP5G4C 3 10 M_DATA_R_30
M_DATA31 5 RP5G4D 4 10 M_DATA_R_31
M_DATA32 4 RP5G11D 5 10 M_DATA_R_32
M_DATA33 3 RP5G11C 6 10 M_DATA_R_33
M_DATA34 1 RP5G11A 8 10 M_DATA_R_34
M_DATA35 4 RP4G5D 5 10 M_DATA_R_35
M_DATA36 8 RP5G6A 1 10 M_DATA_R_36
M_DATA37 7 RP5G6B 2 10 M_DATA_R_37
M_DATA38 5 RP5G6D 4 10 M_DATA_R_38
M_DATA39 4 RP4G3D 5 10 M_DATA_R_39
M_DATA40 3 RP4G5C 6 10 M_DATA_R_40
M_DATA41 2 RP4G5B 7 10 M_DATA_R_41
M_DATA42 4 RP4G6D 5 10 M_DATA_R_42
M_DATA43 3 RP4G6C 6 10 M_DATA_R_43
M_DATA44 3 RP4G3C 6 10 M_DATA_R_44
M_DATA45 2 RP4G3B 7 10 M_DATA_R_45
M_DATA46 4 RP4G4D 5 10 M_DATA_R_46
M_DATA47 3 RP4G4C 6 10 M_DATA_R_47
M_DATA48 2 RP4G6B 7 10 M_DATA_R_48
M_DATA49 1 RP4G6A 8 10 M_DATA_R_49
M_DATA50 3 RP4G7C 6 10 M_DATA_R_50
M_DATA51 2 RP4G7B 7 10 M_DATA_R_51
M_DATA52 2 RP4G4B 7 10 M_DATA_R_52
M_DATA53 1 RP4G4A 8 10 M_DATA_R_53
M_DATA54 3 RP4G1C 6 10 M_DATA_R_54
M_DATA55 2 RP4G1B 7 10 M_DATA_R_55
M_DATA56 1 RP4G7A 8 10 M_DATA_R_56
M_DATA57 4 RP4G8D 5 10 M_DATA_R_57
M_DATA58 2 RP4G8B 7 10 M_DATA_R_58
M_DATA59 1 RP4G8A 8 10 M_DATA_R_59
M_DATA60 1 RP4G1A 8 10 M_DATA_R_60
M_DATA61 4 RP4G2D 5 10 M_DATA_R_61
M_DATA62 2 RP4G2B 7 10 M_DATA_R_62
M_DATA63 1 RP4G2A 8 10 M_DATA_R_63
7,12,14 M_AA[12:6]
M_AA_FR_[12:6] 11
M_AA12 7 RP5G14B 2 10 M_AA_FR_12
M_AA11 6 RP5G14C 3 10 M_AA_FR_11
M_AA10 6 RP5G1C 3 10 M_AA_FR_10
M_AA9 8 RP5G14A 1 10 M_AA_FR_9
M_AA8 5 RP5G14D 4 10 M_AA_FR_8
M_AA7 8 RP5G7A 1 10 M_AA_FR_7
M_AA6 7 RP5G7B 2 10 M_AA_FR_6
7,12,14 M_AA3
M_AA3 5 RP5G7D 4 10 M_AA_FR_3
M_AA_FR_3 11
7,12,14 M_AA0
M_AA0 7 RP5G1B 2 10 M_AA_FR_0
M_AA_FR_0 11
7 M_CB[7:0]
M_CB7 R5G1 10 M_CB_R7
M_CB6 5 RP5G5D 4 10 M_CB_R6
M_CB5 7 RP5G5B 2 10 M_CB_R5
M_CB4 8 RP5G5A 1 10 M_CB_R4
M_CB3 R5G2 10 M_CB_R3
M_CB2 5 RP5G13D 4 10 M_CB_R2
M_CB1 7 RP5G13B 2 10 M_CB_R1
M_CB0 8 RP5G13A 1 10 M_CB_R0
M_CB_R[7:0] 11,12,14
7 M_DQS[8:0]
M_DQS8 6 RP5G13C 3 10 M_DQS_R8
M_DQS7 3 RP4G8C 6 10 M_DQS_R7
M_DQS6 4 RP4G7D 5 10 M_DQS_R6
M_DQS5 1 RP4G5A 8 10 M_DQS_R5
M_DQS4 2 RP5G11B 7 10 M_DQS_R4
M_DQS3 3 RP5G10C 6 10 M_DQS_R3
M_DQS2 4 RP5G9D 5 10 M_DQS_R2
M_DQS1 1 RP6G4A 8 10 M_DQS_R1
M_DQS0 2 RP6G3B 7 10 M_DQS_R0
M_DQS_R[8:0] 11,12,14
7 M_DM[8:0]
M_DM0 2 RP6G1B 7 10 M_DM_R_0
M_DM1 1 RP6G2A 8 10 M_DM_R_1
M_DM2 4 RP5G3D 5 10 M_DM_R_2
M_DM3 7 RP5G4B 2 10 M_DM_R_3
M_DM4 6 RP5G6C 3 10 M_DM_R_4
M_DM5 1 RP4G3A 8 10 M_DM_R_5
M_DM6 4 RP4G1D 5 10 M_DM_R_6
M_DM7 3 RP4G2C 6 10 M_DM_R_7
M_DM8 6 RP5G5C 3 10 M_DM_R_8
M_DM_R_[8:0] 11,12,14
7,12,14 M_BS0# 5 RP5G1D 4 10 M_BS0_FR# 11
7,12,14 M_BS1# 8 RP5G1A 1 10 M_BS1_FR# 11
7,12,14 M_CAS# 8 RP5G8A 1 10 M_CAS_FR# 11
7,12,14 M_RAS# 5 RP5G8D 4 10 M_RAS_FR# 11
7,12,14 M_WE# 7 RP5G8B 2 10 M_WE_FR# 11
Title DDR Series Termination
Size Custom
Project: Intel 852GM CRB
Document Number A#
Rev
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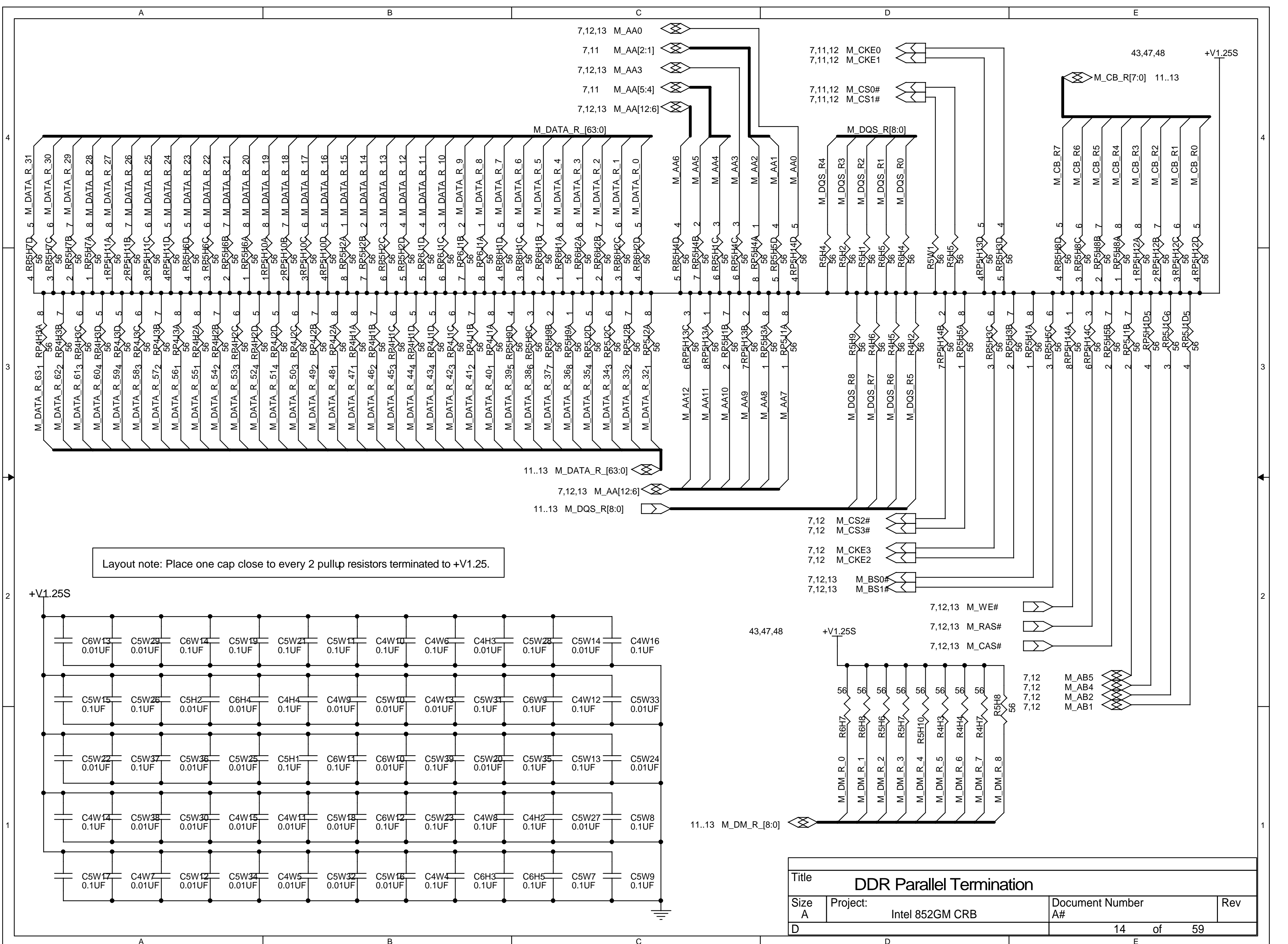

7,12,13 M_AA0
7,11 M_AA[2:1]
7,12,13 M_AA3
7,11 M_AA[5:4]
7,12,13 M_AA[12:6]
7,11,12 M_CKE0
7,11,12 M_CKE1
7,11,12 M_CS0#
7,11,12 M_CS1#
43,47,48
+V1.25S
M_CB_R[7:0] 11..13
M_DATA_R_[63:0]
M_DQS_R[8:0]
11..13 M_DATA_R_[63:0]
7,12,13 M_AA[12:6]
11..13 M_DQS_R[8:0]
7,12 M_CS2#
7,12 M_CS3#
7,12 M_CKE3
7,12 M_CKE2
7,12,13 M_BS0#
7,12,13 M_BS1#
7,12,13 M_WE#
7,12,13 M_RAS#
7,12,13 M_CAS#
7,12 M_AB5
7,12 M_AB4
7,12 M_AB2
7,12 M_AB1
11..13 M_DM_R_[8:0]
Layout note: Place one cap close to every 2 pullup resistors terminated to +V1.25.
+V1.25S
C6W13 0.01UF
C5W29 0.01UF
C6W14 0.1UF
C5W19 0.1UF
C5W21 0.1UF
C5W11 0.1UF
C4W10 0.1UF
C4W6 0.1UF
C4H3 0.01UF
C5W28 0.1UF
C5W14 0.01UF
C4W16 0.1UF
C5W15 0.1UF
C5W26 0.1UF
C5H2 0.01UF
C6H4 0.01UF
C4H4 0.1UF
C4W9 0.01UF
C5W10 0.01UF
C4W13 0.01UF
C5W31 0.1UF
C6W9 0.1UF
C4W12 0.1UF
C5W33 0.01UF
C5W22 0.01UF
C5W37 0.1UF
C5W36 0.01UF
C5W25 0.01UF
C5H1 0.1UF
C6W11 0.1UF
C6W10 0.01UF
C5W39 0.1UF
C5W20 0.01UF
C5W35 0.1UF
C5W13 0.1UF
C5W24 0.01UF
C4W14 0.1UF
C5W38 0.01UF
C5W30 0.01UF
C4W15 0.01UF
C4W11 0.01UF
C5W18 0.01UF
C6W12 0.1UF
C5W23 0.1UF
C4W8 0.1UF
C4H2 0.1UF
C5W27 0.01UF
C5W8 0.1UF
C5W17 0.1UF
C4W7 0.01UF
C5W12 0.01UF
C5W34 0.01UF
C4W5 0.01UF
C5W32 0.01UF
C5W16 0.01UF
C4W4 0.1UF
C6H3 0.1UF
C6H5 0.1UF
C5W7 0.1UF
C5W9 0.1UF
Title
DDR Parallel Termination
Size A
Project: Intel 852GM CRB
Document Number A#
Rev
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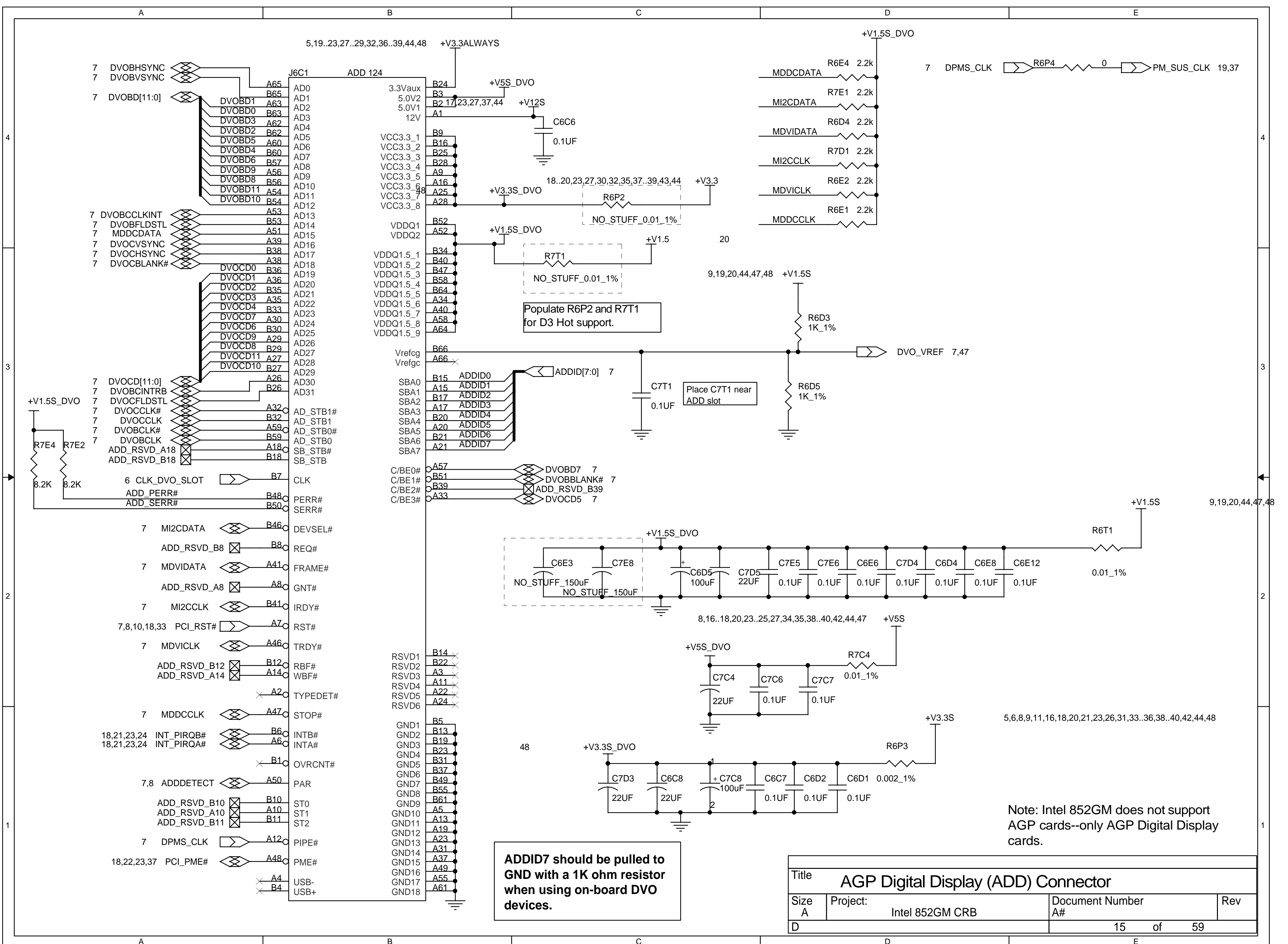

5,19..23,27..29,32,36..39,44,48 +V3.3ALWAYS
J6C1 ADD 124
DVOBHSYNC
DVOBVSYNC
DVOBD[11:0]
DVOBCCLKINT
DVOBFLDSTL
MDDCDATA
DVOCVSYNC
DVOCHSYNC
DVOCBLANK#
DVOCD[11:0]
DVOBCINTRB
DVOCFLDSTL
DVOCCLK#
DVOCCLK
DVOBCLK#
DVOBCLK
ADD_RSVD_A18
ADD_RSVD_B18
CLK_DVO_SLOT
ADD_PERR#
ADD_SERR#
+V1.5S_DVO
R7E4
R7E2
8.2K
8.2K
MI2CDATA
ADD_RSVD_B8
MDVIDATA
ADD_RSVD_A8
MI2CCLK
7,8,10,18,33 PCI_RST#
MDVICLK
ADD_RSVD_B12
ADD_RSVD_A14
MDDCCLK
18,21,23,24 INT_PIRQB#
18,21,23,24 INT_PIRQA#
7,8 ADDDETECT
ADD_RSVD_B10
ADD_RSVD_A10
ADD_RSVD_B11
DPMS_CLK
18,22,23,37 PCI_PME#
3.3Vaux
5.0V2
5.0V1
12V
+V5S_DVO
+V12S
C6C6
0.1UF
17,23,27,37,44
+V3.3S_DVO
18..20,23,27,30,32,35,37..39,43,44
+V3.3
R6P2
NO_STUFF_0.01_1%
+V1.5S_DVO
+V1.5
20
R7T1
NO_STUFF_0.01_1%
Populate R6P2 and R7T1 for D3 Hot support.
9,19,20,44,47,48 +V1.5S
R6D3 1K_1%
DVO_VREF 7,47
C7T1 0.1UF
Place C7T1 near ADD slot
R6D5 1K_1%
ADDID[7:0] 7
DVOBD7 7
DVOBBLANK# 7
ADD_RSVD_B39
DVOCD5 7
+V1.5S_DVO
MDDCDATA R6E4 2.2k
MI2CDATA R7E1 2.2k
MDVIDATA R6D4 2.2k
MI2CCLK R7D1 2.2k
MDVICLK R6E2 2.2k
MDDCCLK R6E1 2.2k
7 DPMS_CLK R6P4 0 PM_SUS_CLK 19,37
+V1.5S 9,19,20,44,47,48
R6T1 0.01_1%
C6E3 C7E8 NO_STUFF_150uF NO_STUFF_150uF
C6D5 100uF
C7D5 22UF
C7E5 C7E6 C6E6 C7D4 C6D4 C6E8 C6E12 0.1UF
8,16..18,20,23..25,27,34,35,38..40,42,44,47 +V5S
+V5S_DVO
R7C4 0.01_1%
C7C4 22UF
C7C6 0.1UF
C7C7 0.1UF
+V3.3S
5,6,8,9,11,16,18,20,21,23,26,31,33..36,38..40,42,44,48
48
+V3.3S_DVO
R6P3 0.002_1%
C7D3 22UF
C6C8 22UF
C7C8 100uF
C6C7 0.1UF
C6D2 0.1UF
C6D1 0.1UF
ADDID7 should be pulled to GND with a 1K ohm resistor when using on-board DVO devices.
Note: Intel 852GM does not support AGP cards--only AGP Digital Display cards.
Title AGP Digital Display (ADD) Connector
Size A
Project: Intel 852GM CRB
Document Number A#
Rev
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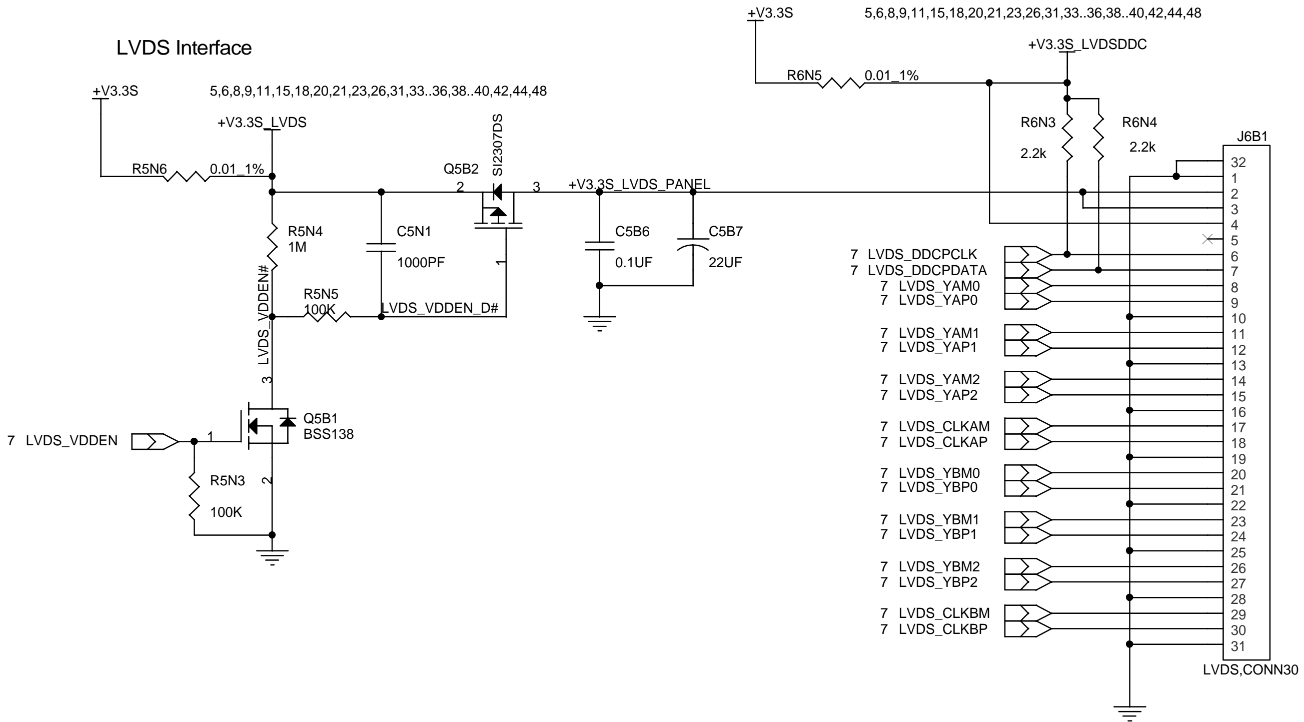
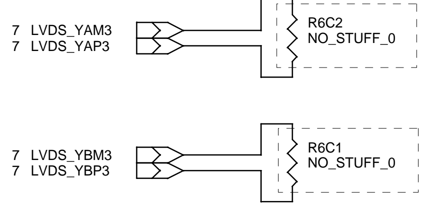
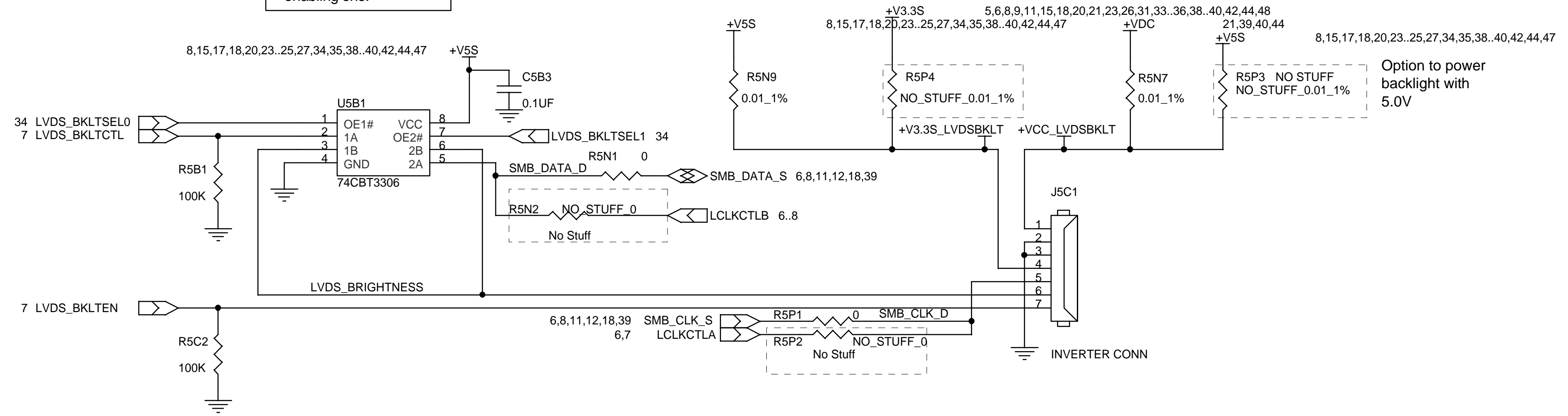
LVDS Interface





BIOS Note: Disable both BKLTSEL lines before enabling one.

LVDS Panel Backlight



Title	LVDS		
Size A	Project: Intel 852GM CRB	Document Number A#	Rev
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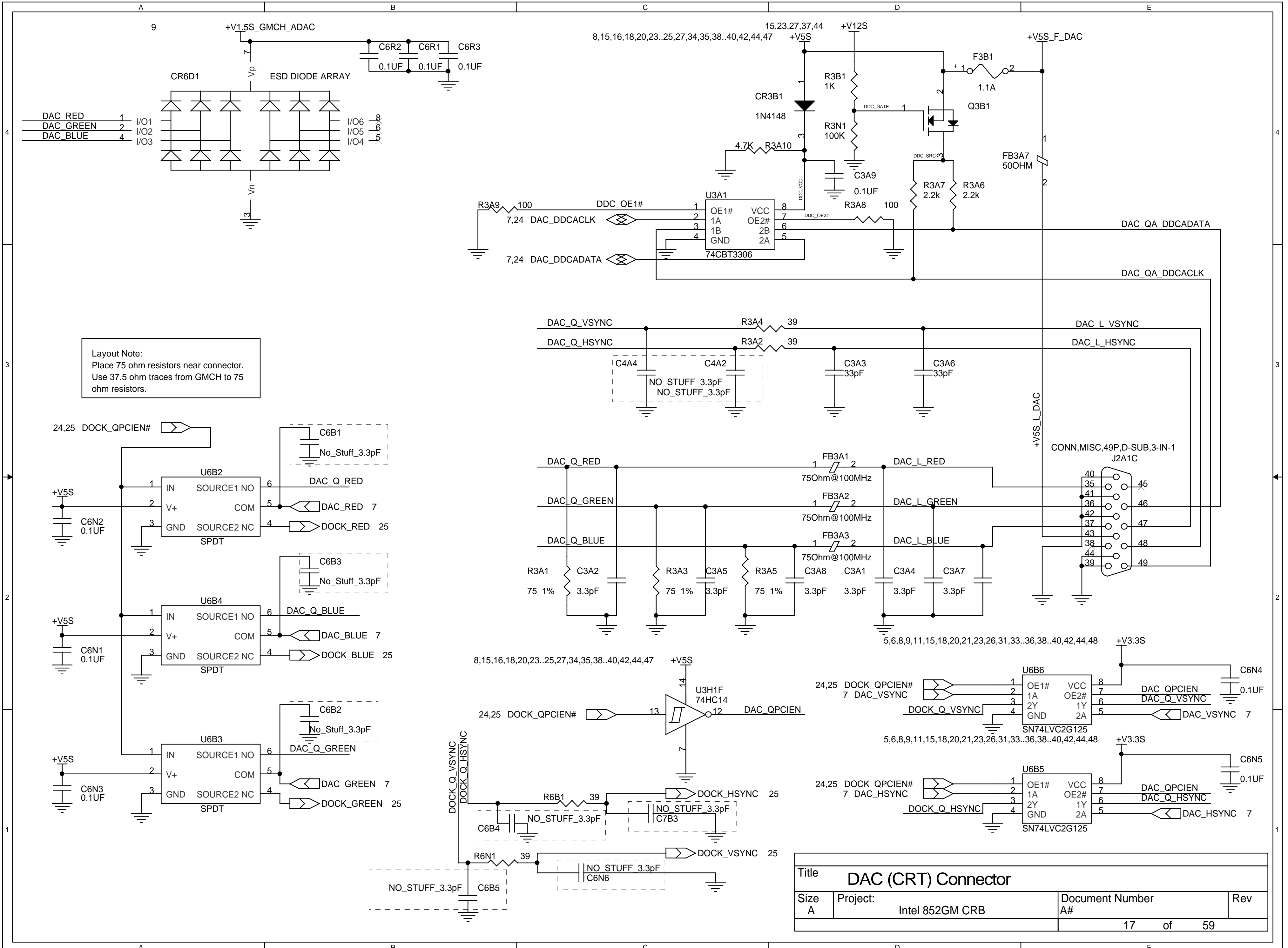
DAC (CRT) Connector
Project: Intel 852GM CRB
Size A
Document Number A#
Rev
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+V1.5S_GMCH_ADAC
CR6D1
ESD DIODE ARRAY
C6R2 C6R1 C6R3
0.1UF 0.1UF 0.1UF
DAC_RED
DAC_GREEN
DAC_BLUE
I/O1 I/O2 I/O3 I/O4 I/O5 I/O6
Vp Vn
+V5S
+V12S
+V5S_F_DAC
15,23,27,37,44
8,15,16,18,20,23..25,27,34,35,38..40,42,44,47
CR3B1 1N4148
R3B1 1K
R3N1 100K
DDC_GATE
Q3B1
F3B1 1.1A
FB3A7 50OHM
R3A10 4.7K
C3A9 0.1UF
R3A7 2.2k
R3A6 2.2k
DDC_SRC
DDC_VCC
U3A1
74CBT3306
OE1# 1A 1B GND VCC OE2# 2B 2A
R3A9 100
DDC_OE1#
R3A8 100
DDC_OE2#
7,24 DAC_DDCACLK
7,24 DAC_DDCADATA
DAC_QA_DDCADATA
DAC_QA_DDCACLK
Layout Note:
Place 75 ohm resistors near connector.
Use 37.5 ohm traces from GMCH to 75 ohm resistors.
DAC_Q_VSYNC
DAC_Q_HSYNC
R3A4 39
R3A2 39
DAC_L_VSYNC
DAC_L_HSYNC
C4A4 C4A2
NO_STUFF_3.3pF
C3A3 33pF
C3A6 33pF
+V5S_L_DAC
CONN,MISC,49P,D-SUB,3-IN-1
J2A1C
24,25 DOCK_QPCIEN#
U6B2 U6B4 U6B3
IN SOURCE1 NO V+ COM GND SOURCE2 NC
SPDT
C6B1 C6B2 C6B3 No_Stuff_3.3pF
DAC_Q_RED DAC_RED 7 DOCK_RED 25
DAC_Q_BLUE DAC_BLUE 7 DOCK_BLUE 25
DAC_Q_GREEN DAC_GREEN 7 DOCK_GREEN 25
C6N2 0.1UF
C6N1 0.1UF
C6N3 0.1UF
FB3A1 FB3A2 FB3A3 75Ohm@100MHz
DAC_L_RED DAC_L_GREEN DAC_L_BLUE
R3A1 75_1% C3A2 3.3pF
R3A3 75_1% C3A5 3.3pF
R3A5 75_1% C3A8 3.3pF
C3A1 3.3pF C3A4 3.3pF C3A7 3.3pF
U3H1F 74HC14
DAC_QPCIEN
5,6,8,9,11,15,18,20,21,23,26,31,33..36,38..40,42,44,48
+V3.3S
U6B6 U6B5
SN74LVC2G125
OE1# 1A 2Y GND VCC OE2# 1Y 2A
C6N4 0.1UF
C6N5 0.1UF
7 DAC_VSYNC
7 DAC_HSYNC
DOCK_Q_VSYNC
DOCK_Q_HSYNC
DAC_Q_VSYNC
DAC_Q_HSYNC
DAC_VSYNC 7
DAC_HSYNC 7
R6B1 39
R6N1 39
DOCK_HSYNC 25
DOCK_VSYNC 25
C6B4 C7B3 C6N6 C6B5 NO_STUFF_3.3pF

ICH4-M

PART A

U7G2A

HUB INTERFACE VSWING VOLTAGE

HUB INTERFACE LAYOUT:
Route signals with 4/8 trace/space routing. Signals must match +/- 0.1" of HUB_STB/STB# signals

The pad of R6H10 needs to be overlap with R6H12

PLACE RCOMP resistor within 0.5" of ICH pad using a thick trace

RCOMP R should be 2/3 board impedance

EEPROM for ICH4-M LAN (Atmel AT93C66-10PC-2.7)

This Bus Switch prevents leakage of the SMBus into devices powered on the switched rail.

Buffer to reduce loading on PCI_RST#

PCI_AD[31:0], PCI_C/BE0#..PCI_C/BE3#, PCI_GNT0#..PCI_GNT4#, PCI_REQ0#..PCI_REQ4#, CLK_ICHPCI, PCI_DEVSEL#, PCI_FRAME#, PCI_REQA#, PCI_REQB#, PCI_GNTA#, PCI_GNTB#, PCI_IRDY#, PCI_PAR, PCI_PERR#, PCI_LOCK#, PCI_PME#, PCI_RST#, PCI_SERR#, PCI_STOP#, PCI_TRDY#

SM_INTRUDER#, SMLINK0, SMLINK1, SMB_CLK, SMB_DATA, SMB_ALERT#/GPIO11

CPU_A20GATE, CPU_A20M#, CPU_DPSLP#, CPU_FERR#, CPU_IGNNE#, CPU_INIT#, CPU_INTR, CPU_NMI, CPU_PWRGOOD, CPU_RCIN#, CPU_SLP#, CPU_SMI#, CPU_STPCLK#

HUB_PD0..HUB_PD11, HUB_CLK, HUB_PSTRB#, HUB_PSTRB, HUB_RCOMP, HUB_VREF, HUB_VSWING

INT_APICCLK, INT_APICD0, INT_APICD1, INT_PIRQA#..INT_PIRQD#, INT_PIRQE#/GPIO2..INT_PIRQH#/GPIO5, INT_IRQ14, INT_IRQ15, INT_SERIRQ

EEP_CS, EEP_DIN, EEP_DOUT, EEP_SHCLK

LAN_RXD0..LAN_RXD2, LAN_TXD0..LAN_TXD2, LAN_JCLK, LAN_RSTSYNC, LAN_RST#

U7G1 AT88SC153; U6G1 74CBT3306; U8G1 74AHC1G08; CR8G2A/CR8G2B 3904

Title	ICH4-M (1 of 3)		
Size A	Project: Intel 852GM CRB	Document Number A#	Rev
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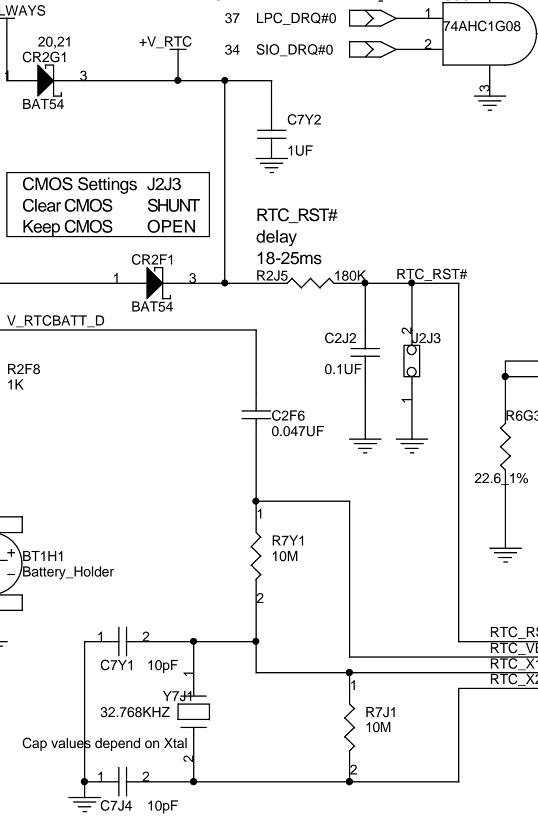
ICH4M Strapping Options

	Function	Board Default	Optional Override
R6V2	No Reboot	NO STUFF	STUFF for No Reboot
R7V7	Safe Mode Boot	NO STUFF	STUFF for safe mode
R7V8	A16 swap override	NO STUFF	STUFF for A16 swap override
R7V9	Reserved	NO STUFF	STUFF

RTC Circuitry



ICH4-M

PART B

U7G2B

CRB/SV Detect
Default: 2-3 for CRB

Layout: Route
USB_RBIAS/RBIAS#
Differentially

NO_STUFF_MFG-TEST-JUMPER

Title	ICH4-M (2 of 3)		
Size A	Project: Intel 852GM CRB	Document Number A#	Rev
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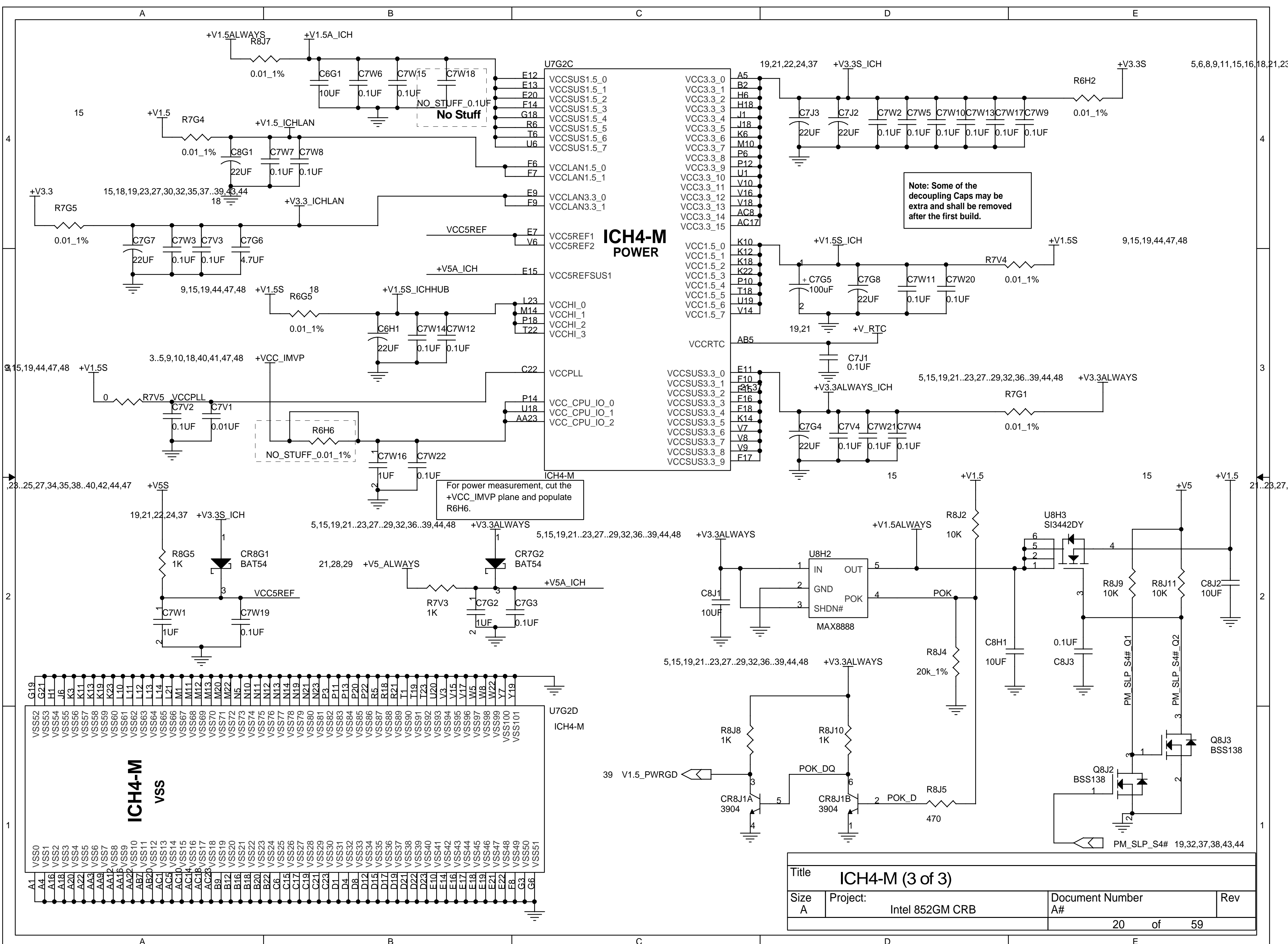

A
B
C
D
E
4
3
2
1
+V1.5ALWAYS
R8J7
0.01_1%
+V1.5A_ICH
C6G1
10UF
C7W6
0.1UF
C7W15
0.1UF
C7W18
NO_STUFF_0.1UF
No Stuff
U7G2C
E12
E13
E20
F14
G18
R6
T6
U6
VCCSUS1.5_0
VCCSUS1.5_1
VCCSUS1.5_2
VCCSUS1.5_3
VCCSUS1.5_4
VCCSUS1.5_5
VCCSUS1.5_6
VCCSUS1.5_7
15
+V1.5
R7G4
0.01_1%
+V1.5_ICHLAN
C8G1
22UF
C7W7
0.1UF
C7W8
0.1UF
F6
F7
VCCLAN1.5_0
VCCLAN1.5_1
+V3.3
15,18,19,23,27,30,32,35,37..39,43,44
18
+V3.3_ICHLAN
R7G5
0.01_1%
C7G7
22UF
C7W3
0.1UF
C7V3
0.1UF
C7G6
4.7UF
E9
F9
VCCLAN3.3_0
VCCLAN3.3_1
VCC5REF
E7
V6
VCC5REF1
VCC5REF2
+V5A_ICH
E15
VCC5REFSUS1
ICH4-M
POWER
9,15,19,44,47,48
+V1.5S
18
R6G5
0.01_1%
+V1.5S_ICHHUB
C6H1
22UF
C7W14
0.1UF
C7W12
0.1UF
L23
M14
P18
T22
VCCHI_0
VCCHI_1
VCCHI_2
VCCHI_3
3..5,9,10,18,40,41,47,48
+VCC_IMVP
C22
VCCPLL
+V1.5S
0
R7V5
VCCPLL
C7V2
0.1UF
C7V1
0.01UF
P14
U18
AA23
VCC_CPU_IO_0
VCC_CPU_IO_1
VCC_CPU_IO_2
R6H6
NO_STUFF_0.01_1%
C7W16
1UF
C7W22
0.1UF
ICH4-M
For power measurement, cut the +VCC_IMVP plane and populate R6H6.
19,21,22,24,37
+V3.3S_ICH
A5
B2
H6
H18
J1
J18
K6
M10
P6
P12
U1
V10
V16
V18
AC8
AC17
VCC3.3_0
VCC3.3_1
VCC3.3_2
VCC3.3_3
VCC3.3_4
VCC3.3_5
VCC3.3_6
VCC3.3_7
VCC3.3_8
VCC3.3_9
VCC3.3_10
VCC3.3_11
VCC3.3_12
VCC3.3_13
VCC3.3_14
VCC3.3_15
+V3.3S
5,6,8,9,11,15,16,18,21,23
R6H2
0.01_1%
C7J3
22UF
C7J2
22UF
C7W2
0.1UF
C7W5
0.1UF
C7W10
0.1UF
C7W13
0.1UF
C7W17
0.1UF
C7W9
0.1UF
Note: Some of the decoupling Caps may be extra and shall be removed after the first build.
K10
K12
K18
K22
P10
T18
U19
V14
VCC1.5_0
VCC1.5_1
VCC1.5_2
VCC1.5_3
VCC1.5_4
VCC1.5_5
VCC1.5_6
VCC1.5_7
+V1.5S_ICH
+V1.5S
9,15,19,44,47,48
R7V4
0.01_1%
C7G5
100uF
C7G8
22UF
C7W11
0.1UF
C7W20
0.1UF
19,21
+V_RTC
AB5
VCCRTC
C7J1
0.1UF
E11
F10
F15
F16
F18
K14
V7
V8
V9
F17
VCCSUS3.3_0
VCCSUS3.3_1
VCCSUS3.3_2
VCCSUS3.3_3
VCCSUS3.3_4
VCCSUS3.3_5
VCCSUS3.3_6
VCCSUS3.3_7
VCCSUS3.3_8
VCCSUS3.3_9
+V3.3ALWAYS_ICH
5,15,19,21..23,27..29,32,36..39,44,48
+V3.3ALWAYS
R7G1
0.01_1%
C7G4
22UF
C7V4
0.1UF
C7W21
0.1UF
C7W4
0.1UF
,23..25,27,34,35,38..40,42,44,47
+V5S
19,21,22,24,37
+V3.3S_ICH
R8G5
1K
CR8G1
BAT54
VCC5REF
C7W1
1UF
C7W19
0.1UF
5,15,19,21..23,27..29,32,36..39,44,48
+V3.3ALWAYS
21,28,29
+V5_ALWAYS
R7V3
1K
CR7G2
BAT54
+V5A_ICH
C7G2
1UF
C7G3
0.1UF
15
+V1.5
R8J2
10K
U8H3
SI3442DY
15
+V5
+V1.5
21..23,27,
5,15,19,21..23,27..29,32,36..39,44,48
+V3.3ALWAYS
+V1.5ALWAYS
U8H2
IN
OUT
GND
POK
SHDN#
MAX8888
C8J1
10UF
POK
R8J4
20k_1%
C8H1
10UF
0.1UF
C8J3
R8J9
10K
R8J11
10K
C8J2
10UF
PM_SLP_S4#_Q1
PM_SLP_S4#_Q2
Q8J3
BSS138
Q8J2
BSS138
5,15,19,21..23,27..29,32,36..39,44,48
+V3.3ALWAYS
R8J8
1K
R8J10
1K
39
V1.5_PWRGD
POK_DQ
CR8J1A
3904
CR8J1B
3904
POK_D
R8J5
470
PM_SLP_S4#
19,32,37,38,43,44
U7G2D
ICH4-M
ICH4-M
VSS
Title
ICH4-M (3 of 3)
Size
A
Project:
Intel 852GM CRB
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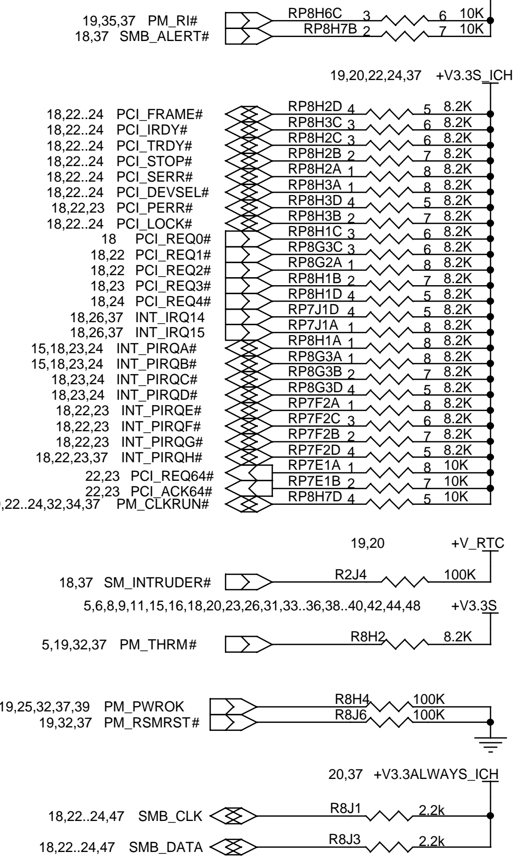
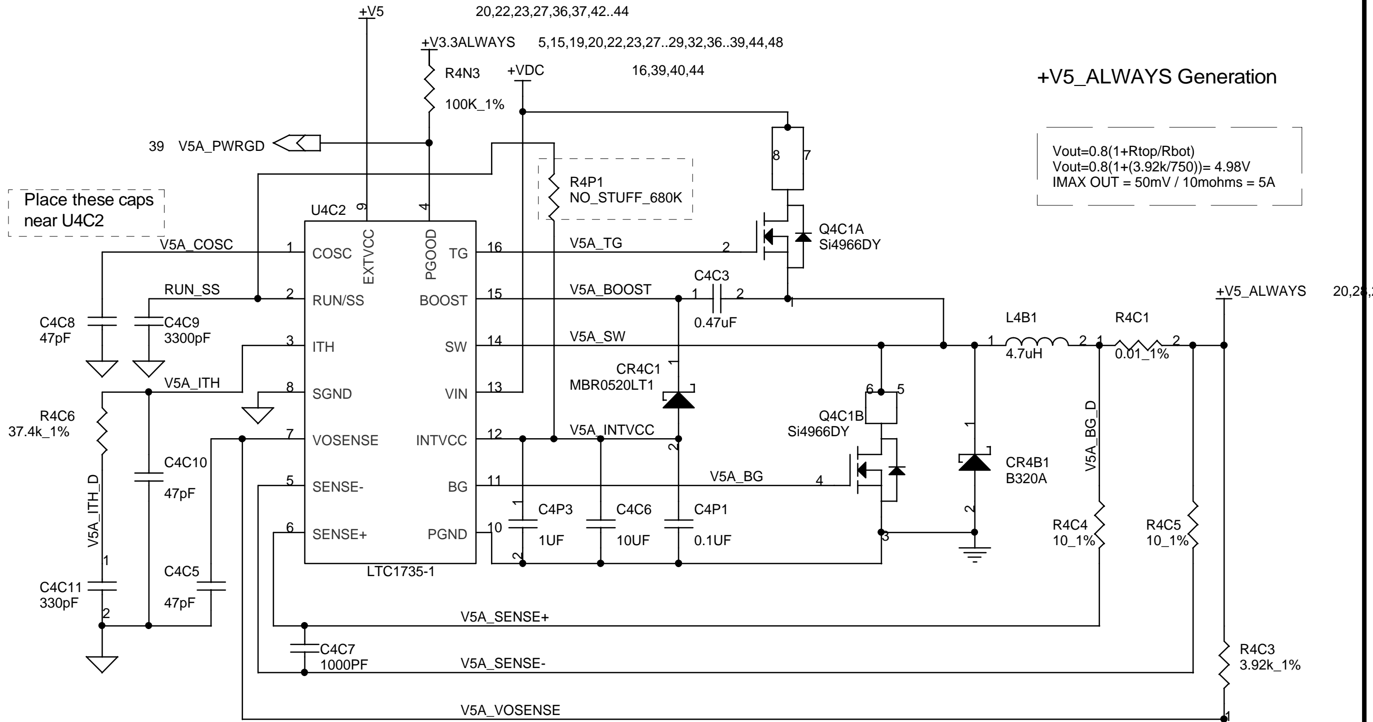
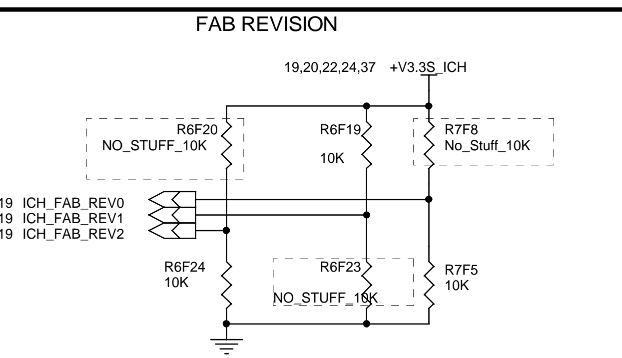
ICH4 Pullups



+V5_ALWAYS Generation

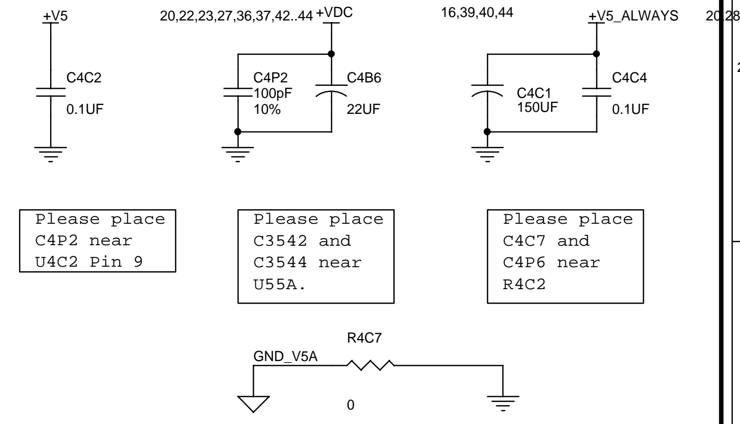


FAB REVISION



FAB ID Strapping Table

ICH_FAB_REV 2	1	0	BOARD FAB
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8



Title	ICH4-M Pullups and Testpoints		
Size A	Project: Intel 852GM CRB	Document Number A#	Rev
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PCI Slot 1 & 2

SLOT1 (J7B2, CON120_PCI)

Power rails: -V12S (23,44); +V12S_PCI (23); +V5S_PCI (23); +V3.3ALWAYS (5,15,19..21,23,27..29,32,36..39,44,48); +V3.3S_PCI (23); +V5_PCI (23)

Pin	Signal	Pin	Signal
B1	-12V	A1	TRST#
B2	TCK	A2	+12V
B3	GND1	A3	TMS
B4	TDO	A4	TDI
B5	+5V (1)	A5	+5V (7)
B6	+5V (2)	A6	INTA#
B7	INTB#	A7	INTC#
B8	INTD#	A8	+5V (8)
B9	PRSNT1#	A9	RSV3
B10	RSV1	A10	+5V (9)
B11	PRSNT2#	A11	RSV4
B12	GND2	A12	GND14
B13	GND3	A13	GND15
B14	RSV2	A14	RSV5
B15	GND4	A15	RST#
B16	CLK	A16	+5V (10)
B17	GND5	A17	GNT#
B18	REQ#	A18	GND16
B19	+5V (3)	A19	PME#
B20	AD31	A20	AD30
B21	AD29	A21	+3.3V (7)
B22	GND6	A22	AD28
B23	AD27	A23	AD26
B24	AD25	A24	GND17
B25	+3.3V (1)	A25	AD24
B26	C/BE3#	A26	IDSEL
B27	AD23	A27	+3.3V (8)
B28	GND8	A28	AD22
B29	AD21	A29	AD20
B30	AD19	A30	GND18
B31	+3.3V (2)	A31	AD18
B32	AD17	A32	AD16
B33	C/BE2#	A33	+3.3V (9)
B34	GND9	A34	FRAME#
B35	IRDY#	A35	GND19
B36	+3.3V (3)	A36	TRDY#
B37	DEVSEL#	A37	GND20
B38	GND10	A38	STOP#
B39	LOCK#	A39	+3.3V (10)
B40	PERR#	A40	SDONE
B41	+3.3V (4)	A41	SBO#
B42	SERR#	A42	GND21
B43	+3.3V (5)	A43	PAR
B44	C/BE1#	A44	AD15
B45	AD14	A45	+3.3V (11)
B46	GND11	A46	AD13
B47	AD12	A47	AD11
B48	AD10	A48	GND22
B49	GND12	A49	AD09
KEY		KEY	
B52	AD08	A52	C/BE0#
B53	AD07	A53	+3.3V (12)
B54	+3.3V (6)	A54	AD06
B55	AD05	A55	AD04
B56	AD03	A56	GND23
B57	GND13	A57	AD02
B58	AD01	A58	AD00
B59	+5V (4)	A59	+5V (11)
B60	ACK64#	A60	REQ64#
B61	+5V (5)	A61	+5V (12)
B62	+5V (6)	A62	+5V (13)

Slot 1 B-side nets: 18,21,23 INT_PIRQG#; 18,21,23 INT_PIRQE#; C7B10 0.01UF SLT1_PRSNT1#; C7C1 0.01UF SLT1_PRSNT2#; 18,23,24,32,34,37 INT_SERIRQ; 6 CLK_PCI_SLOT1; 18,21 PCI_REQ1#; 18,23,24 PCI_AD31; 18,23,24 PCI_AD29; 18,23,24 PCI_AD27; 18,23,24 PCI_AD25; 18,23,24 PCI_C/BE3#; 18,23,24 PCI_AD23; 18,23,24 PCI_AD21; 18,23,24 PCI_AD19; 18,23,24 PCI_AD17; 18,23,24 PCI_C/BE2#; 18,21,23,24 PCI_IRDY#; 18,21,23,24 PCI_DEVSEL#; 18,21,23,24 PCI_LOCK#; 18,21,23 PCI_PERR#; 18,21,23,24 PCI_SERR#; 18,23,24 PCI_C/BE1#; 18,23,24 PCI_AD14; 18,23,24 PCI_AD12; 18,23,24 PCI_AD10; 18,23,24 PCI_AD8; 18,23,24 PCI_AD7; 18,23,24 PCI_AD5; 18,23,24 PCI_AD3; 18,23,24 PCI_AD1; 21,23 PCI_ACK64#

Slot 1 A-side nets: INT_PIRQF# 18,21,23; INT_PIRQH# 18,21,23,37; PM_CLKRUN# 19,21,23,24,32,34,37; PCI_GATED_RST# 23,32,37; BUF_PCI_RST# 18,23,24,26,31,32,34,37; PCI_GNT1# 18; PCI_PME# 15,18,23,37; PCI_AD30 18,23,24; PCI_AD28 18,23,24; PCI_AD26 18,23,24; PCI_AD24 18,23,24; SLT1_IDSEL — R7C5 680 — PCI_AD16 18,23,24; PCI_AD22 18,23,24; PCI_AD20 18,23,24; PCI_AD18 18,23,24; PCI_AD16 18,23,24; PCI_FRAME# 18,21,23,24; PCI_TRDY# 18,21,23,24; PCI_STOP# 18,21,23,24; SMB_CLK 18,21,23,24,47; SMB_DATA 18,21,23,24,47; PCI_PAR 18,23,24; PCI_AD15 18,23,24; PCI_AD13 18,23,24; PCI_AD11 18,23,24; PCI_AD9 18,23,24; PCI_C/BE0# 18,23,24; PCI_AD6 18,23,24; PCI_AD4 18,23,24; PCI_AD2 18,23,24; PCI_AD0 18,23,24; PCI_REQ64# 21,23

SLOT2 (J8B3, CON120_PCI)

Power rails: -V12S (23,44); +V12S_PCI (23); +V5_PCI (23); +V5S_PCI (23); +V3.3ALWAYS (5,15,19..21,23,27..29,32,36..39,44,48); +V3.3S_PCI (23)

Pin assignments identical to Slot 1.

Slot 2 B-side nets: 18,21,23 INT_PIRQF#; 18,21,23,37 INT_PIRQH#; C8N1 SLT2_PRSNT1#; 0.01UF C8C1 SLT2_PRSNT2# 0.01UF; 18,23,24,32,34,37 INT_SERIRQ; 6 CLK_PCI_SLOT2; 18,21 PCI_REQ2#; 18,23,24 PCI_AD31; 18,23,24 PCI_AD29; 18,23,24 PCI_AD27; 18,23,24 PCI_AD25; 18,23,24 PCI_C/BE3#; 18,23,24 PCI_AD23; 18,23,24 PCI_AD21; 18,23,24 PCI_AD19; 18,23,24 PCI_AD17; 18,23,24 PCI_C/BE2#; 18,21,23,24 PCI_IRDY#; 18,21,23,24 PCI_DEVSEL#; 18,21,23,24 PCI_LOCK#; 18,21,23 PCI_PERR#; 18,21,23,24 PCI_SERR#; 18,23,24 PCI_C/BE1#; 18,23,24 PCI_AD14; 18,23,24 PCI_AD12; 18,23,24 PCI_AD10; 18,23,24 PCI_AD8; 18,23,24 PCI_AD7; 18,23,24 PCI_AD5; 18,23,24 PCI_AD3; 18,23,24 PCI_AD1; 21,23 PCI_ACK64#

Slot 2 A-side nets: INT_PIRQG# 18,21,23; INT_PIRQE# 18,21,23; PM_CLKRUN# 19,21,23,24,32,34,37; PCI_GATED_RST# 23,32,37; BUF_PCI_RST# 18,23,24,26,31,32,34,37; PCI_GNT2# 18; PCI_PME# 15,18,23,37; PCI_AD30 18,23,24; PCI_AD28 18,23,24; PCI_AD26 18,23,24; PCI_AD24 18,23,24; SLT2_IDSEL — R8C1 680 — PCI_AD17 18,23,24; PCI_AD22 18,23,24; PCI_AD20 18,23,24; PCI_AD18 18,23,24; PCI_AD16 18,23,24; PCI_FRAME# 18,21,23,24; PCI_TRDY# 18,21,23,24; PCI_STOP# 18,21,23,24; SMB_CLK 18,21,23,24,47; SMB_DATA 18,21,23,24,47; PCI_PAR 18,23,24; PCI_AD15 18,23,24; PCI_AD13 18,23,24; PCI_AD11 18,23,24; PCI_AD9 18,23,24; PCI_C/BE0# 18,23,24; PCI_AD6 18,23,24; PCI_AD4 18,23,24; PCI_AD2 18,23,24; PCI_AD0 18,23,24; PCI_REQ64# 21,23

Legacy header

18,19,23 PCI_GNTA# — J7G1 (5Pin_Keyed-HDR), pins 1–6

19..21,24,37 +V3.3S_ICH — R7V2 8.2K

PCI_REQA# 18,23

INT_SERIRQ 18,23,24,32,34,37

R7V1 8.2K — 19..21,24,37 +V3.3S_ICH

LEGACY HEADER
FOR ADD-IN
AUDIO CARD
TESTING
VIA SLOT1 ONLY

20,21,23,27,36,37,42..44 +V5 — R8N1 NO_STUFF_0 — 23 +V5_PCI

Title	PCI Slot 1 & 2		
Size: A	Project: Intel 852GM CRB	Document Number: A#	Rev
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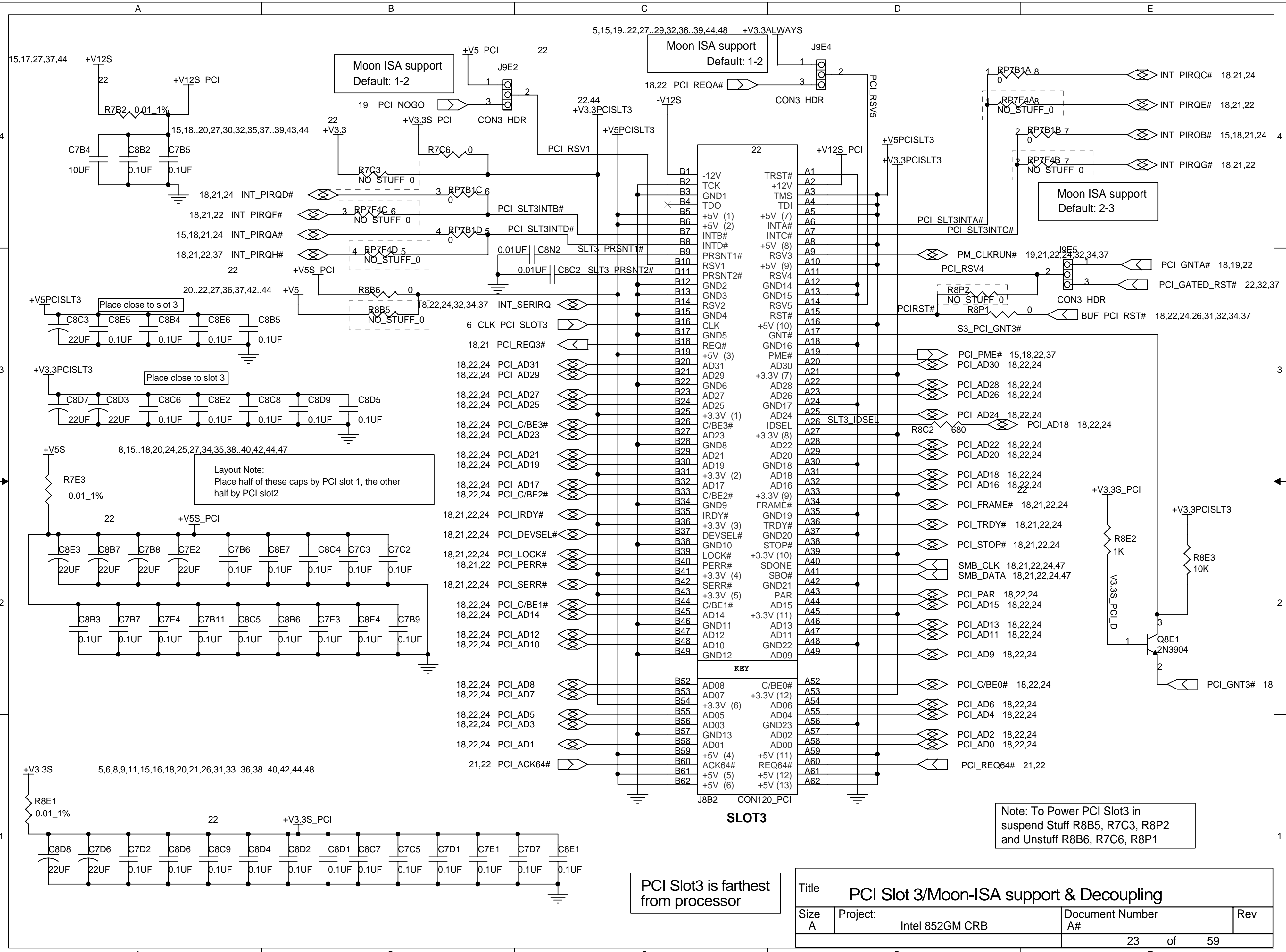
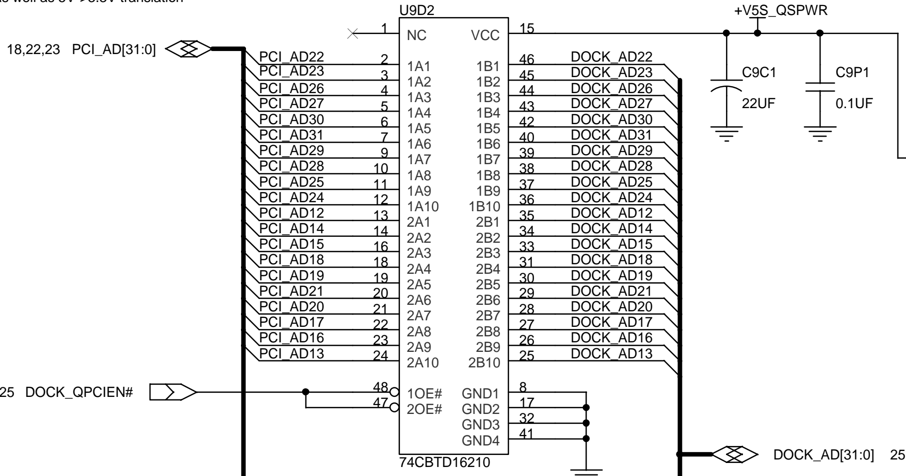
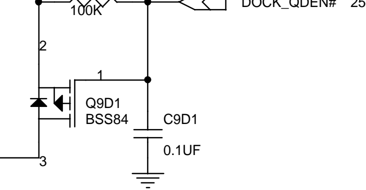


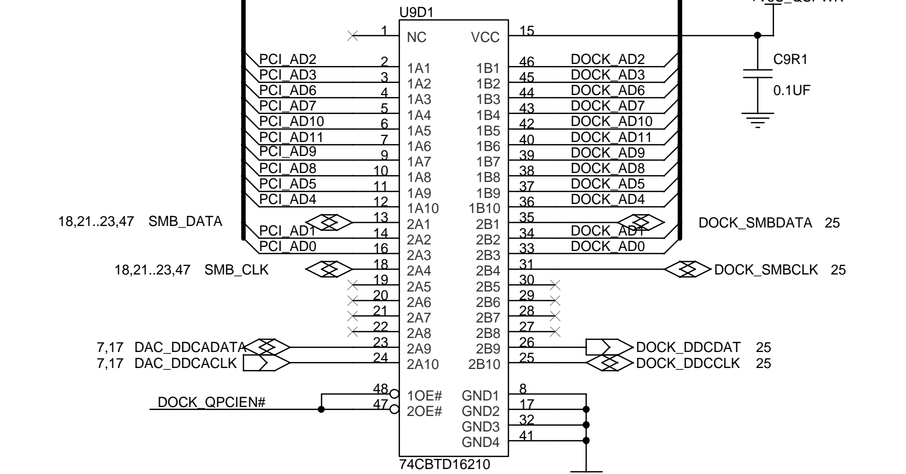
Title: PCI Slot 3/Moon-ISA support & Decoupling

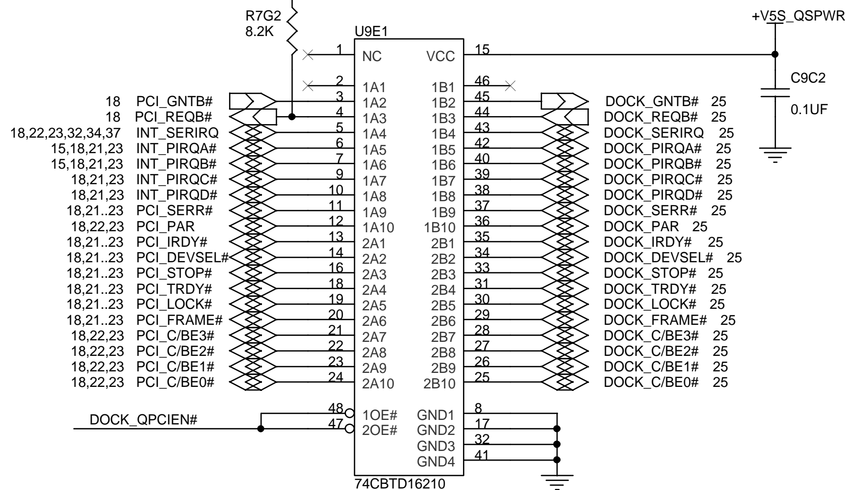
Size: A | Project: Intel 852GM CRB | Document Number: A# | Rev

Qbuffers used for isolation during suspend
as well as 5V->3.3V translation





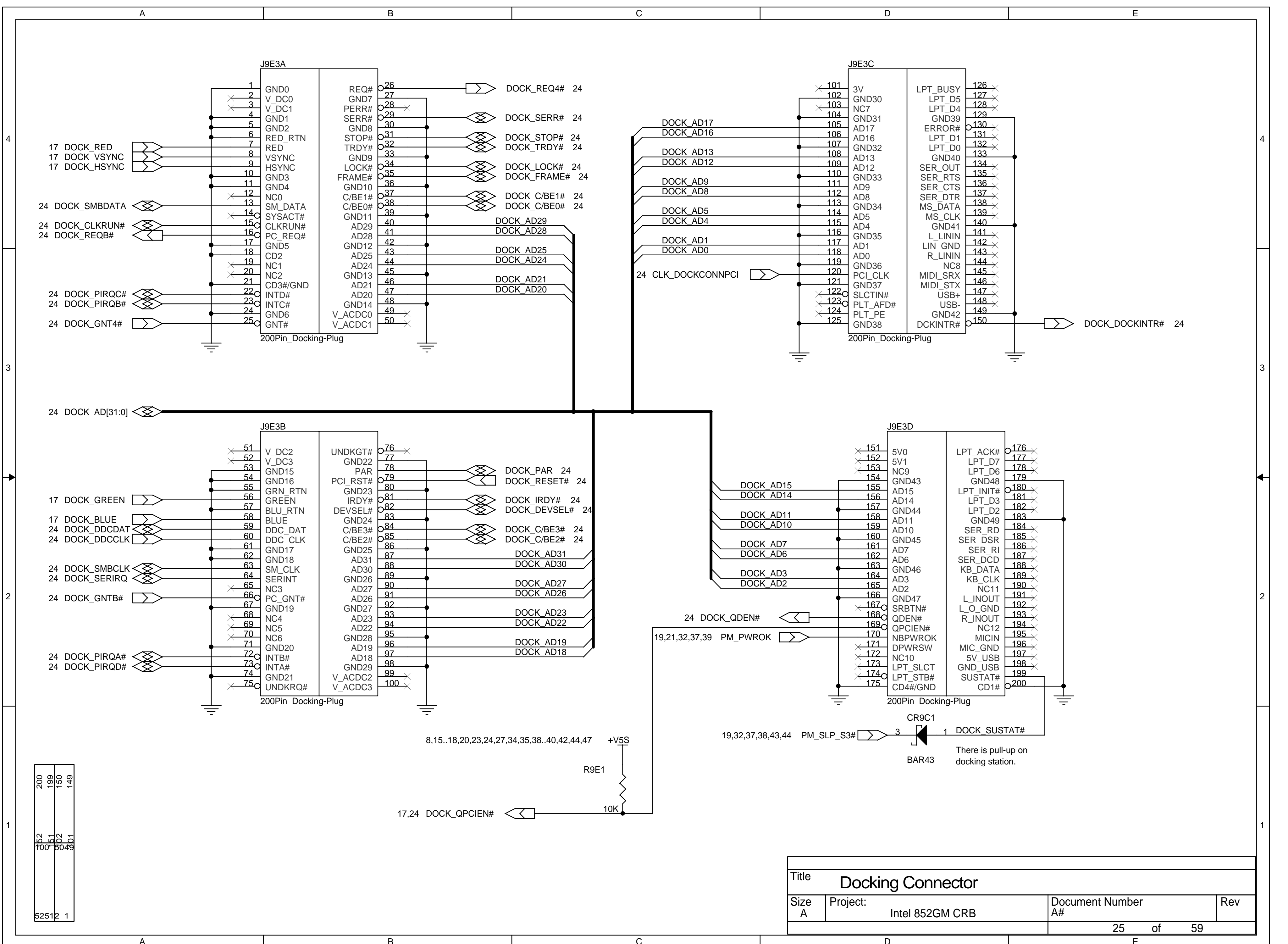




U9C1 — SN74CBTD3384 QUIET DOCK QSWITCH

+V5S_QSPWR

Title	Docking Q-Switches	
Size: A	Project: Intel 852GM CRB	Document Number: A#
		24 of 59



Title	Docking Connector		
Size A	Project: Intel 852GM CRB	Document Number A#	Rev
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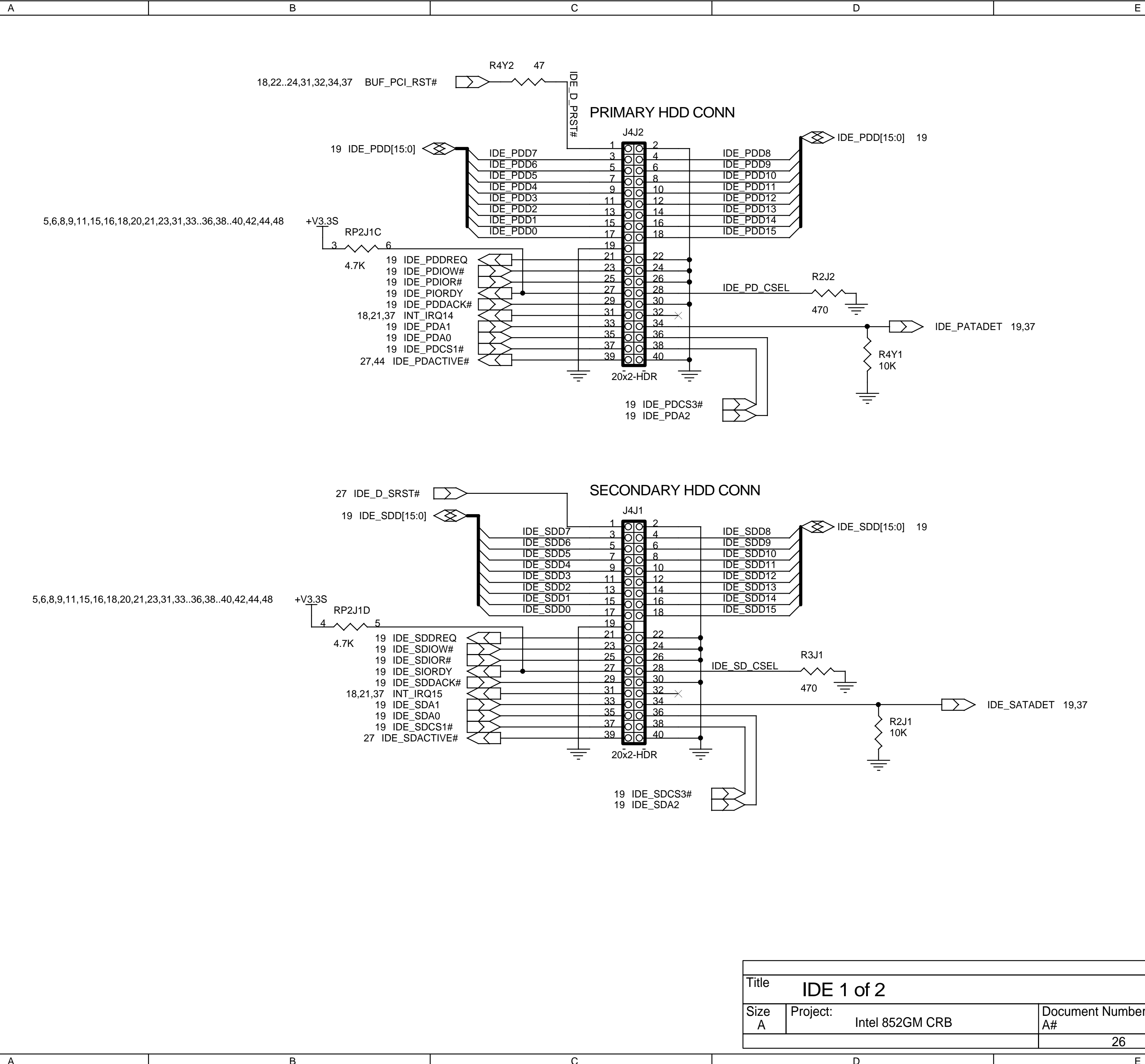

Title	IDE 1 of 2		
Size A	Project: Intel 852GM CRB	Document Number A#	Rev
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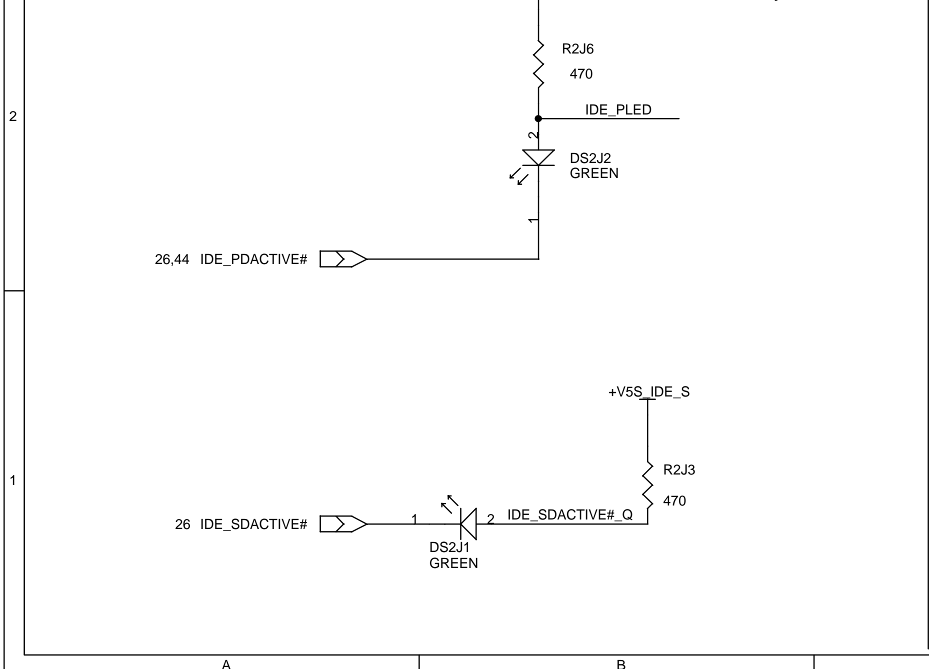
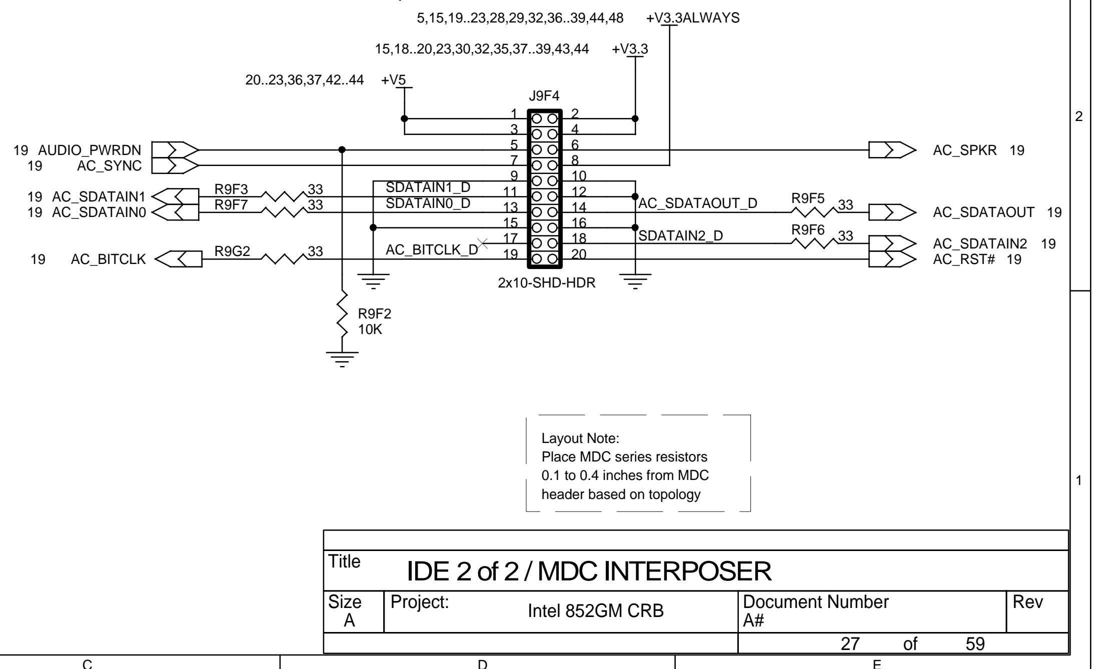
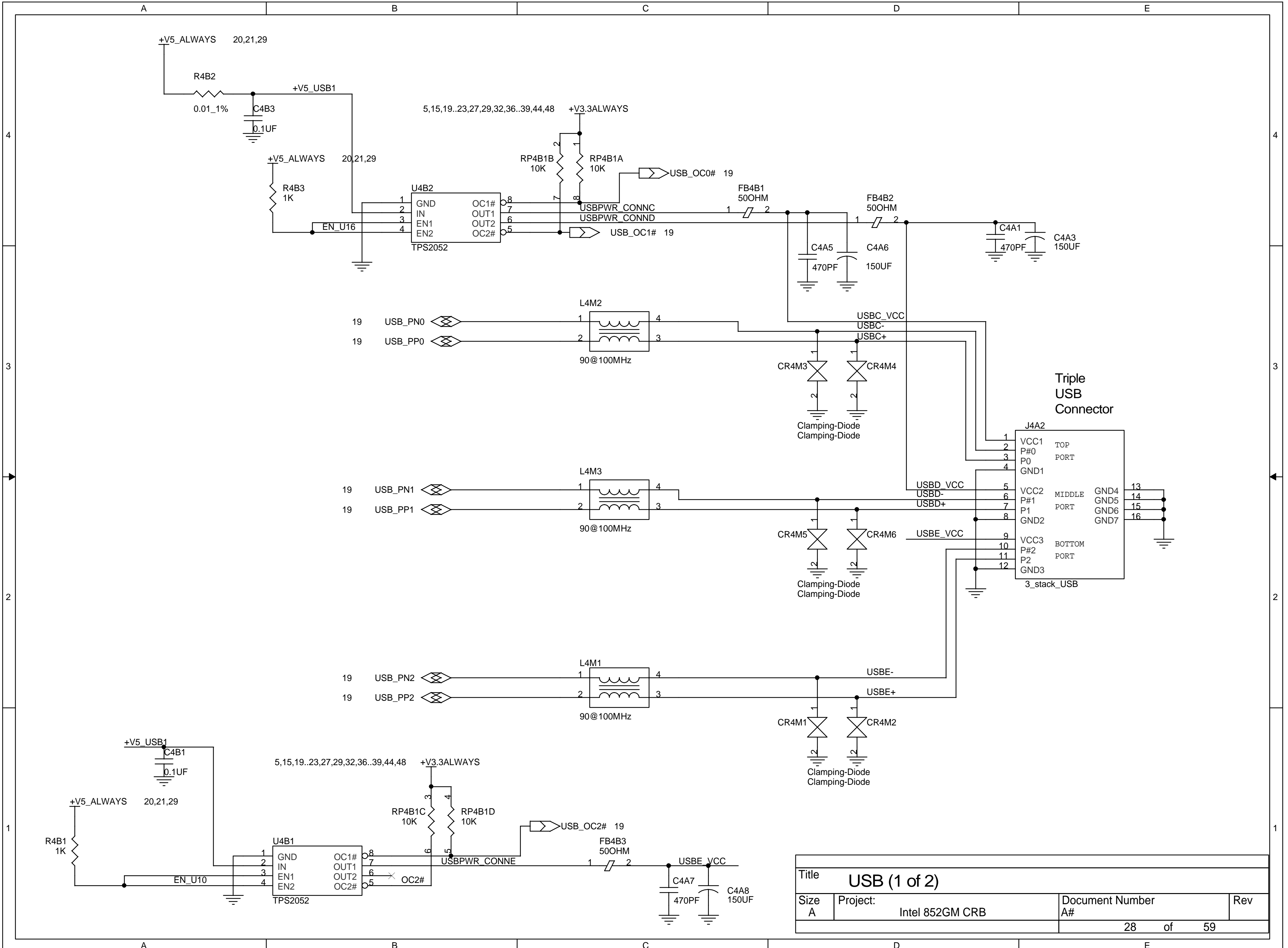
Secondary IDE Power

8,15..18,20,23..25,34,35,38..40,42,44,47 +V5S
U3H1A 74HC14
C2H1 0.1UF
34,37 IDE_SPWR_EN#
IDE_SPWR_EN
U3H1E 74HC14
IDE_SPWR2_D
R2H5 1M
R2H6 390K
IDE_SPWR2
C2H2 1000PF
U2H1A SI4925DY
U2H1B SI4925DY
R2H1 NO_STUFF_0
V5S_IDE_PD
Note: Primary IDE Power on Turner DC/DC Module
+V5S_IDE_S
R2H8 100K
SHMIDT4
R2W1 1M
C2W1 0.1UF
U3H1D 74HC14
SHMIDT2
U3H1B 74HC14
IDE_SRST#
R3H2 47
IDE_D_SRST# 26
R2H7 0.01_1%
C2W3 0.1UF
C2J1 22UF
C2W2 0.1UF
C2H3 100uF
+V12S_IDE_S
J2H1 4Pin_PwrConn
Q3H1 BSS138
IDE_SPWR_EN#
15,17,23,37,44 +V12S
IDE_SPWR_EN_Q#
R2G11 1M
R2G10 100K
C2G14 1000PF
IDE_SPWR_EN_D#
Q2G4 SI2307DS
Q3G1 2N7002
IDE_SPWR_EN
8,15..18,20,23..25,34,35,38..40,42,44,47 +V5S
SPARE GATE
U3H1C 74HC14
SHMIDT3
TP_SHMIDT_C
R3H1 0

For Secondary IDE Drive Only







Title	USB (1 of 2)		
Size A	Project: Intel 852GM CRB	Document Number A#	Rev
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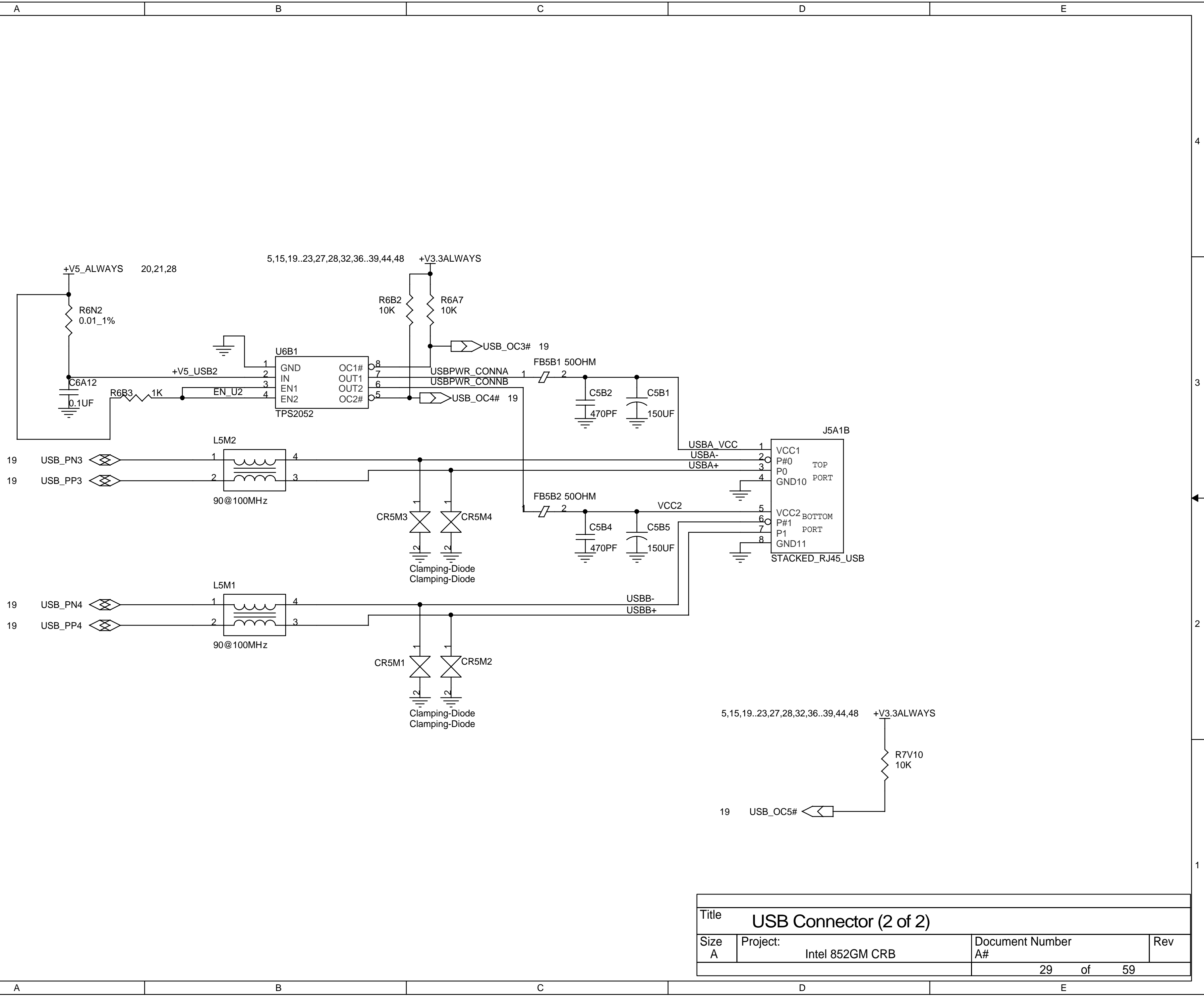

Title	USB Connector (2 of 2)		
Size A	Project: Intel 852GM CRB	Document Number A#	Rev
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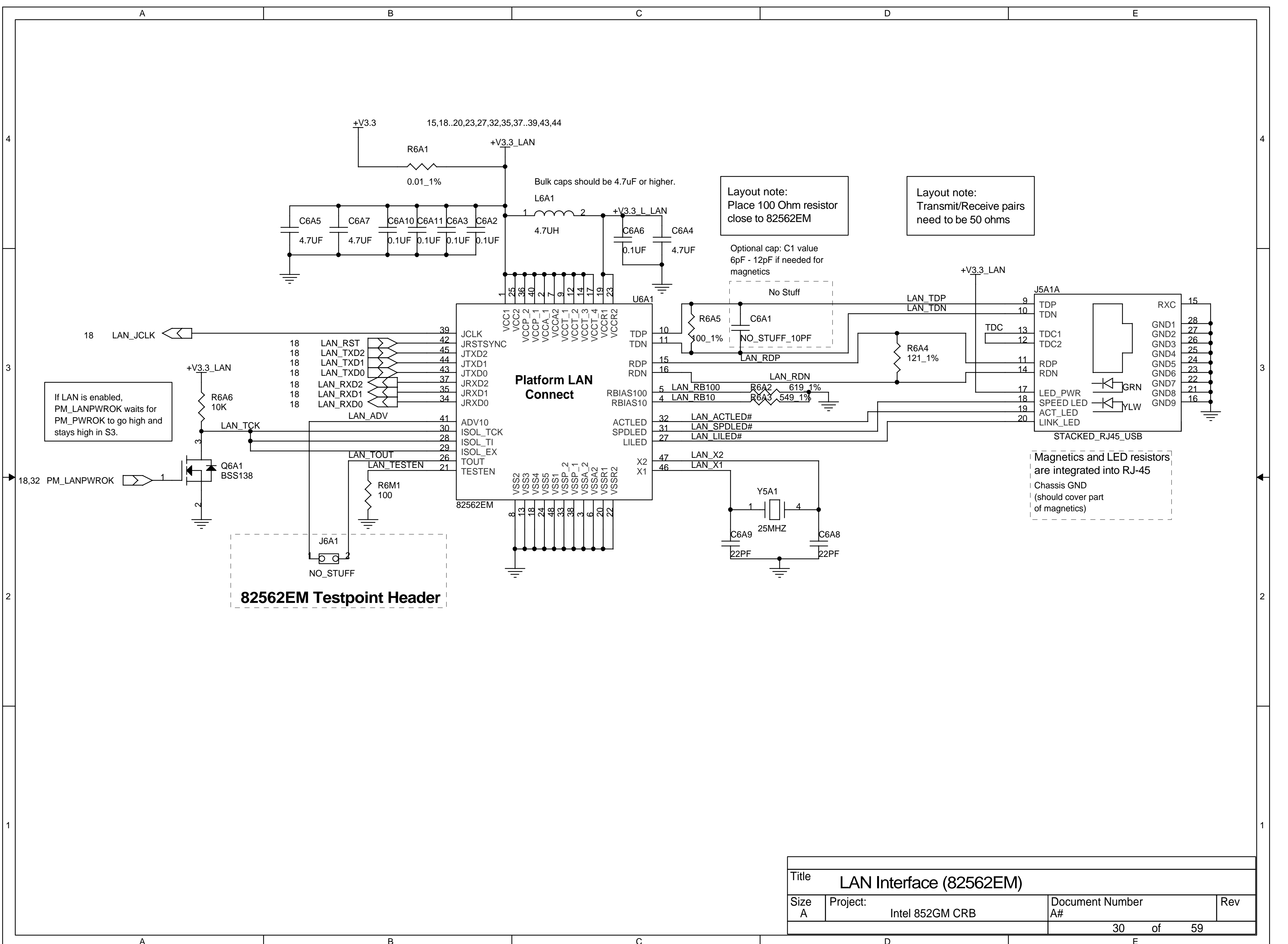

+V3.3
15,18..20,23,27,32,35,37..39,43,44
R6A1
0.01_1%
+V3.3_LAN
Bulk caps should be 4.7uF or higher.
L6A1
4.7UH
+V3.3_L_LAN
C6A5 4.7UF
C6A7 4.7UF
C6A10 0.1UF
C6A11 0.1UF
C6A3 0.1UF
C6A2 0.1UF
C6A6 0.1UF
C6A4 4.7UF
Layout note:
Place 100 Ohm resistor close to 82562EM
Layout note:
Transmit/Receive pairs need to be 50 ohms
Optional cap: C1 value 6pF - 12pF if needed for magnetics
No Stuff
R6A5 100_1%
C6A1 NO_STUFF_10PF
+V3.3_LAN
J5A1A
LAN_TDP
LAN_TDN
LAN_RDP
LAN_RDN
R6A4 121_1%
TDC
U6A1
18 LAN_JCLK
18 LAN_RST
18 LAN_TXD2
18 LAN_TXD1
18 LAN_TXD0
18 LAN_RXD2
18 LAN_RXD1
18 LAN_RXD0
Platform LAN Connect
JCLK JRSTSYNC JTXD2 JTXD1 JTXD0 JRXD2 JRXD1 JRXD0 ADV10 ISOL_TCK ISOL_TI ISOL_EX TOUT TESTEN
TDP TDN RDP RDN RBIAS100 RBIAS10 ACTLED SPDLED LILED X2 X1
VCC1 VCC2 VCCP_2 VCCP_1 VCCA_1 VCCA2 VCCT_1 VCCT_2 VCCT_3 VCCT_4 VCCR1 VCCR2
VSS2 VSS3 VSS4 VSS5 VSS1 VSSP_2 VSSP_1 VSSA_2 VSSA2 VSSR1 VSSR2
82562EM
LAN_RB100 R6A2 619_1%
LAN_RB10 R6A3 549_1%
LAN_ACTLED#
LAN_SPDLED#
LAN_LILED#
LAN_X2
LAN_X1
TDP TDN TDC1 TDC2 RDP RDN LED_PWR SPEED LED ACT_LED LINK_LED
RXC GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND8 GND9
GRN
YLW
STACKED_RJ45_USB
Magnetics and LED resistors are integrated into RJ-45
Chassis GND (should cover part of magnetics)
Y5A1 25MHZ
C6A9 22PF
C6A8 22PF
+V3.3_LAN
R6A6 10K
If LAN is enabled, PM_LANPWROK waits for PM_PWROK to go high and stays high in S3.
LAN_TCK
LAN_ADV
LAN_TOUT
LAN_TESTEN
R6M1 100
Q6A1 BSS138
18,32 PM_LANPWROK
J6A1
NO_STUFF
82562EM Testpoint Header
Title
LAN Interface (82562EM)
Size A
Project: Intel 852GM CRB
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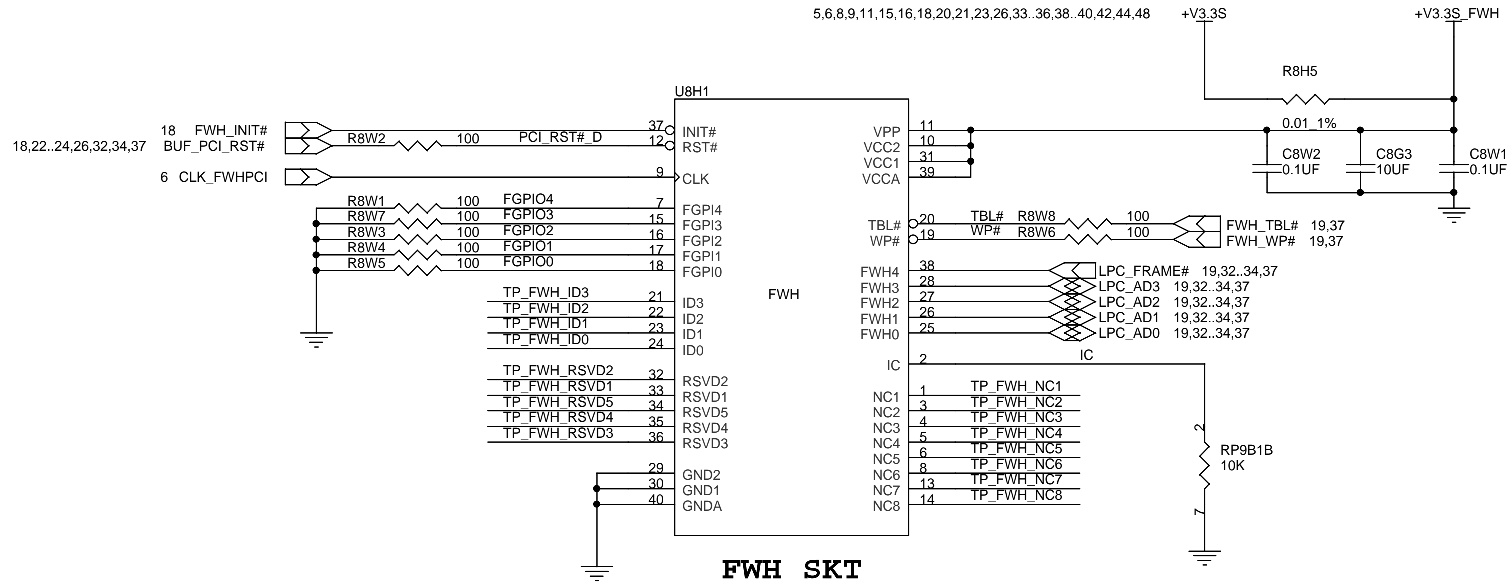

FWH sits in the
FWH_TSOP_Socket,
Not on the board

Title	FWH		
Size A	Project: Intel 852GM CRB	Document Number A#	Rev
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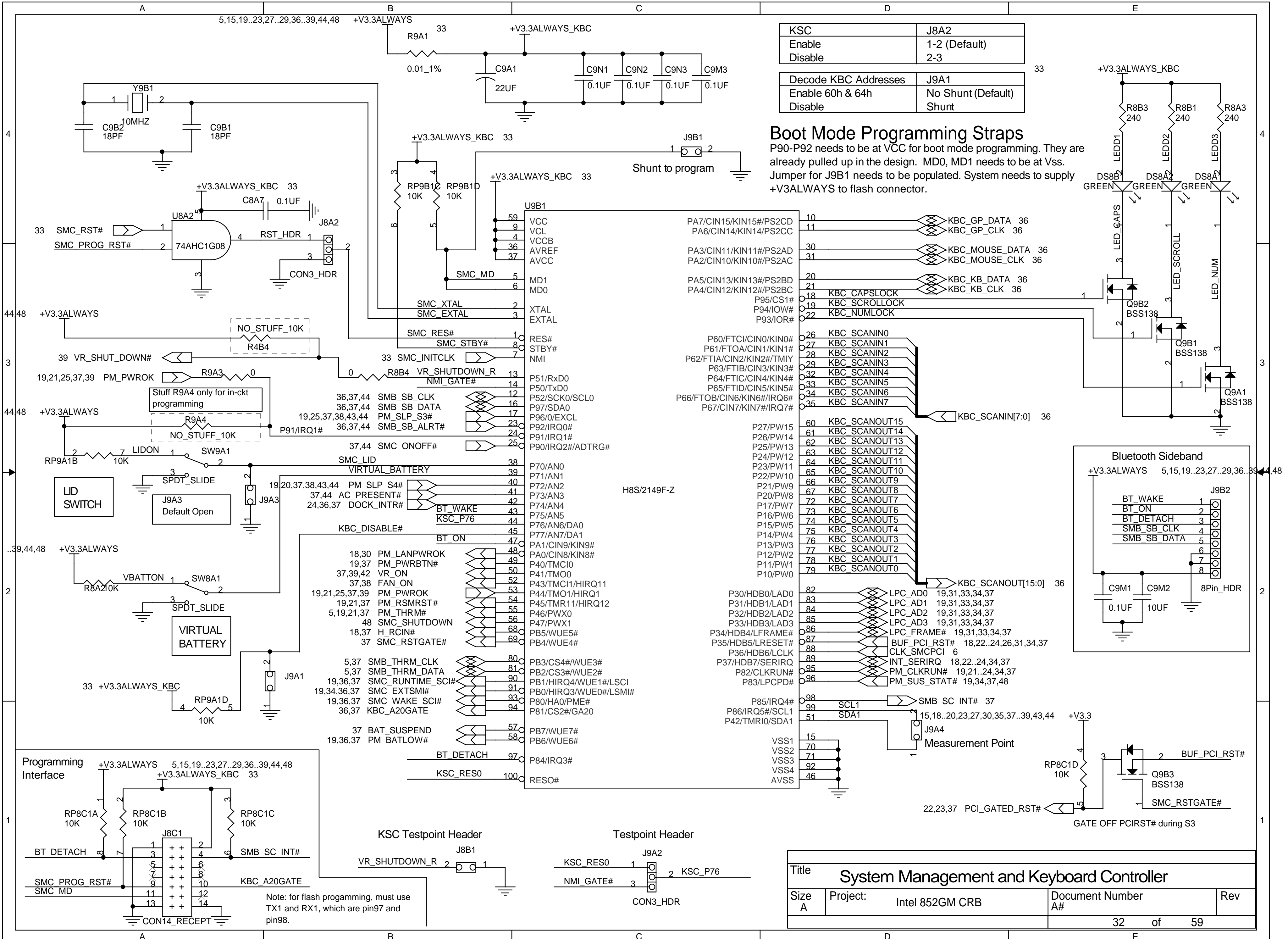

KSC | J8A2
Enable | 1-2 (Default)
Disable | 2-3
Decode KBC Addresses | J9A1
Enable 60h & 64h | No Shunt (Default)
Disable | Shunt
Boot Mode Programming Straps
P90-P92 needs to be at VCC for boot mode programming. They are already pulled up in the design. MD0, MD1 needs to be at Vss. Jumper for J9B1 needs to be populated. System needs to supply +V3ALWAYS to flash connector.
Shunt to program
J9B1
+V3.3ALWAYS
+V3.3ALWAYS_KBC
R9A1
0.01_1%
C9A1
22UF
C9N1
C9N2
C9N3
C9M3
0.1UF
Y9B1
10MHZ
C9B2
18PF
C9B1
18PF
RP9B1C
RP9B1D
10K
U8A2
74AHC1G08
SMC_RST#
SMC_PROG_RST#
RST_HDR
J8A2
CON3_HDR
C8A7
U9B1
H8S/2149F-Z
VCC
VCL
VCCB
AVREF
AVCC
MD1
MD0
XTAL
EXTAL
RES#
STBY#
NMI
SMC_MD
SMC_XTAL
SMC_EXTAL
SMC_RES#
SMC_STBY#
SMC_INITCLK
NO_STUFF_10K
R4B4
VR_SHUT_DOWN#
PM_PWROK
R9A3
R8B4
VR_SHUTDOWN_R
NMI_GATE#
Stuff R9A4 only for in-ckt programming
R9A4
P91/IRQ1#
RP9A1B
LIDON
SW9A1
SPDT_SLIDE
LID SWITCH
J9A3
Default Open
SMC_LID
VIRTUAL_BATTERY
PM_SLP_S4#
AC_PRESENT#
DOCK_INTR#
BT_WAKE
KSC_P76
KBC_DISABLE#
BT_ON
VBATTON
SW8A1
R8A2
VIRTUAL BATTERY
J9A1
RP9A1D
SMB_SB_CLK
SMB_SB_DATA
PM_SLP_S3#
SMB_SB_ALRT#
SMC_ONOFF#
PM_LANPWROK
PM_PWRBTN#
VR_ON
FAN_ON
PM_RSMRST#
PM_THRM#
SMC_SHUTDOWN
H_RCIN#
SMC_RSTGATE#
SMB_THRM_CLK
SMB_THRM_DATA
SMC_RUNTIME_SCI#
SMC_EXTSMI#
SMC_WAKE_SCI#
KBC_A20GATE
BAT_SUSPEND
PM_BATLOW#
BT_DETACH
KSC_RES0
RESO#
KBC_GP_DATA
KBC_GP_CLK
KBC_MOUSE_DATA
KBC_MOUSE_CLK
KBC_KB_DATA
KBC_KB_CLK
KBC_CAPSLOCK
KBC_SCROLLOCK
KBC_NUMLOCK
KBC_SCANIN0 … KBC_SCANIN7
KBC_SCANIN[7:0]
KBC_SCANOUT0 … KBC_SCANOUT15
KBC_SCANOUT[15:0]
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LPC_FRAME#
BUF_PCI_RST#
CLK_SMCPCI
INT_SERIRQ
PM_CLKRUN#
PM_SUS_STAT#
SMB_SC_INT#
SCL1
SDA1
J9A4
Measurement Point
VSS1
VSS2
VSS3
VSS4
AVSS
R8B3
R8B1
R8A3
240
LEDD1
LEDD2
LEDD3
DS8B1
DS8A2
DS8A1
GREEN
LED_CAPS
LED_SCROLL
LED_NUM
Q9B2
Q9B1
Q9A1
BSS138
Bluetooth Sideband
J9B2
BT_DETACH
8Pin_HDR
C9M1
C9M2
10UF
RP8C1D
Q9B3
SMC_RSTGATE#
PCI_GATED_RST#
GATE OFF PCIRST# during S3
Programming Interface
RP8C1A
RP8C1B
RP8C1C
J8C1
CON14_RECEPT
SMB_SC_INT#
SMC_PROG_RST#
SMC_MD
KBC_A20GATE
Note: for flash progamming, must use TX1 and RX1, which are pin97 and pin98.
KSC Testpoint Header
J8B1
VR_SHUTDOWN_R
Testpoint Header
J9A2
KSC_RES0
NMI_GATE#
KSC_P76
CON3_HDR
Title
System Management and Keyboard Controller
Size
A
Project:
Intel 852GM CRB
Document Number
A#
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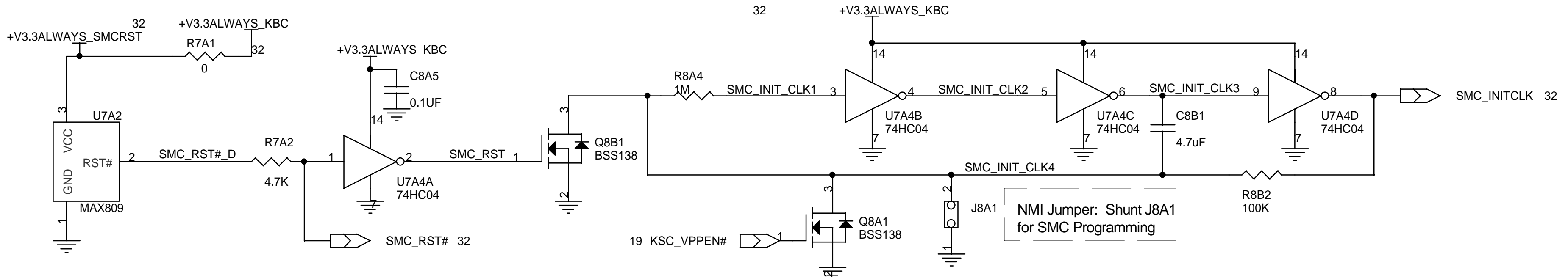
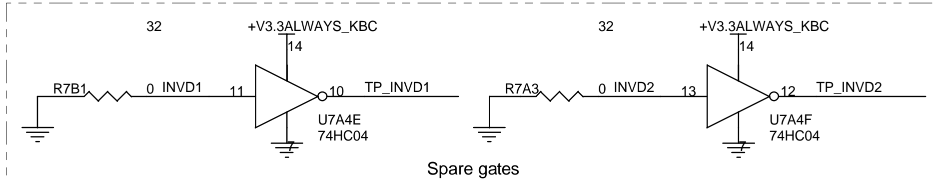
SMC SUSPEND TIMER



Circuitry provides an interrupt to the SMC every 1s while in suspend (this allows the SMC to complete housekeeping functions while suspended)

1Hz Clock	J8A1
Disable	Shunt (Default)
Enable	No Shunt



Spare gates

PORT 80-83 DISPLAY

Port	J9H1
82-83	Shunt
80-81	No Shunt (Default)

CR9G1 7-SEG-LED-DISPLAY High Nibble (Left)

CR9G2 7-SEG-LED-DISPLAY Low Nibble (Right) — PORT 80, 82

CR9H2 7-SEG-LED-DISPLAY High Nibble (Left)

CR9H1 7-SEG-LED-DISPLAY Low Nibble (Right) — PORT 81, 83

LED_SEGA, LED_SEGB, LED_SEGC, LED_SEGD, LED_SEGE, LED_SEGF, LED_SEGG, LED_SEGDP

7SEG_LED_CT1, 7SEG_LED_CT2, 7SEG_LED_CT3, 7SEG_LED_CT4

5,6,8,9,11,15,16,18,20,21,23,26,31,34..36,38..40,42,44,48 +V3.3S

RP8H5D, RP8H5C, RP8H5B, RP8H4D, RP8H4B, RP8H4C, RP8H4A, RP8H5A 150

U9H1 EPM7064STC

LPC_FRAME# 19,31,32,34,37

PORT82_EN#

J9H1

PLD_PD

R9W2 10K

LED_MUX_HI81, LED_MUX_LO81, LED_MUX_HI80, LED_MUX_LO80

6 CLK_PCI_PORT80

7,8,10,15,18 PCI_RST#

OE#_PORT80

R9W1 100

R8J13 1K

SUS_CLK_Q

19,37 SUS_CLK

Q8J4 BSS138

LPC_AD3 19,31,32,34,37
LPC_AD2 19,31,32,34,37
LPC_AD1 19,31,32,34,37
LPC_AD0 19,31,32,34,37

C9W1 0.1UF, C9W4 0.1UF, C9W3 0.1UF, C9Y1 0.1UF, C9W2 0.1UF, C9H1 10UF

Q9H1 2N3904, Q8H3 2N3904, Q8H4 2N3904, Q8J1 2N3904

LED_MUX_HI81 RP9H1A 150 LED_MUX_HI81_D
LED_MUX_HI80 RP9H1B 150 LED_MUX_HI80_D
LED_MUX_LO81 RP9H1C 150 LED_MUX_LO81_D
LED_MUX_LO80 RP9H1D 150 LED_MUX_LO80_D

Title	SMC Suspend Timer and Port 80 LEDs		
Size A	Project: Intel 852GM CRB	Document Number A#	Rev
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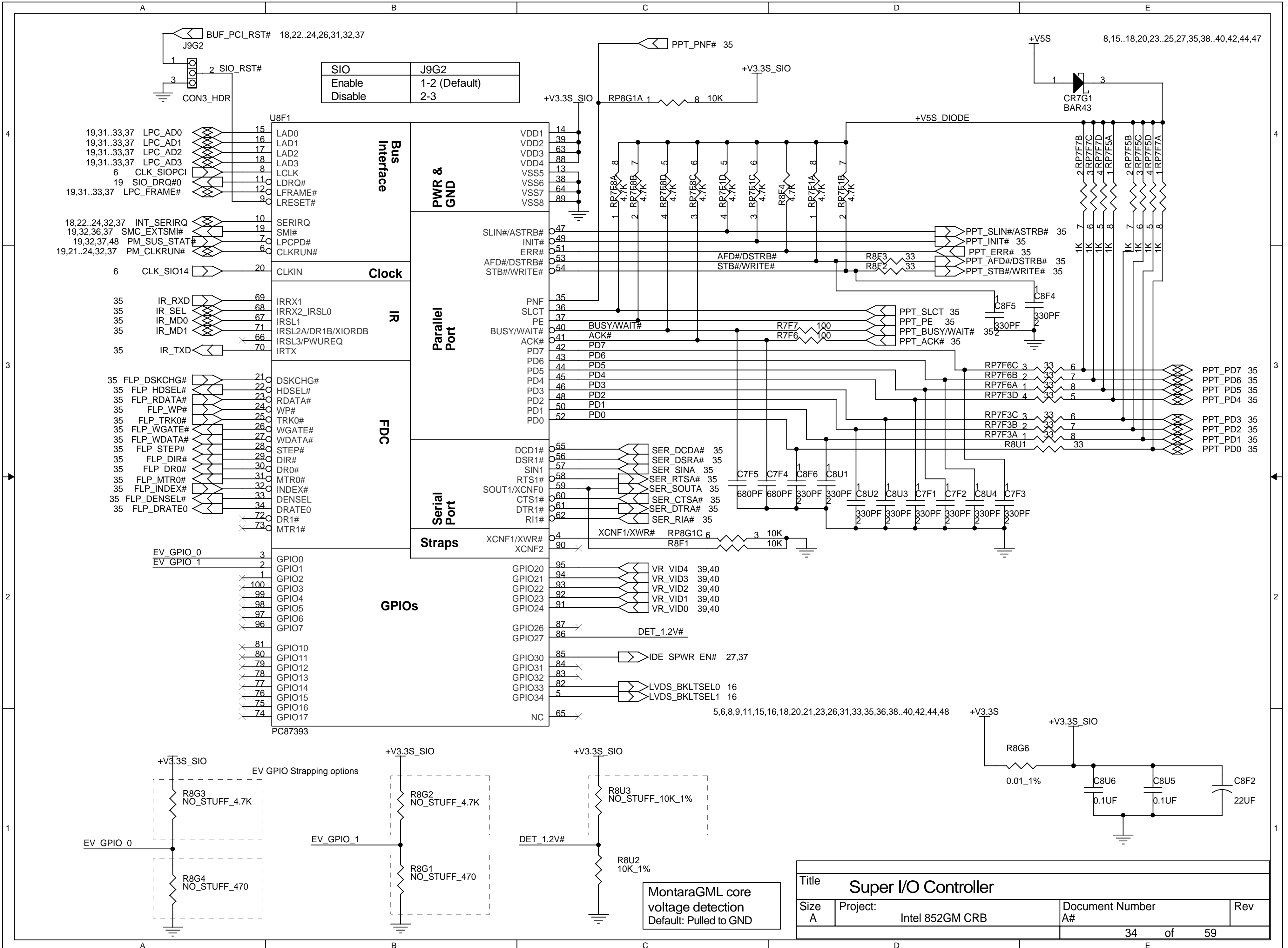

BUF_PCI_RST# 18,22..24,26,31,32,37
J9G2
SIO_RST#
CON3_HDR
SIO | J9G2
Enable | 1-2 (Default)
Disable | 2-3
PPT_PNF# 35
+V3.3S_SIO
RP8G1A 10K
+V5S
8,15..18,20,23..25,27,35,38..40,42,44,47
CR7G1
BAR43
+V5S_DIODE
U8F1
Bus Interface
LAD0
LAD1
LAD2
LAD3
LCLK
LDRQ#
LFRAME#
LRESET#
19,31..33,37 LPC_AD0
19,31..33,37 LPC_AD1
19,31..33,37 LPC_AD2
19,31..33,37 LPC_AD3
6 CLK_SIOPCI
19 SIO_DRQ#0
19,31..33,37 LPC_FRAME#
18,22..24,32,37 INT_SERIRQ
19,32,36,37 SMC_EXTSMI#
19,32,37,48 PM_SUS_STAT#
19,21..24,32,37 PM_CLKRUN#
SERIRQ
SMI#
LPCPD#
CLKRUN#
6 CLK_SIO14
CLKIN
Clock
IR
IRRX1
IRRX2_IRSL0
IRSL1
IRSL2A/DR1B/XIORDB
IRSL3/PWUREQ
IRTX
35 IR_RXD
35 IR_SEL
35 IR_MD0
35 IR_MD1
35 IR_TXD
FDC
DSKCHG#
HDSEL#
RDATA#
WP#
TRK0#
WGATE#
WDATA#
STEP#
DIR#
DR0#
MTR0#
INDEX#
DENSEL
DRATE0
DR1#
MTR1#
35 FLP_DSKCHG#
35 FLP_HDSEL#
35 FLP_RDATA#
35 FLP_WP#
35 FLP_TRK0#
35 FLP_WGATE#
35 FLP_WDATA#
35 FLP_STEP#
35 FLP_DIR#
35 FLP_DR0#
35 FLP_MTR0#
35 FLP_INDEX#
35 FLP_DENSEL#
35 FLP_DRATE0
PWR & GND
VDD1
VDD2
VDD3
VDD4
VSS5
VSS6
VSS7
VSS8
Parallel Port
SLIN#/ASTRB#
INIT#
ERR#
AFD#/DSTRB#
STB#/WRITE#
PNF
SLCT
PE
BUSY/WAIT#
ACK#
PD7
PD6
PD5
PD4
PD3
PD2
PD1
PD0
PPT_SLIN#/ASTRB# 35
PPT_INIT# 35
PPT_ERR# 35
PPT_AFD#/DSTRB# 35
PPT_STB#/WRITE# 35
PPT_SLCT 35
PPT_PE 35
PPT_BUSY/WAIT# 35
PPT_ACK# 35
PPT_PD7 35
PPT_PD6 35
PPT_PD5 35
PPT_PD4 35
PPT_PD3 35
PPT_PD2 35
PPT_PD1 35
PPT_PD0 35
Serial Port
DCD1#
DSR1#
SIN1
RTS1#
SOUT1/XCNF0
CTS1#
DTR1#
RI1#
SER_DCDA# 35
SER_DSRA# 35
SER_SINA 35
SER_RTSA# 35
SER_SOUTA 35
SER_CTSA# 35
SER_DTRA# 35
SER_RIA# 35
Straps
XCNF1/XWR#
XCNF2
RP8G1C 10K
R8F1 10K
GPIOs
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO10
GPIO11
GPIO12
GPIO13
GPIO14
GPIO15
GPIO16
GPIO17
GPIO20
GPIO21
GPIO22
GPIO23
GPIO24
GPIO26
GPIO27
GPIO30
GPIO31
GPIO32
GPIO33
GPIO34
NC
EV_GPIO_0
EV_GPIO_1
VR_VID4 39,40
VR_VID3 39,40
VR_VID2 39,40
VR_VID1 39,40
VR_VID0 39,40
DET_1.2V#
IDE_SPWR_EN# 27,37
LVDS_BKLTSEL0 16
LVDS_BKLTSEL1 16
PC87393
5,6,8,9,11,15,16,18,20,21,23,26,31,33,35,36,38..40,42,44,48
+V3.3S
R8G6
0.01_1%
C8U6 0.1UF
C8U5 0.1UF
C8F2 22UF
EV GPIO Strapping options
R8G3 NO_STUFF_4.7K
R8G4 NO_STUFF_470
R8G2 NO_STUFF_4.7K
R8G1 NO_STUFF_470
R8U3 NO_STUFF_10K_1%
R8U2 10K_1%
MontaraGML core voltage detection
Default: Pulled to GND
Title
Super I/O Controller
Size A
Project: Intel 852GM CRB
Document Number A#
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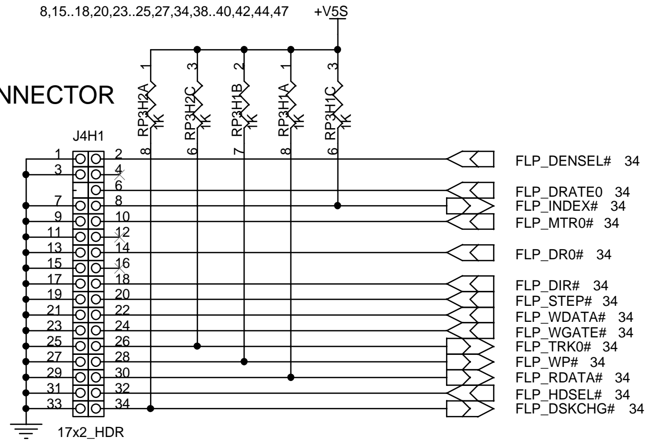

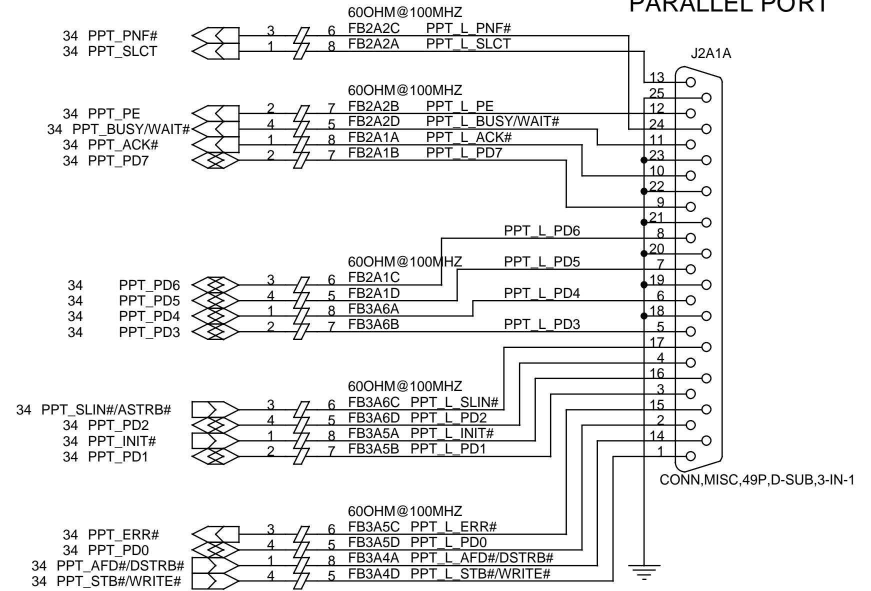

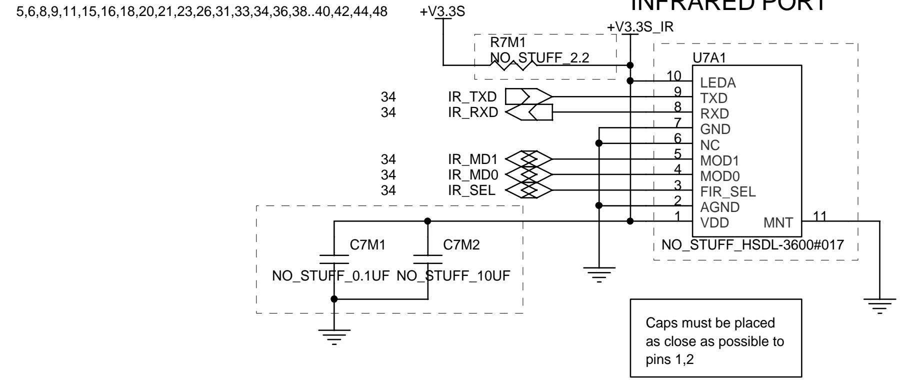

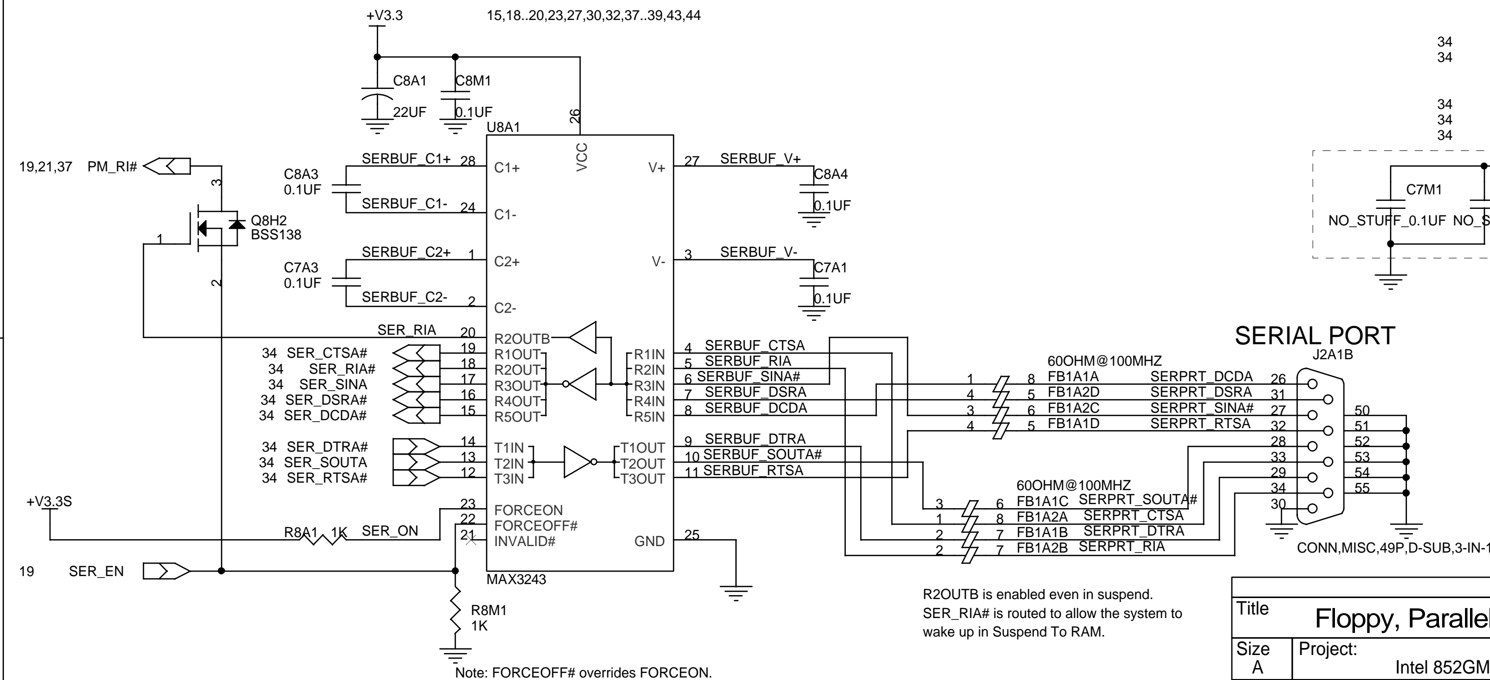

Title	Floppy, Parallel, Serial, and IR Ports		
Size A	Project: Intel 852GM CRB	Document Number A#	Rev
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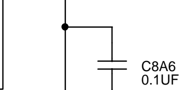
Scan Matrix Key Board

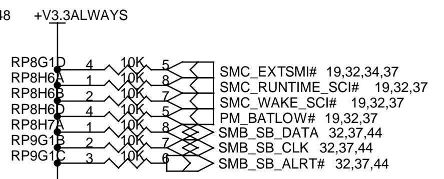
J9D1 NO_STUFF_24Pin_ZIF-HDR

KBC_SCANOUT[15:0] 32

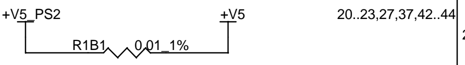
KBC_SCANIN[7:0] 32

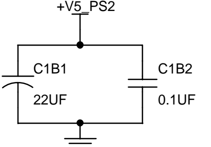


U8A3 SN74CBTD3384



J1A1 DUAL_PS2





If a PS/2 "breakout" connector is used,the keyboard PS/2 connector can be used for both a PS/2 keyboard and a second PS/2 mouse. Otherwise, the keyboard PS/2 connector will only support a PS/2 keyboard.

Title	Keyboard and Mouse Connectors		
Size A	Project: Intel 852GM CRB	Document Number A#	Rev
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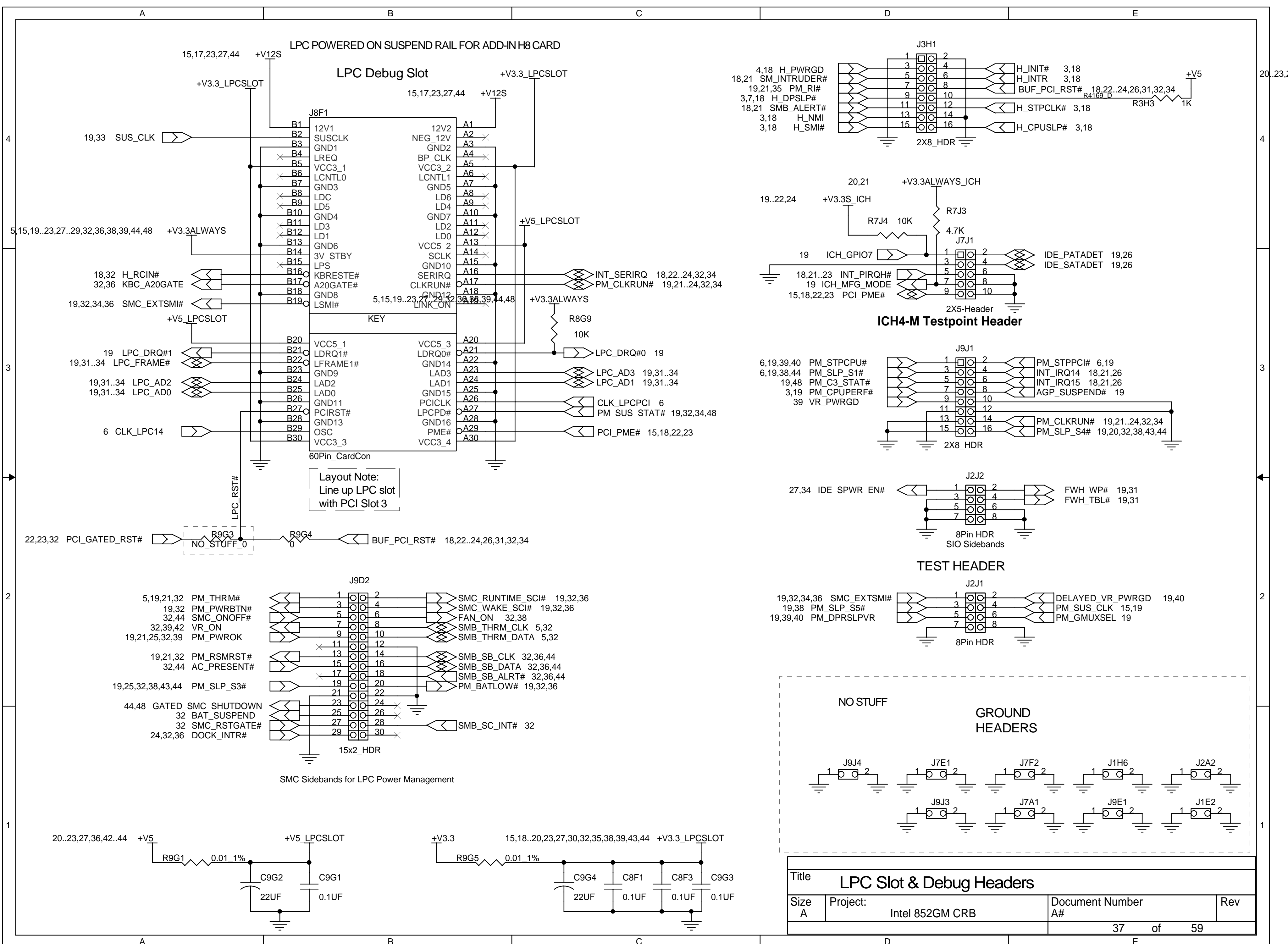

LPC POWERED ON SUSPEND RAIL FOR ADD-IN H8 CARD
LPC Debug Slot
J8F1
60Pin_CardCon
KEY
12V1
SUSCLK
GND1
LREQ
VCC3_1
LCNTL0
GND3
LDC
LD5
GND4
LD3
LD1
GND6
3V_STBY
LPS
KBRESTE#
A20GATE#
GND8
LSMI#
12V2
NEG_12V
GND2
BP_CLK
VCC3_2
LCNTL1
GND5
LD6
LD4
GND7
LD2
LD0
VCC5_2
SCLK
GND10
SERIRQ
CLKRUN#
GND12
LINK_ON
VCC5_1
LDRQ1#
LFRAME1#
GND9
LAD2
LAD0
GND11
PCIRST#
GND13
OSC
VCC3_3
VCC5_3
LDRQ0#
GND14
LAD3
LAD1
GND15
PCICLK
LPCPD#
GND16
PME#
VCC3_4
15,17,23,27,44 +V12S
+V3.3_LPCSLOT
19,33 SUS_CLK
5,15,19..23,27..29,32,36,38,39,44,48 +V3.3ALWAYS
18,32 H_RCIN#
32,36 KBC_A20GATE
19,32,34,36 SMC_EXTSMI#
+V5_LPCSLOT
19 LPC_DRQ#1
19,31..34 LPC_FRAME#
19,31..34 LPC_AD2
19,31..34 LPC_AD0
6 CLK_LPC14
INT_SERIRQ 18,22..24,32,34
PM_CLKRUN# 19,21..24,32,34
+V3.3ALWAYS
R8G9
10K
LPC_DRQ#0 19
LPC_AD3 19,31..34
LPC_AD1 19,31..34
CLK_LPCPCI 6
PM_SUS_STAT# 19,32,34,48
PCI_PME# 15,18,22,23
Layout Note:
Line up LPC slot
with PCI Slot 3
LPC_RST#
22,23,32 PCI_GATED_RST#
R9G3
NO_STUFF_0
R9G4
0
BUF_PCI_RST# 18,22..24,26,31,32,34
J9D2
15x2_HDR
5,19,21,32 PM_THRM#
19,32 PM_PWRBTN#
32,44 SMC_ONOFF#
32,39,42 VR_ON
19,21,25,32,39 PM_PWROK
19,21,32 PM_RSMRST#
32,44 AC_PRESENT#
19,25,32,38,43,44 PM_SLP_S3#
44,48 GATED_SMC_SHUTDOWN
32 BAT_SUSPEND
32 SMC_RSTGATE#
24,32,36 DOCK_INTR#
SMC_RUNTIME_SCI# 19,32,36
SMC_WAKE_SCI# 19,32,36
FAN_ON 32,38
SMB_THRM_CLK 5,32
SMB_THRM_DATA 5,32
SMB_SB_CLK 32,36,44
SMB_SB_DATA 32,36,44
SMB_SB_ALRT# 32,36,44
PM_BATLOW# 19,32,36
SMB_SC_INT# 32
SMC Sidebands for LPC Power Management
20..23,27,36,42..44 +V5
+V5_LPCSLOT
R9G1 0.01_1%
C9G2 22UF
C9G1 0.1UF
+V3.3
15,18..20,23,27,30,32,35,38,39,43,44 +V3.3_LPCSLOT
R9G5 0.01_1%
C9G4 22UF
C8F1 0.1UF
C8F3 0.1UF
C9G3 0.1UF
J3H1
2X8_HDR
4,18 H_PWRGD
18,21 SM_INTRUDER#
19,21,35 PM_RI#
3,7,18 H_DPSLP#
18,21 SMB_ALERT#
3,18 H_NMI
3,18 H_SMI#
H_INIT# 3,18
H_INTR 3,18
BUF_PCI_RST# 18,22..24,26,31,32,34
H_STPCLK# 3,18
H_CPUSLP# 3,18
+V5
R4169_D
R3H3 1K
20..23,2
20,21 +V3.3ALWAYS_ICH
19..22,24 +V3.3S_ICH
R7J3 4.7K
R7J4 10K
J7J1
2X5-Header
19 ICH_GPIO7
18,21..23 INT_PIRQH#
19 ICH_MFG_MODE
15,18,22,23 PCI_PME#
IDE_PATADET 19,26
IDE_SATADET 19,26
ICH4-M Testpoint Header
J9J1
2X8_HDR
6,19,39,40 PM_STPCPU#
6,19,38,44 PM_SLP_S1#
19,48 PM_C3_STAT#
3,19 PM_CPUPERF#
39 VR_PWRGD
PM_STPPCI# 6,19
INT_IRQ14 18,21,26
INT_IRQ15 18,21,26
AGP_SUSPEND# 19
PM_CLKRUN# 19,21..24,32,34
PM_SLP_S4# 19,20,32,38,43,44
J2J2
27,34 IDE_SPWR_EN#
FWH_WP# 19,31
FWH_TBL# 19,31
8Pin HDR
SIO Sidebands
TEST HEADER
J2J1
19,32,34,36 SMC_EXTSMI#
19,38 PM_SLP_S5#
19,39,40 PM_DPRSLPVR
DELAYED_VR_PWRGD 19,40
PM_SUS_CLK 15,19
PM_GMUXSEL 19
8Pin HDR
NO STUFF
GROUND
HEADERS
J9J4
J7E1
J7F2
J1H6
J2A2
J9J3
J7A1
J9E1
J1E2
Title
LPC Slot & Debug Headers
Size
A
Project:
Intel 852GM CRB
Document Number
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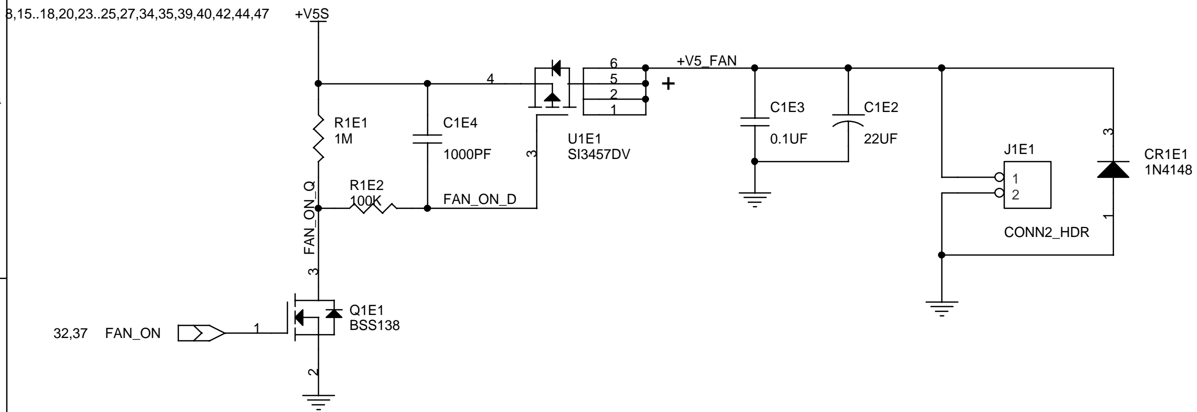
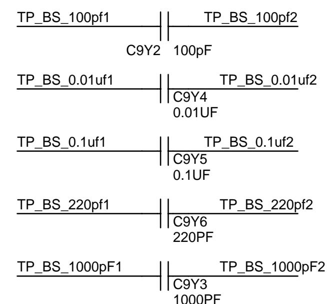
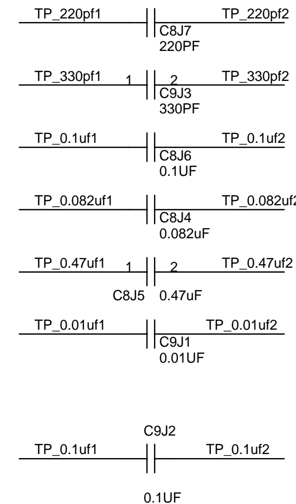






System State LEDs

9..23,27..29,32,36,37,39,44,48 +V3.3ALWAYS

19,37 PM_SLP_S5#

Q2G6
SI2307DS

S5_LED_C

R2H3
68

S5_LED_A

LED for S5

DS2H1
GREEN

5,15,19..23,27..29,32,36,37,39,44,48 +V3.3ALWAYS

19,20,32,37,43,44 PM_SLP_S4#

Q2G2
SI2307DS

S4_LED_C

R2H4
68

S4_LED_A

LED for S4

DS2H2
GREEN

19,37 PM_SLP_S5#

Q2G3
BSS138

15,18..20,23,27,30,32,35,37,39,43,44 +V3.3

19,25,32,37,43,44 PM_SLP_S3#

Q2G5
SI2307DS

PM_SUSLEDPWR

R2H2
68

PM_SUSLED

LED for S3

DS1H2
GREEN

5,6,8,9,11,15,16,18,20,21,23,26,31,33..36,39,40,42,44,48 +V3.3S

6,19,37,44 PM_SLP_S1#

Q1G2
SI2307DS

S1_LED_C

R1H2
68

S1_LED_A

LED for S1

DS1H3
GREEN

5,6,8,9,11,15,16,18,20,21,23,26,31,33..36,39,40,42,44,48 +V3.3S

R1H1
68

SO_LED_A

LED for S0

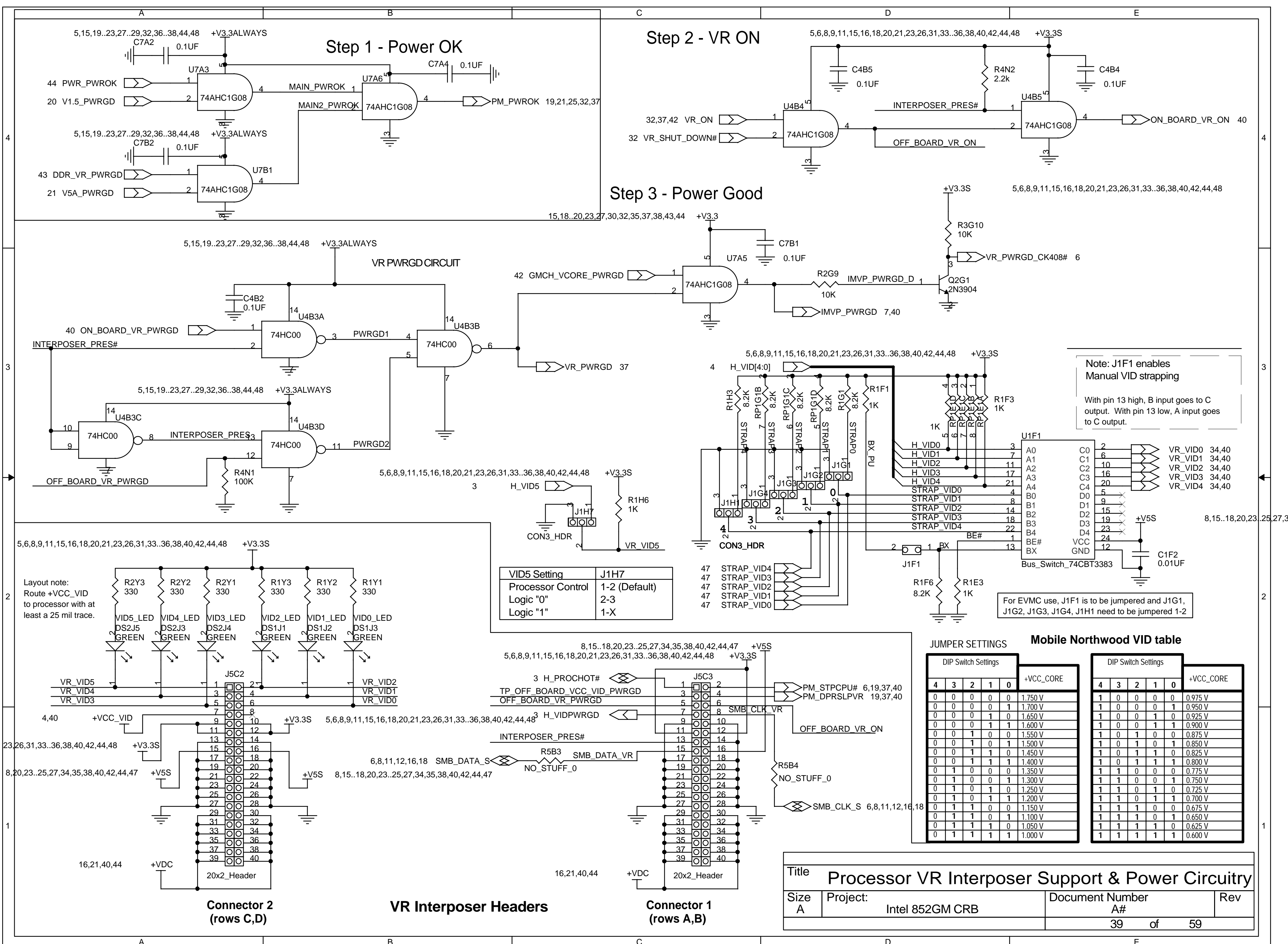
DS1H1
GREEN

SO_LED_C

6,19,37,44 PM_SLP_S1#

Q1G1
BSS138

Title	Fan Circuit, Test Capacitors and System State LEDs		
Size A	Project: Intel 852GM CRB	Document Number A#	Rev
		38 of 59	



VID5 Setting	J1H7
Processor Control	1-2 (Default)
Logic "0"	2-3
Logic "1"	1-X

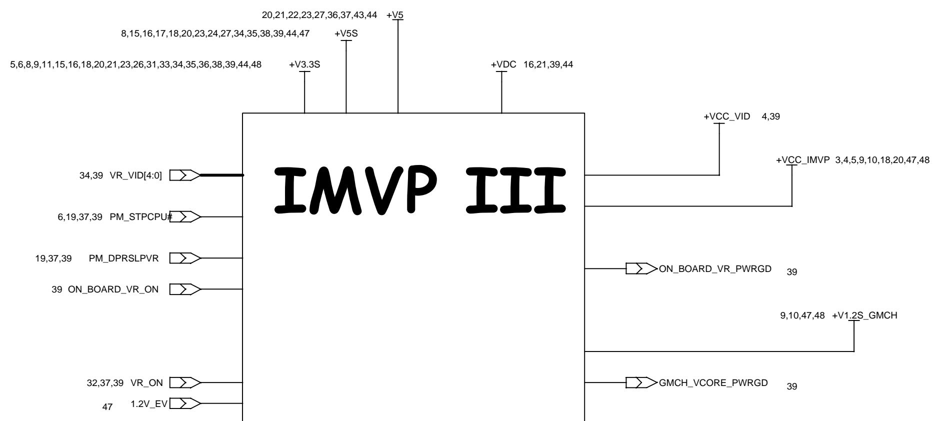
JUMPER SETTINGS

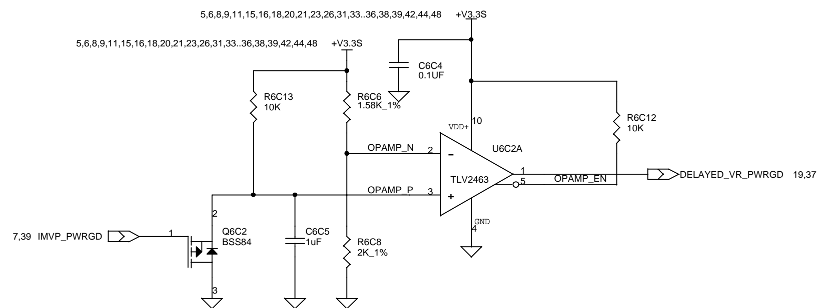
Mobile Northwood VID table

DIP Switch Settings					+VCC_CORE
4	3	2	1	0	
0	0	0	0	0	1.750 V
0	0	0	0	1	1.700 V
0	0	0	1	0	1.650 V
0	0	0	1	1	1.600 V
0	0	1	0	0	1.550 V
0	0	1	0	1	1.500 V
0	0	1	1	0	1.450 V
0	0	1	1	1	1.400 V
0	1	0	0	0	1.350 V
0	1	0	0	1	1.300 V
0	1	0	1	0	1.250 V
0	1	0	1	1	1.200 V
0	1	1	0	0	1.150 V
0	1	1	0	1	1.100 V
0	1	1	1	0	1.050 V
0	1	1	1	1	1.000 V

DIP Switch Settings					+VCC_CORE
4	3	2	1	0	
1	0	0	0	0	0.975 V
1	0	0	0	1	0.950 V
1	0	0	1	0	0.925 V
1	0	0	1	1	0.900 V
1	0	1	0	0	0.875 V
1	0	1	0	1	0.850 V
1	0	1	1	0	0.825 V
1	0	1	1	1	0.800 V
1	1	0	0	0	0.775 V
1	1	0	0	1	0.750 V
1	1	0	1	0	0.725 V
1	1	0	1	1	0.700 V
1	1	1	0	0	0.675 V
1	1	1	0	1	0.650 V
1	1	1	1	0	0.625 V
1	1	1	1	1	0.600 V

Title	Processor VR Interposer Support & Power Circuitry		
Size: A	Project: Intel 852GM CRB	Document Number: A#	Rev





Title	IMVP-III VR Controller		
Size A	Project: Intel 852GM CRB	Document Number A#	Rev
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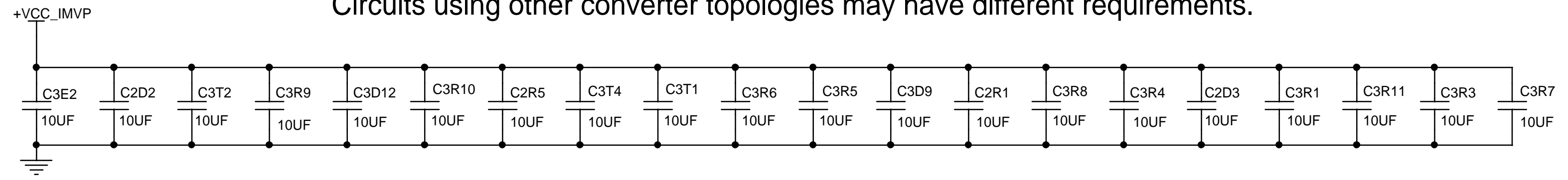
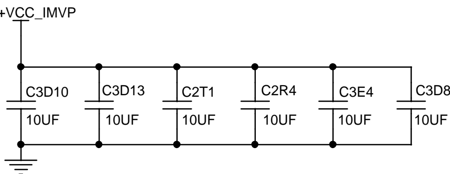
Processor Decoupling

Bulk decoupling values are tuned to Intel's IMVP III 2 phase VR design.
Circuits using other converter topologies may have different requirements.

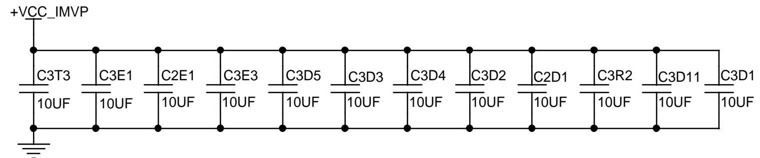
V_CORE Mid and High Frequency Decoupling



V_CORE Bulk and Mid Frequency Decoupling



V_CORE Mid and High Frequency Decoupling (under CPU)



Title	Processor Decoupling		
Size A	Project: Intel 852GM CRB	Document Number A#	Rev
		41 of 59	

BLANK

Title	Montara-GM VR and VCCP		
Size A	Project: Intel 852GM CRB	Document Number A#	Rev
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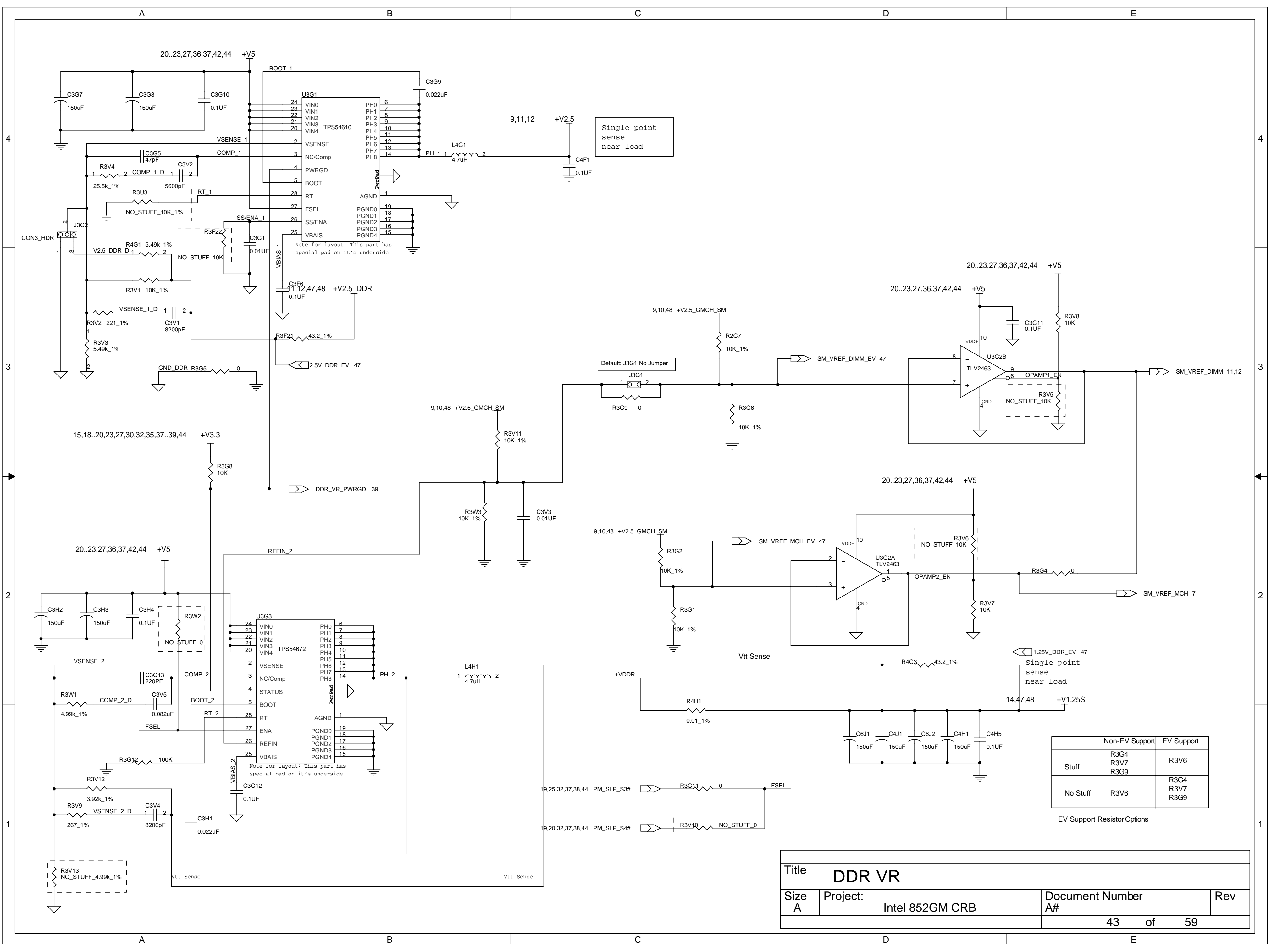

20..23,27,36,37,42,44 +V5
BOOT_1
C3G7 150uF
C3G8 150uF
C3G10 0.1UF
C3G9 0.022uF
U3G1
TPS54610
VIN0 VIN1 VIN2 VIN3 VIN4
VSENSE NC/Comp PWRGD BOOT RT FSEL SS/ENA VBAIS
PH0 PH1 PH2 PH3 PH4 PH5 PH6 PH7 PH8
AGND PGND0 PGND1 PGND2 PGND3 PGND4
PwrPad
Note for layout: This part has special pad on it's underside
VSENSE_1
COMP_1
C3G5 47pF
R3V4 25.5k_1%
COMP_1_D
C3V2 5600pF
R3U3 NO_STUFF_10K_1%
RT_1
SS/ENA_1
R3F22 NO_STUFF_10K
C3G1 0.01UF
CON3_HDR
J3G2
R4G1 5.49k_1%
V2.5_DDR_D
R3V1 10K_1%
VBIAS_1
C3F6 0.1UF
1,12,47,48 +V2.5_DDR
R3V2 221_1%
VSENSE_1_D
C3V1 8200pF
R3V3 5.49k_1%
R3F21 43.2_1%
2.5V_DDR_EV 47
GND_DDR R3G5 0
9,11,12 +V2.5
PH_1
L4G1 4.7uH
C4F1 0.1UF
Single point sense near load
15,18..20,23,27,30,32,35,37..39,44 +V3.3
R3G8 10K
DDR_VR_PWRGD 39
9,10,48 +V2.5_GMCH_SM
R3V11 10K_1%
R3W3 10K_1%
C3V3 0.01UF
Default: J3G1 No Jumper
J3G1
R3G9 0
R2G7 10K_1%
R3G6 10K_1%
SM_VREF_DIMM_EV 47
20..23,27,36,37,42,44 +V5
C3G11 0.1UF
R3V8 10K
U3G2B
TLV2463
OPAMP1_EN
R3V5 NO_STUFF_10K
SM_VREF_DIMM 11,12
REFIN_2
R3G2 10K_1%
R3G1 10K_1%
SM_VREF_MCH_EV 47
U3G2A
TLV2463
R3V6 NO_STUFF_10K
OPAMP2_EN
R3G4 0
SM_VREF_MCH 7
R3V7 10K
20..23,27,36,37,42,44 +V5
C3H2 150uF
C3H3 150uF
C3H4 0.1UF
R3W2 NO_STUFF_0
U3G3
TPS54672
VIN0 VIN1 VIN2 VIN3 VIN4
VSENSE NC/Comp STATUS BOOT RT ENA REFIN VBAIS
PH0 PH1 PH2 PH3 PH4 PH5 PH6 PH7 PH8
AGND PGND0 PGND1 PGND2 PGND3 PGND4
Note for layout: This part has special pad on it's underside
VSENSE_2
C3G13 220PF
COMP_2
R3W1 4.99k_1%
COMP_2_D
C3V5 0.082uF
BOOT_2
RT_2
FSEL
R3G12 100K
R3V12 3.92k_1%
R3V9 267_1%
VSENSE_2_D
C3V4 8200pF
VBIAS_2
C3G12 0.1UF
C3H1 0.022uF
R3V13 NO_STUFF_4.99k_1%
Vtt Sense
PH_2
L4H1 4.7uH
+VDDR
Vtt Sense
1.25V_DDR_EV 47
R4G3 43.2_1%
Single point sense near load
R4H1 0.01_1%
14,47,48 +V1.25S
C6J1 150uF
C4J1 150uF
C6J2 150uF
C4H1 150uF
C4H5 0.1UF
19,25,32,37,38,44 PM_SLP_S3#
R3G11 0
FSEL
19,20,32,37,38,44 PM_SLP_S4#
R3V10 NO_STUFF_0
Non-EV Support | EV Support
Stuff | R3G4 R3V7 R3G9 | R3V6
No Stuff | R3V6 | R3G4 R3V7 R3G9
EV Support Resistor Options
Title DDR VR
Size A
Project: Intel 852GM CRB
Document Number A#
Rev
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HDM Connector Assembly (base board)

HDM conn. is a modulized conn. design in 2 parts. 3 pin power recepticle and a 72 pin recepticle. The 2 parts will be arranged as shown on this schematic page.

Title	DC/DC Connector		
Size A	Project: Intel 852GM CRB	Document Number A#	Rev
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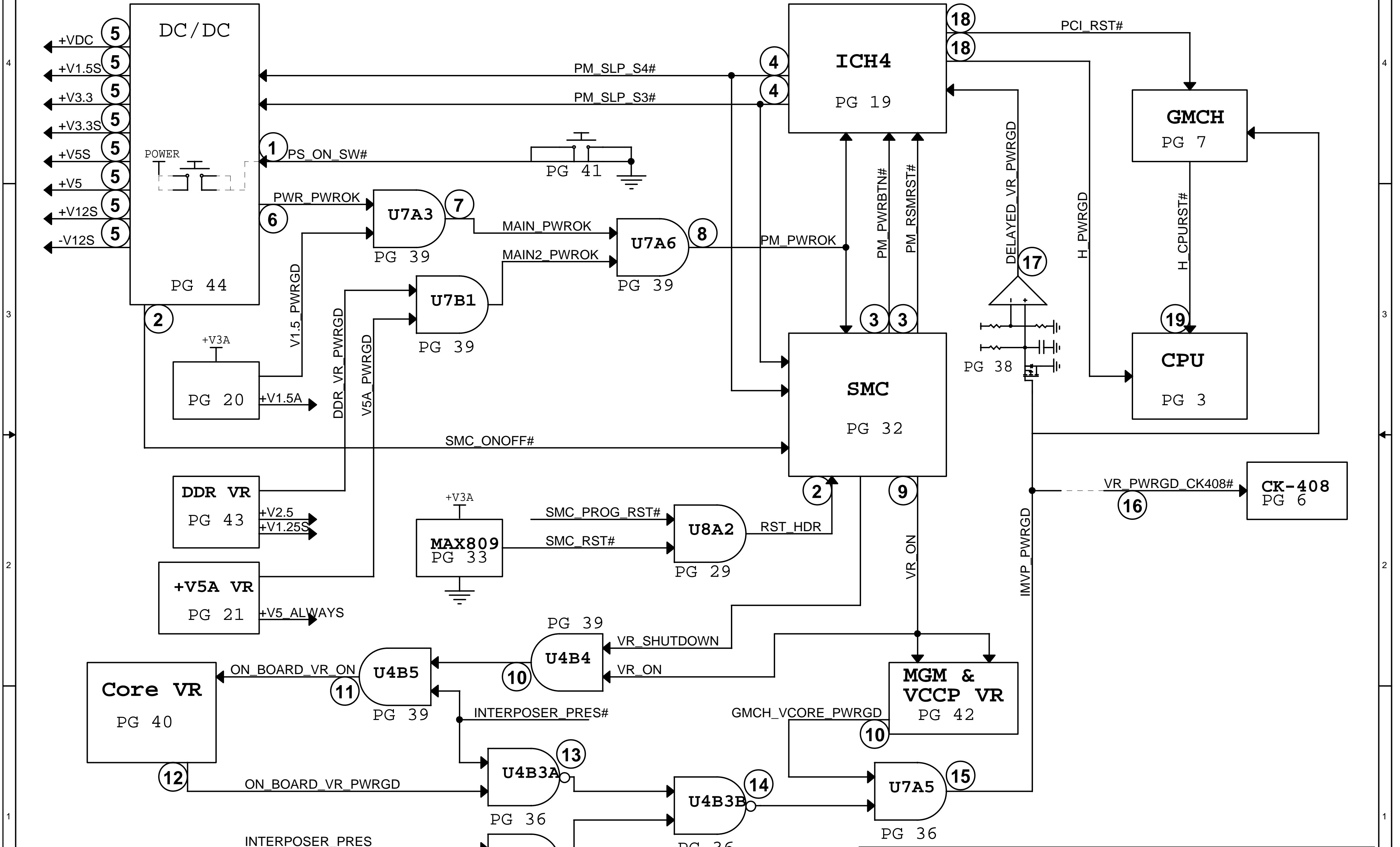
Power On Sequence



Title	Power On Check list		
Size A	Project: Intel 852GM CRB	Document Number A#	Rev
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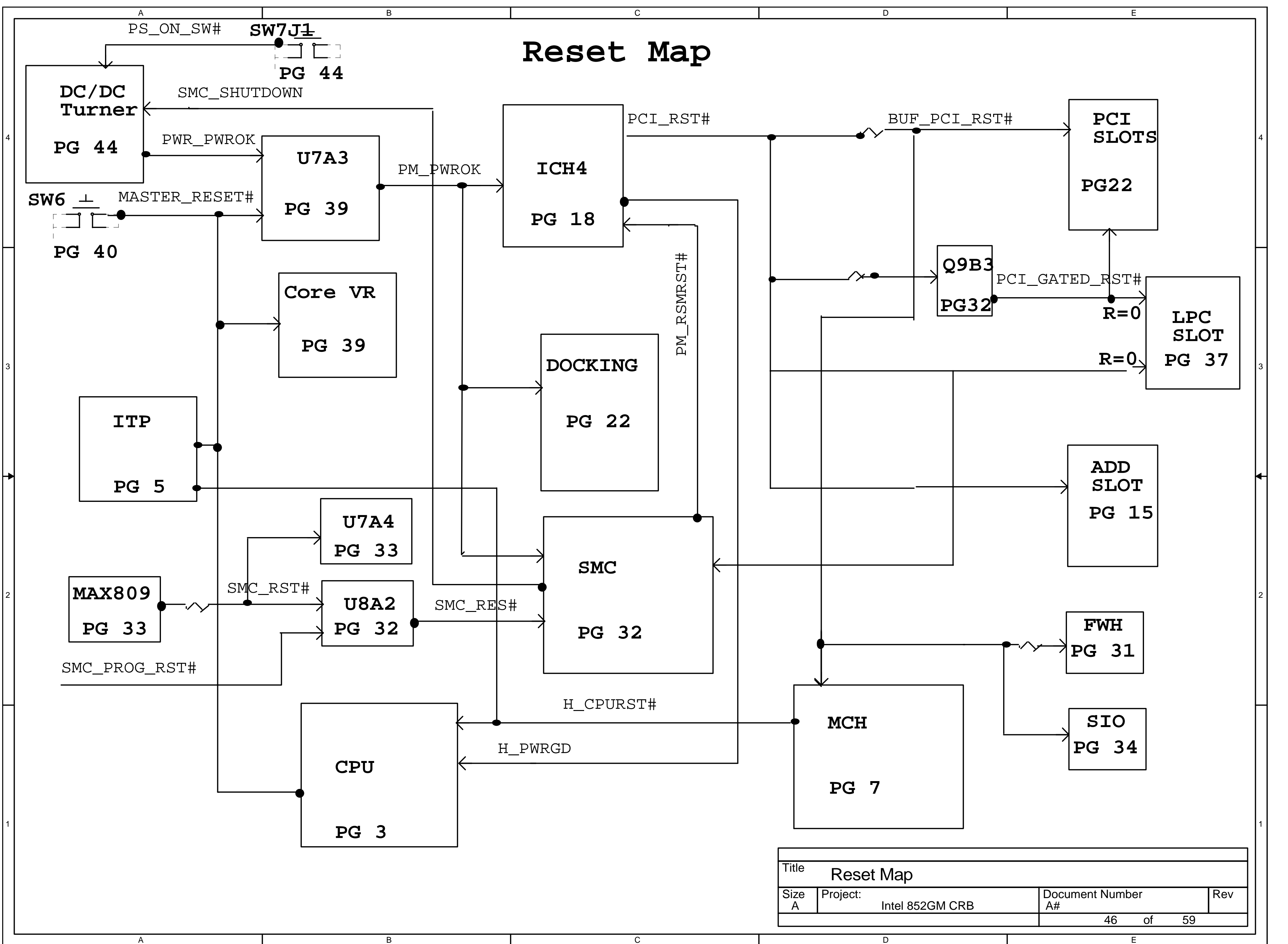
Reset Map
PS_ON_SW#
SW7J1
PG 44
DC/DC Turner
PG 44
SMC_SHUTDOWN
PWR_PWROK
U7A3
PG 39
PM_PWROK
ICH4
PG 18
PCI_RST#
BUF_PCI_RST#
PCI SLOTS
PG22
SW6
MASTER_RESET#
PG 40
Core VR
PG 39
PM_RSMRST#
Q9B3
PG32
PCI_GATED_RST#
R=0
LPC SLOT
PG 37
R=0
DOCKING
PG 22
ITP
PG 5
ADD SLOT
PG 15
U7A4
PG 33
SMC
PG 32
MAX809
PG 33
SMC_RST#
U8A2
PG 32
SMC_RES#
SMC_PROG_RST#
FWH
PG 31
SIO
PG 34
H_CPURST#
MCH
PG 7
H_PWRGD
CPU
PG 3
Title
Reset Map
Size
A
Project:
Intel 852GM CRB
Document Number
A#
Rev
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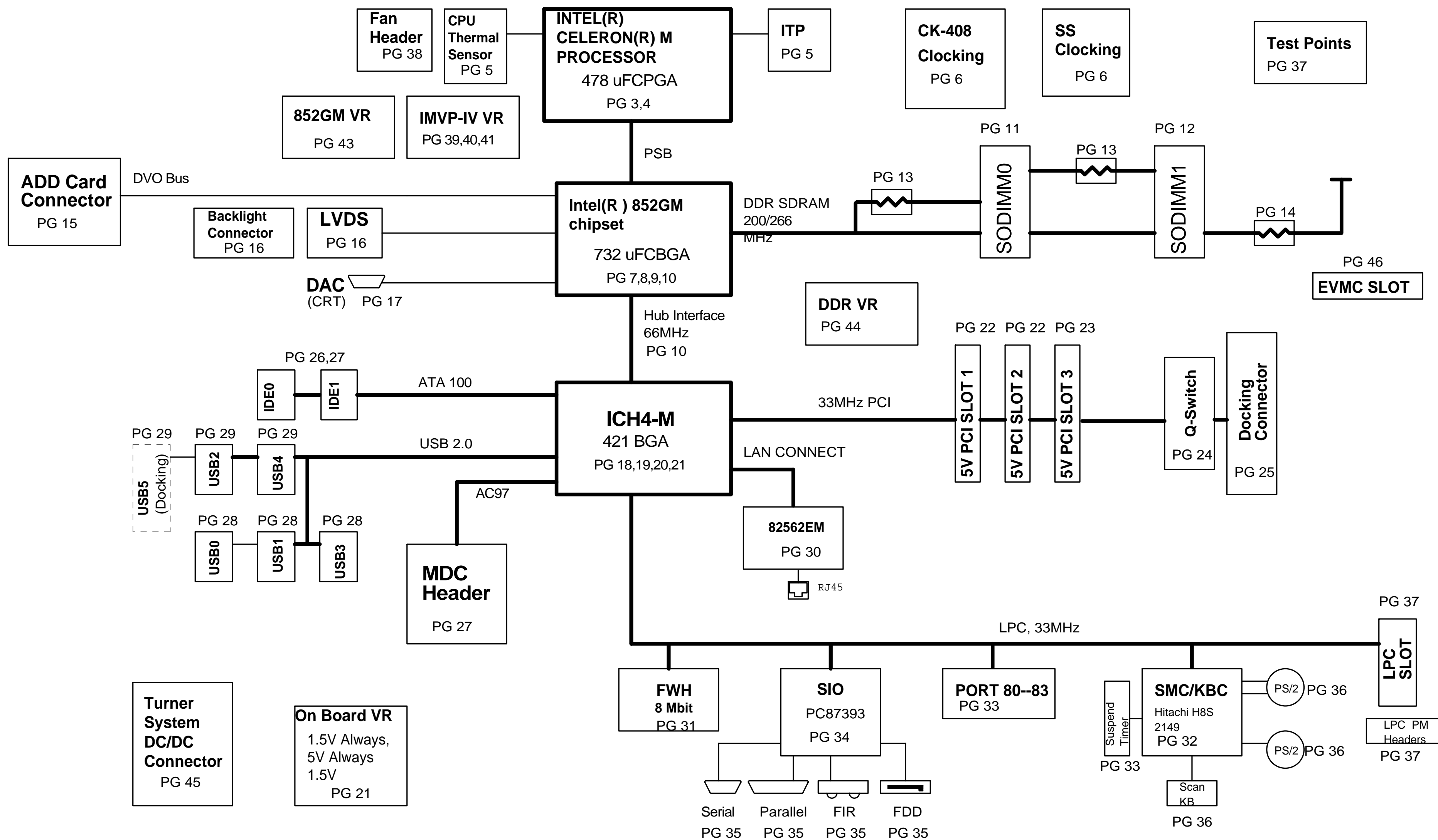
INTEL(R) CELERON(R) M PROCESSOR / INTEL(R) 852GM CHIPSET CUSTOMER REFERENCE BOARD

Fab 4

REV 4.403



Title	Block Diagram		
Size A	Project: Intel Celeron M / 852GM CRB	Document Number C26116	Rev 4.403
Date: Wednesday, January 12, 2005		Sheet 1 of 51	

CUSTOMER REFERENCE PLATFORM

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails

Rail	Description
+VDC	Primary DC system power supply (10 to 21V)
+VCC_CORE	Core voltage for processor
+VCCP	1.05V rail for processor PSB, 852GM PSB
+V1.8S	1.8V for processor PLL and VID circuitry
+V1.25S	1.25V DDR Termination voltage
+V1.35S	1.35V for 852GM core
+V1.5S	1.5V switched power rail (off in S3-S5)
+V1.5ALWAYS	1.5V always on power rail
+V1.5	1.5V power rail (off in S4-S5)
+V2.5	2.5V power rail for DDR
+V3.3ALWAYS	3.3V always on power rail
+V3.3	3.3V power rail (off in S4-S5)
+V3.3S	3.3V switched power rail (off in S3-S5)
+V5ALWAYS	5.0V for ICH4M's VCC5REFSUS
+V5	5.0V power rail (off in S4-S5)
+V5S	5.0V switched power rail (off in S3-S5)
+V12S	12.0V switched power rail (off in S3-S5)
-V12S	-12.0V switched power rail for PCI (off in S3-S5)

I^{2}C / SMB Addresses

Device	Address	Hex	Bus
Clock Generator	1101 001x	D2	SMB_ICH_S
Spread Spectrum Clock	1101 010x	D4	SMB_ICH_S
SO-DIMM0	1010 000x	A0	SMB_ICH_S
SO-DIMM1	1010 001x	A2	SMB_ICH_S
Thermal Sensor Header	1001 000x	90	SMB_ICH
LVDS Backlight Inverter	____ ____	__	SMB_ICH
Dock Connector	____ ____	__	SMB_ICH
Smart Battery	0001 011x	16	SMB_SB
Smart Battery Charger	0001 001x	12	SMB_SB
Smart Selector	0001 010x	14	SMB_SB
Bluetooth Header	____ ____	__	SMB_SB
LPC Pwr Mngmnt Header	____ ____	__	SMB_SB
LPC Pwr Mngmnt Header	____ ____	__	SMB_THRM
Thermal Diode	1001 110x	9C	SMB_THRM
EV Support:			
DV0-DV3	0101 0001	51	SMB_ICH
V5-V8	0101 0010	52	SMB_ICH
PV0-PV3	0101 0011	53	SMB_ICH
DV4	0101 0100	54	SMB_ICH
V9-V12	0101 0101	55	SMB_ICH
I1-I4	0101 0110	56	SMB_ICH
EP1-EP4	0101 0111	57	SMB_ICH
PV4	0101 0100	58	SMB_ICH
V1-V4	0101 1001	59	SMB_ICH

Default Jumper Settings

Jumper	Default	Option	Description	Page
J3F3	1-X	1-2	CPU BSEL Override	03
J7B2	1-X	1-2	GMCH Strap: PSB Voltage	08
J7B3	1-2	1-X	GMCH Strap: DVO Strap	08
J7B4	1-2	1-X	GMCH Strap: Clock Config	08
J7B5	1-2	1-X	GMCH Strap: Clock Config	08
J7C1	1-2	1-X	GMCH Strap: Clock Config	08
J6E1	2-3	1-2	LVDS EV	08
J6D1	1-X	1-2	No-Shunt Default	09
J4F1	1-X	1-2	No-Shunt Default	09
J2J3	1-X	1-2	CMOS Clear	19
J8J2	2-3	1-2	CRB/SV Detect	19
J9E2	1-2	2-3	Moon ISA Support	23
J9E4	1-2	2-3	Moon ISA Support	23
J9E5	2-3	1-2	Moon ISA Support	23
J9B1	1-X	1-2	SMC/KBC Programming	32
J8A2	1-2	2-3	SMC/KBC Disable	32
J9A1	1-X	1-2	KBC 60/64 Decode Disable	32
J9A3	1-X	1-2	SMC_LID Disable	32
J8A1	1-2	1-X	NMI Jumper	33
J9H1	1-X	1-2	Port 80-81/82-83 Select	33
J9G2	1-2	2-3	SIO Disable	34
J3G1	1-X	1-2	DDR EV Support	44
J1H4	1-X	1-2	A_FAN_P1	46
J1H5	1-X	1-2	A_FAN_P0	46
J9J2	1-X	1-2	EVMC ITP_DBRESET#	46

PCI Devices

Device	IDSEL #	REQ/GNT #		Interrupts	PC/PCI
Slot 1	AD16	1	1	F, G, H, E	A
Slot 2	AD17	2	2	G, F, E, H	A
Slot 3	AD18	3	3	C, D, B, A (E, F, G, H optional)	A
Docking	AD28	4	4	B, C, D, A	B
LAN	(AD24 internal)			A, B	

LEDs and Switches

LED	Page	Reference
Primary IDE	27	DS2J2
Secondary IDE	27	DS2J1
SMC/KBC Num Lock	32	DS8A1
SMC/KBC Scroll Lock	32	DS8A2
SMC/KBC Caps Lock	32	DS8B1
VID0	34	DS1J1
VID1	34	DS1J2
VID2	34	DS1J3
VID3	34	DS1J4
VID4	34	DS2J3
VID5	34	DS2J4
S0 State	38	DS1H1
S1 State	38	DS1H3
S3 State	38	DS1H2
S4 State	38	DS2H2
S5 State	38	DS2H1

Switch	Page	Reference
Virtual Battery On/Off	32	SW8A1
Lid	32	SW9A1
Power On/Off	45	SW8J1
Reset	45	SW7J1

Wake Events

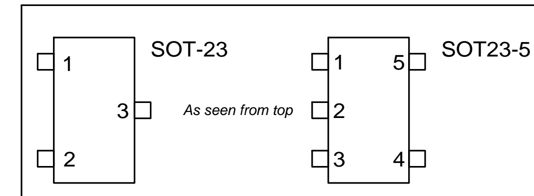
RI# (Ring Indicate) from serial port
PME# (Power Management Event) from PCI/mini-PCI slots, ADD slot, LPC slot
LAN I/O from 82562EM
LID switch attached to SMC
USB
AC97 wake on ring
SmLink for AOL II
Hot Key from the scan matrix keyboard

Net Naming Conventions

Suffix
= Active Low Signal

Prefix
H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

PCB Footprints



Power States

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALWAYS	+V*	+V*S	Clocks
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1M (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend To Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 / Soft OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Stuff / No_Stuff Resistors for Celeron M A0 / A1

Resistor	CeleronM A0	Celeron M A1 and follow-on silicon
R3T1	Stuffed	No_Stuffed
R2T3	Stuffed	No_Stuffed

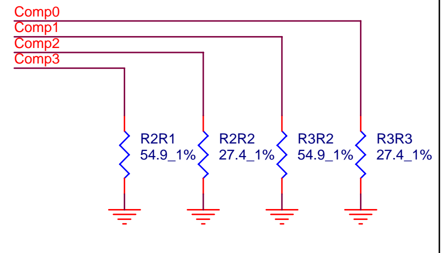
Title	Notes and Annotations		
Size: A	Project: Intel Celeron M / 852GM CRB	Document Number: C26116	Rev: 4.403
Date:	Wednesday, January 12, 2005	Sheet 2 of 51	

Place testpoint on H_IERR# with a GND 0.1" away

H_TDI pullup (R3T3) must be placed within 300ps of CPU TDI pin (within 2")

0.5" max length

Layout note:
COMP0 and COMP2 need to be Zo=27.4ohm traces. Best estimate is 18mil wide trace for outer layers and 14mil if on internal layer. See DG of Processor.Traces should be shorter than 0.5". Refer to latest CS layout COMP1, COMP3 should be routed as Zo=55ohm traces shorter than 0.5"



J3F3 should open to support Celeron M

R3T1 & R2T3 are to be stuffed for A0 silicon and no_stuffed for A1 and follow-on silicon

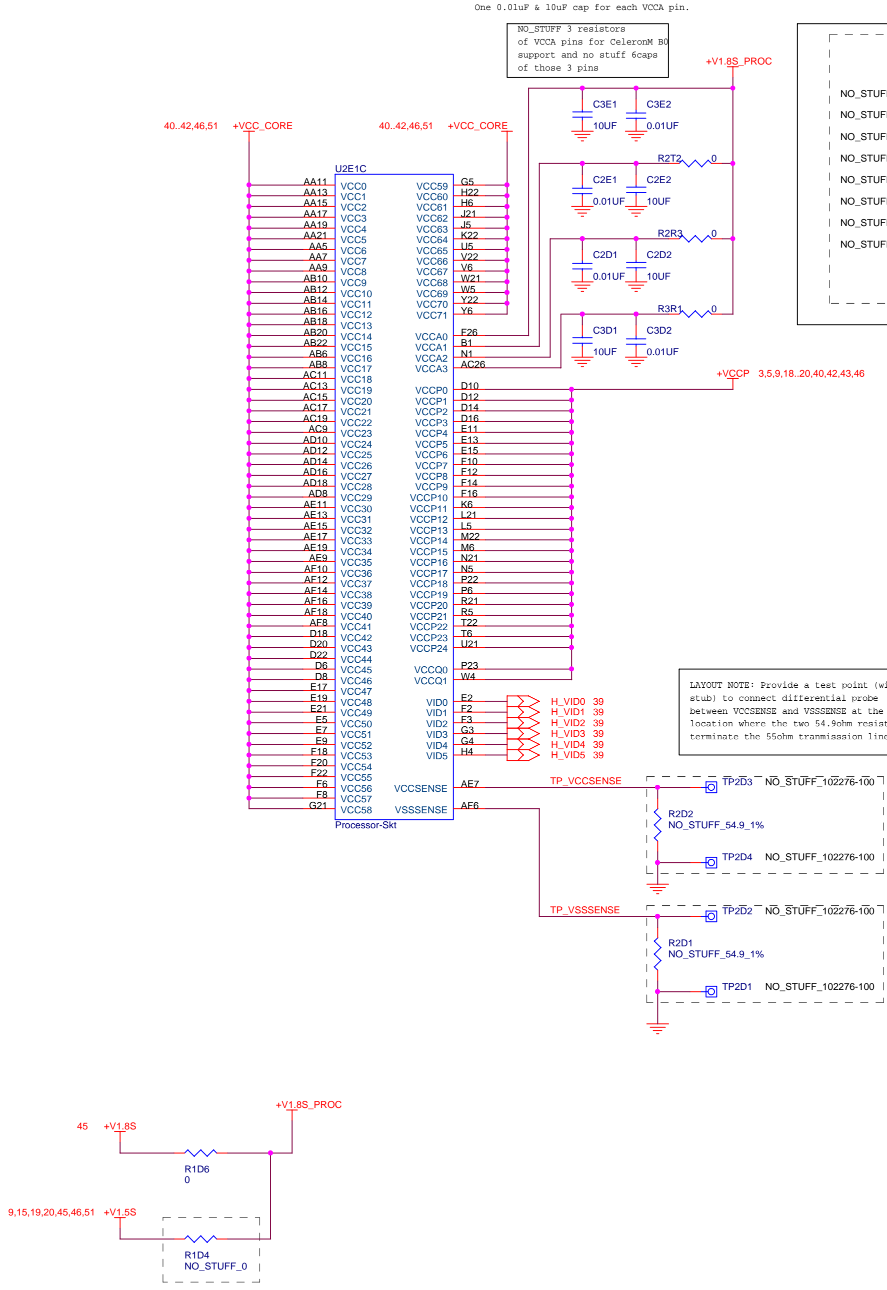
Title	Intel Celeron M Processor 1 of 2		
Size Custom	Project: Intel Celeron M / 852GM CRB	Document Number C26116	Rev 4.403
Date:	Wednesday, January 12, 2005	Sheet 3 of 51	

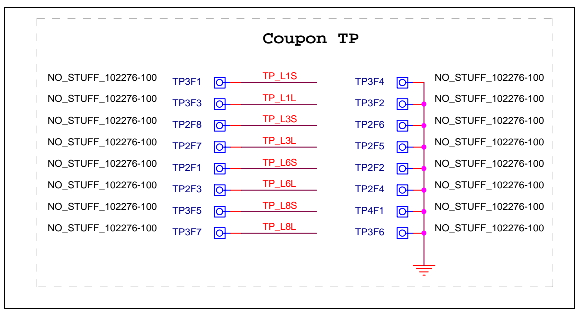
U2E1D

Processor-Skt

One 0.01uF & 10uF cap for each VCCA pin.

NO_STUFF 3 resistors of VCCA pins for CeleronM B0 support and no stuff 6caps of those 3 pins





LAYOUT NOTE: Provide a test point (with no stub) to connect differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55ohm tranmission lines.

45 +V1.8S

+V1.8S_PROC

R1D6
0

9,15,19,20,45,46,51 +V1.5S

R1D4
NO_STUFF_0

Title	Intel Celeron M Processor 2 of 2		
Size A	Project: Intel Celeron M / 852GM CRB	Document Number C26116	Rev 4.403
Date:	Wednesday, January 12, 2005	Sheet 4 of 51	

CPU Thermal Sensor

Address Select Straps
Current Address:
1001 110x

Layout Note:
Route H_THERMDA and H_THERMDC on same layer.
10 mil trace on 10 mil spacing.

Note: No Stuff for Normal Operation

Note:
If using Thermal Diode Conn, NO STUFF C372 and U14.

Layout:
Route H_TCK according to DG guidelines

Run separate H_TCK trace to processor for FBO and TCK pins on ITP.

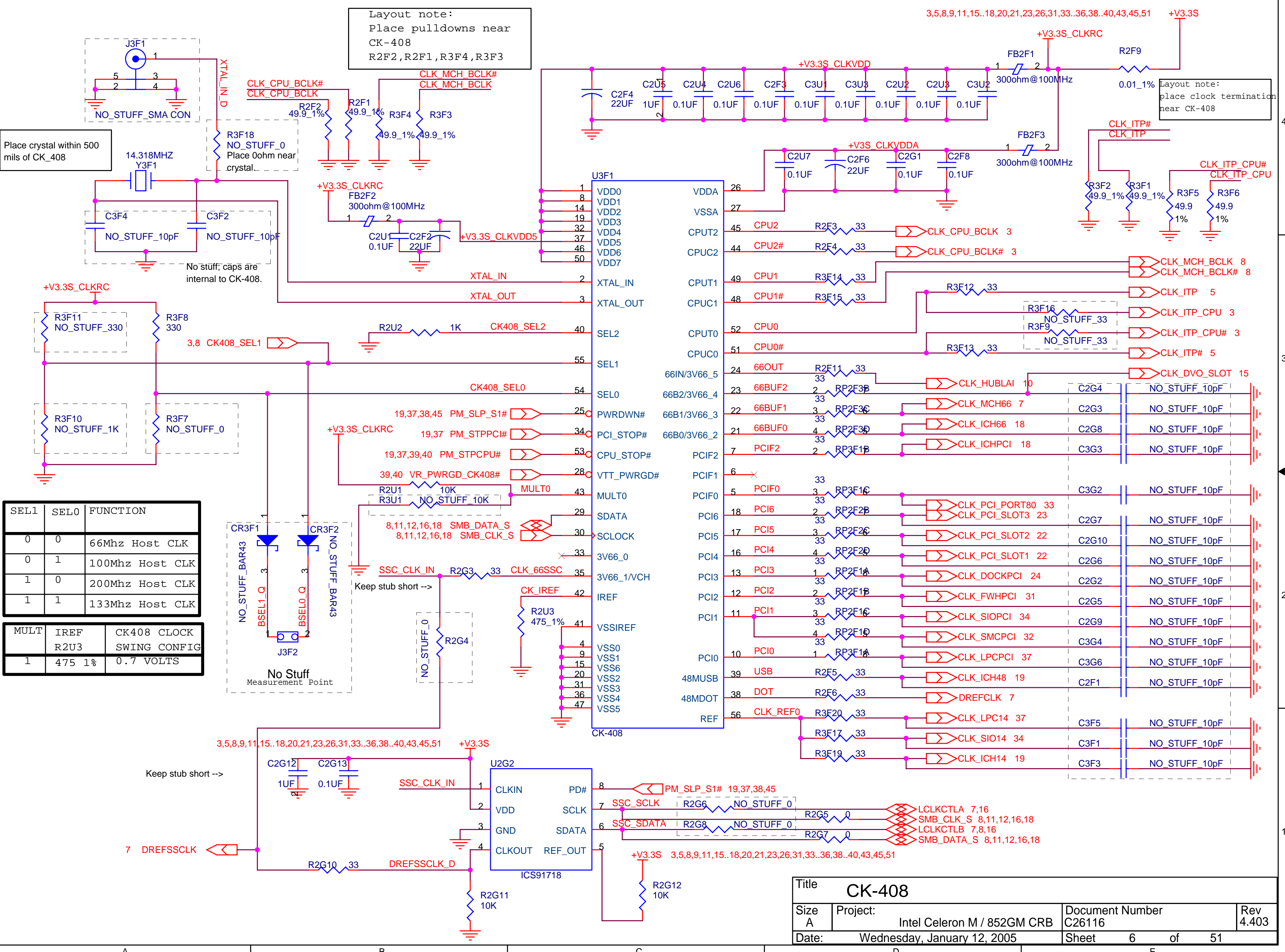
The ITP should be at the end of the H_CPURST# transmission line but less than 6.0" from the processor.

Note:
All traces between ITP Con and 0 ohm res must be short as possible

Note:
C1F2 not needed for Customer Platforms

Place TCK pulldown resistor within 1" of ITP.

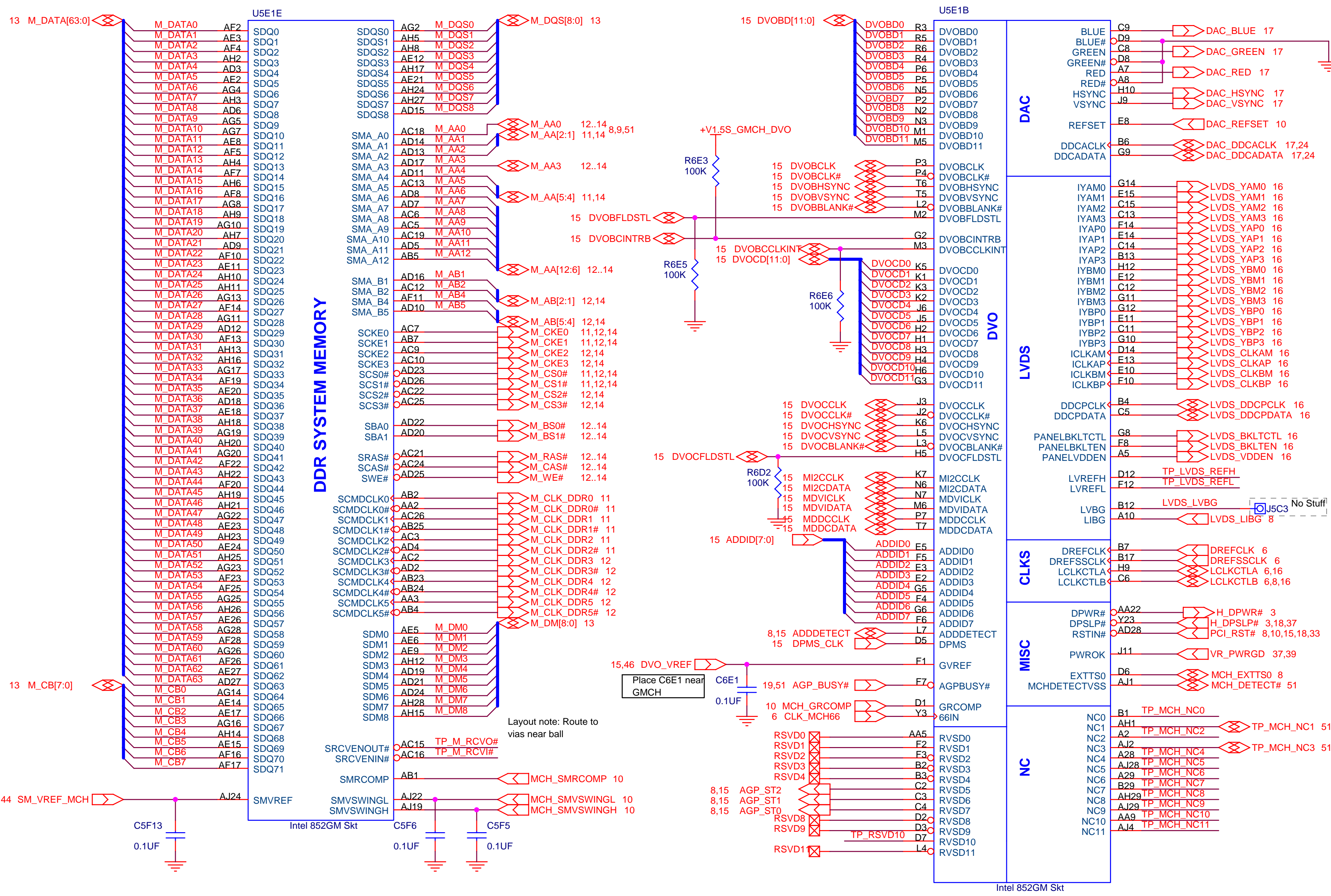
Title	CPU Thermal Sensor & ITP	
Size A	Project: Intel Celeron M / 852GM CRB	Document Number C26116 — Rev 4.403
Date: Wednesday, January 12, 2005		Sheet 5 of 51



SEL1	SEL0	FUNCTION
0	0	66Mhz Host CLK
0	1	100Mhz Host CLK
1	0	200Mhz Host CLK
1	1	133Mhz Host CLK

MULT	IREF R2U3	CK408 CLOCK SWING CONFIG
1	475 1%	0.7 VOLTS

Title	CK-408		
Size A	Project: Intel Celeron M / 852GM CRB	Document Number C26116	Rev 4.403
Date: Wednesday, January 12, 2005		Sheet 6 of 51	



Title	Intel 852GM GMCH (1 of 3)		
Size A	Project: Intel Celeron M / 852GM CRB	Document Number C26116	Rev 4.403
Date: Wednesday, January 12, 2005		Sheet 7 of 51	

External Thermal Sensor Header

3,5,6,9,11,15..18,20,21,23,26,31,33..36,38..40,43,45,51 +V3.3S

R5P12 10K

J4C1 6Pin_HDR

6,11,12,16,18 SMB_DATA_S
6,11,12,16,18 SMB_CLK_S
7 MCH_EXTTS0

U5E1A HOST

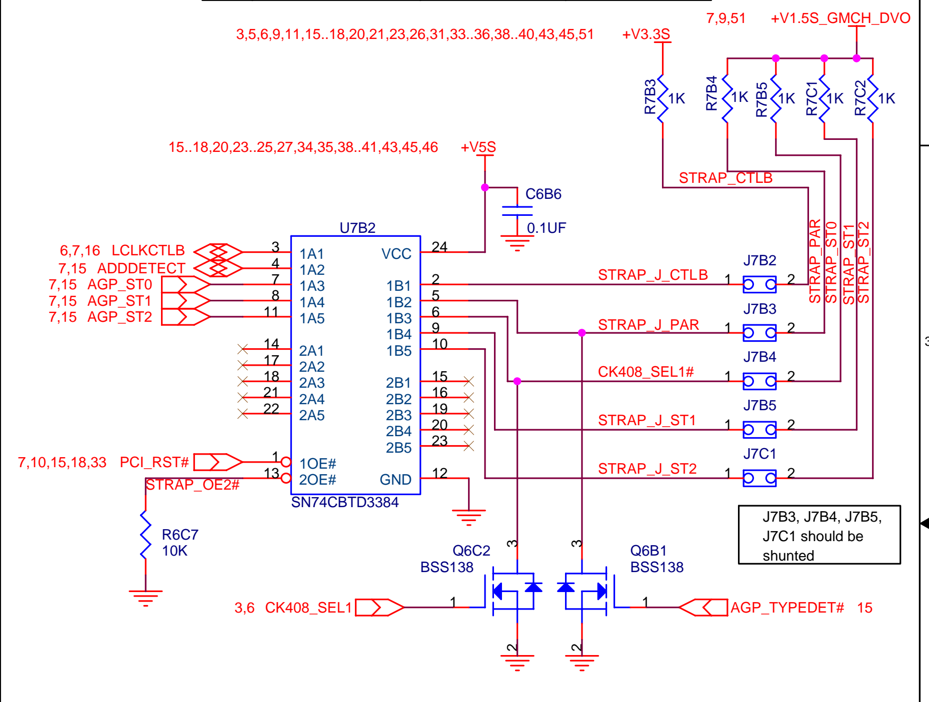
HUB I/F

Intel 852GM Skt

Layout Note:
MCH_HXSWING and MCH_HYSWING should be 10mil traces with 20mil spacing

GMCH Strapping Options

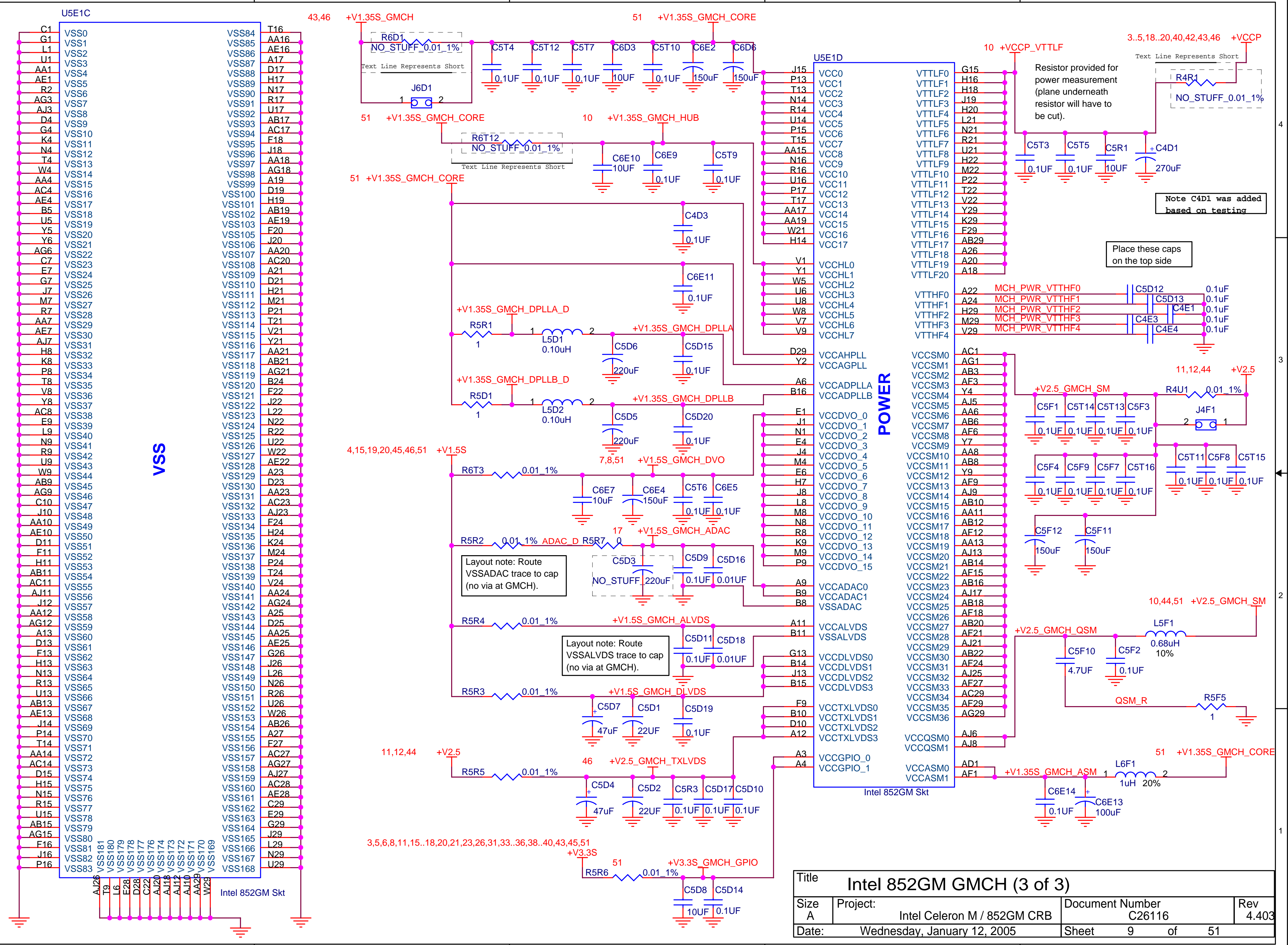
	Function	Board Default	Optional Override
J7B2	PSB Voltage Select	No JMP for 1.05V	Reserved
J7B3	DVO Strap	JMP	Reserved
J7B4	GST0	JMP	
J7B5	GST1	JMP	
J7C1	GST2	JMP	



J6E1 Default: pins 2-3. For EV work jumper pins 1-2

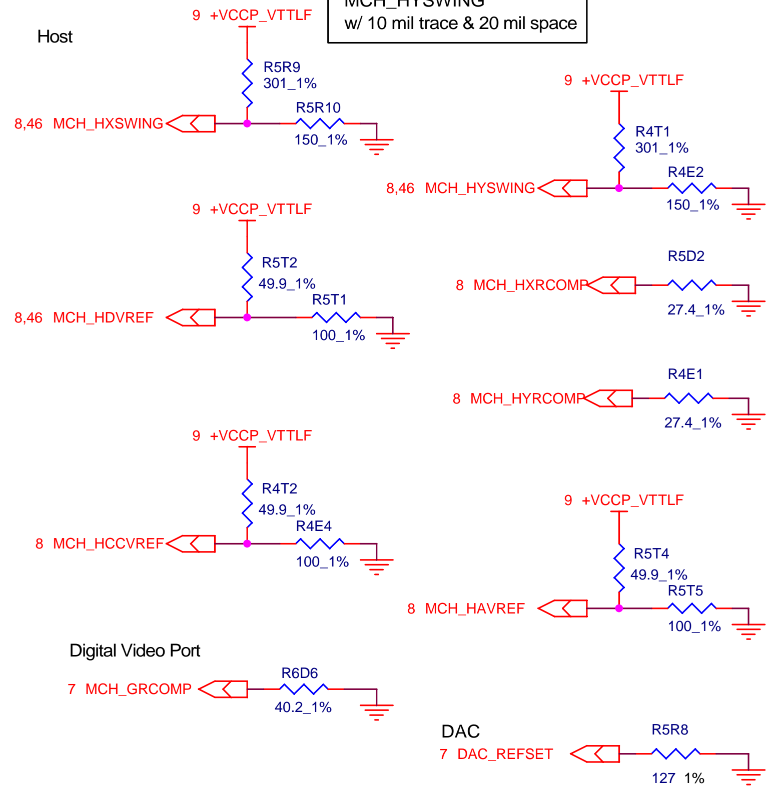
51 EPOT_VW0
J6E1
LVDS_LIBG 7
EPOT_DEFAULT R6E7 1.5K_1%

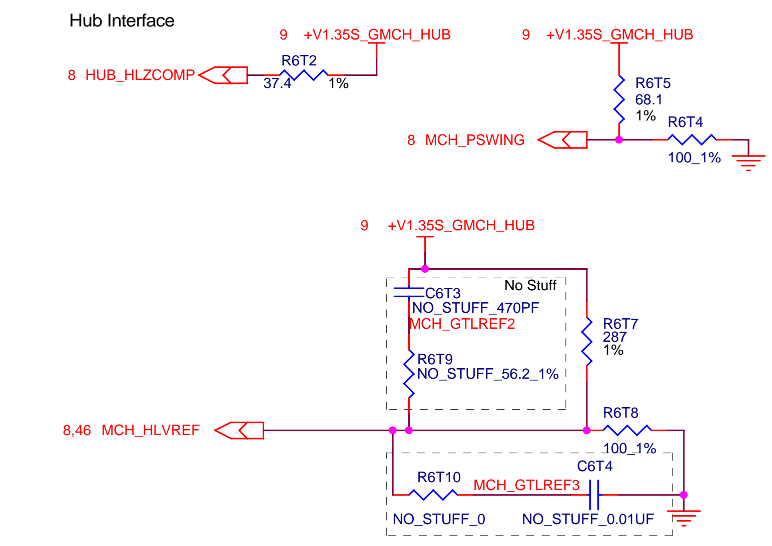
Title	Intel 852GM GMCH (2 of 3)		
Size A	Project: Intel Celeron M / 852GM CRB	Document Number C26116	Rev 4.403
Date:	Wednesday, January 12, 2005	Sheet 8 of 51	



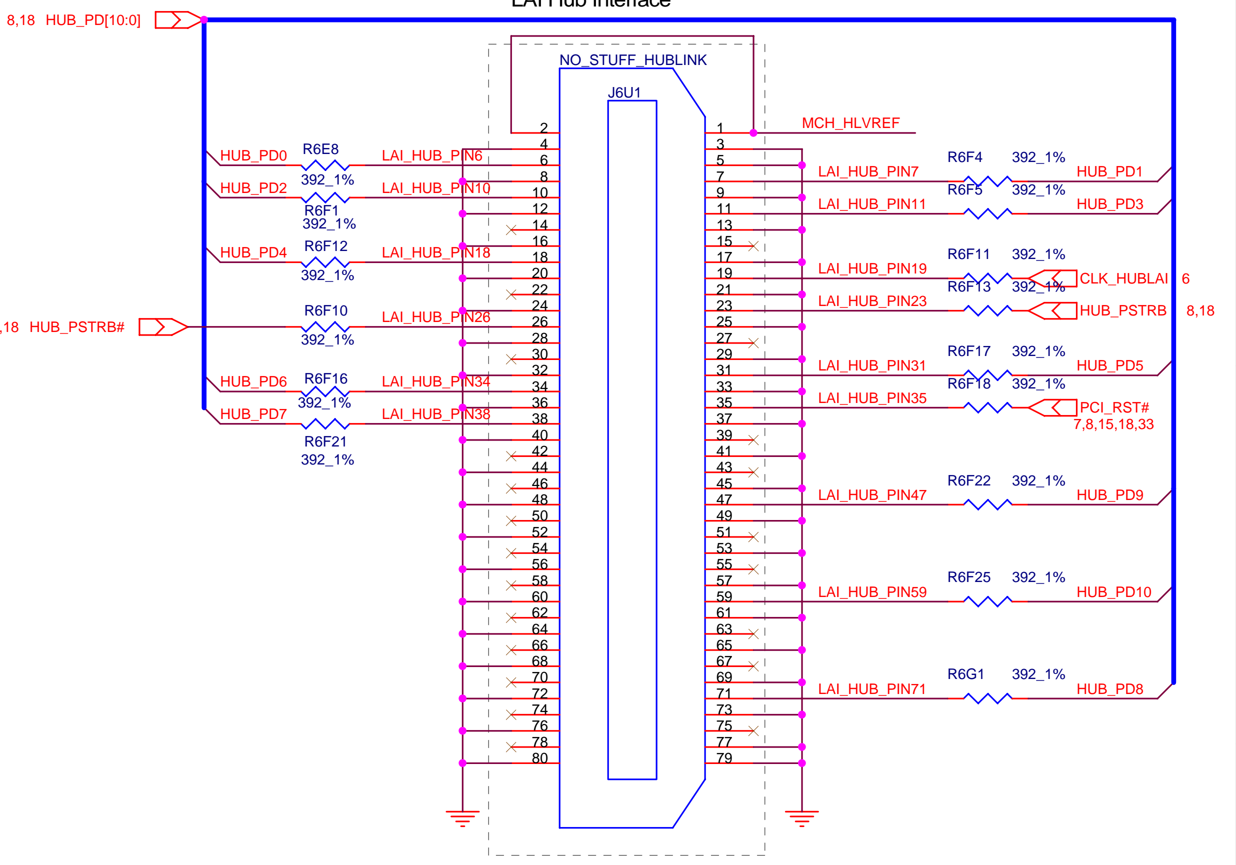
Title	Intel 852GM GMCH (3 of 3)		
Size: A	Project: Intel Celeron M / 852GM CRB	Document Number: C26116	Rev: 4.403
Date: Wednesday, January 12, 2005		Sheet 9 of 51	

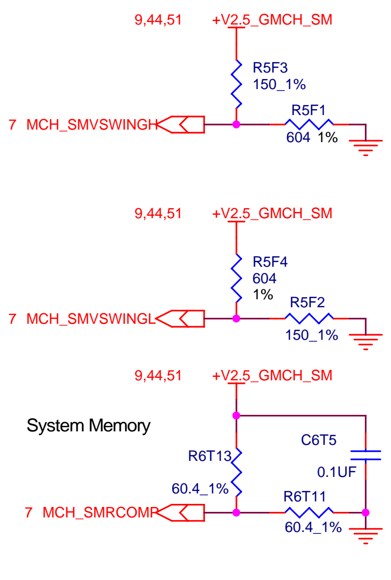
GMCH Compensation & Reference Voltages





LAI Hub Interface





Manufacturing Support

J4D1
ANCHOR_CLIP_GHOST
J6D2
ANCHOR_CLIP_GHOST
J4F2
ANCHOR_CLIP_GHOST
J6F1
ANCHOR_CLIP_GHOST

Title	Intel 852GM GMCH Circuitry		
Size A	Project: Intel Celeron M / 852GM CRB	Document Number C26116	Rev 4.403
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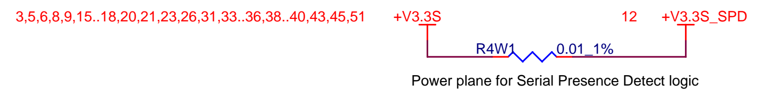
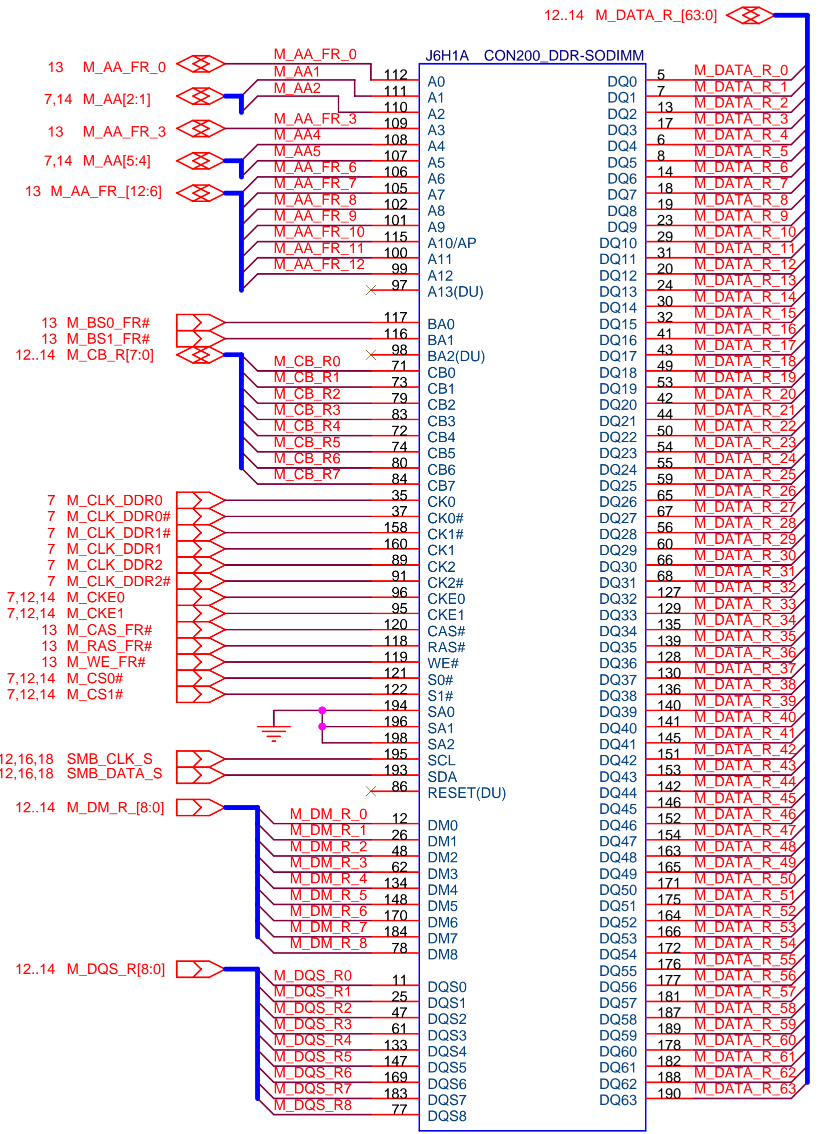
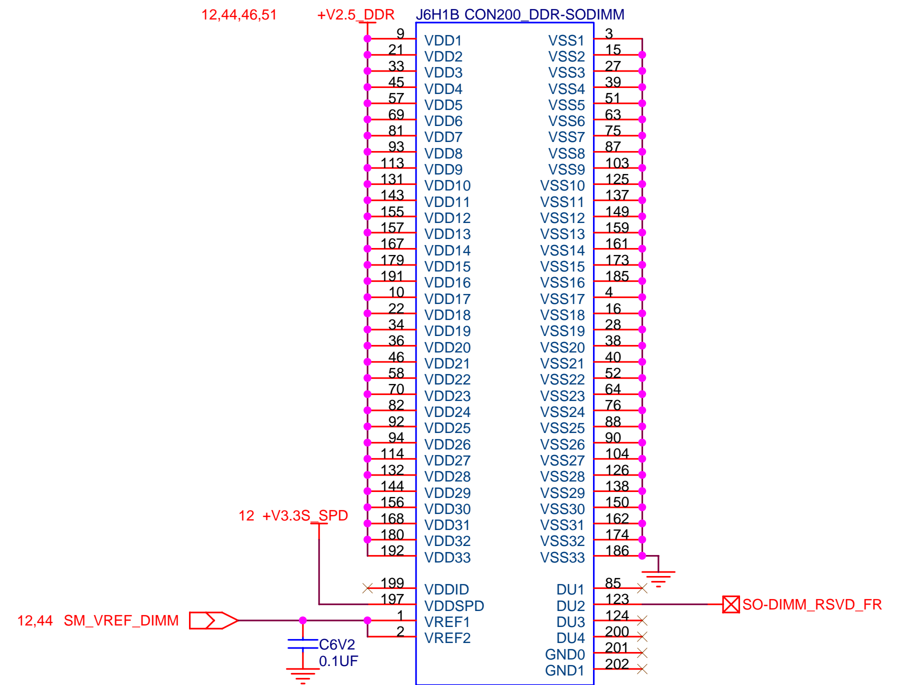
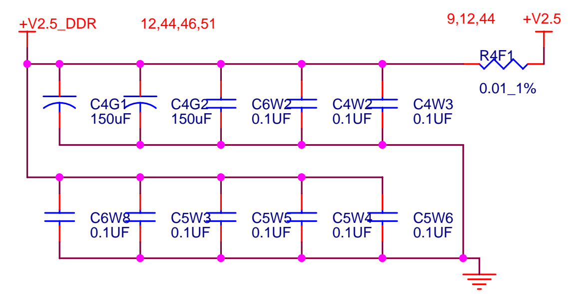




SO-DIMM 0





Layout note: Place capacitors between and near DDR connector if possible.

Title	DDR SO-DIMMs (1 of 2)		
Size A	Project: Intel Celeron M / 852GM CRB	Document Number C26116	Rev 4.403
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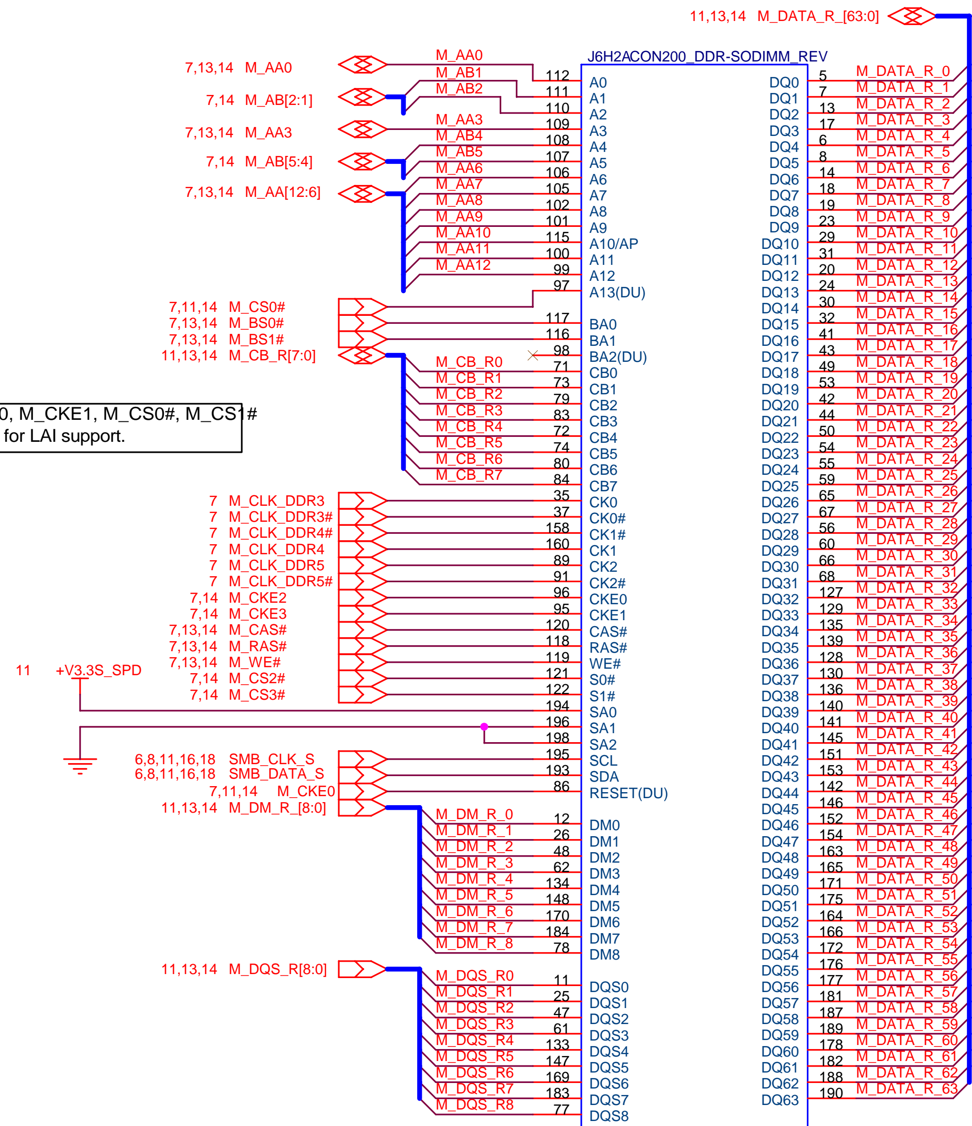
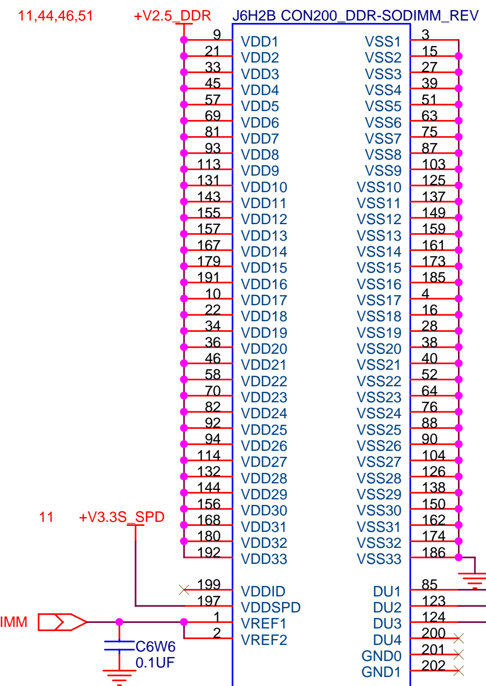
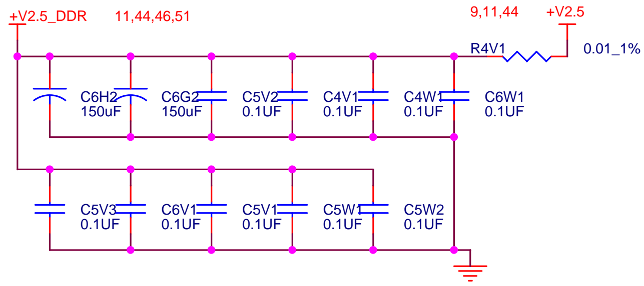


M_CKE0, M_CKE1, M_CS0#, M_CS1# are only for LAI support.





SO-DIMM 1

SO-DIMM 1 is placed farther from the GMCH than SO-DIMM 0

Layout note: Place capacitors between and near DDR connectors if possible.

Title	DDR SO-DIMMs (2 of 2)		
Size A	Project: Intel Celeron M / 852GM CRB	Document Number C26116	Rev 4.403
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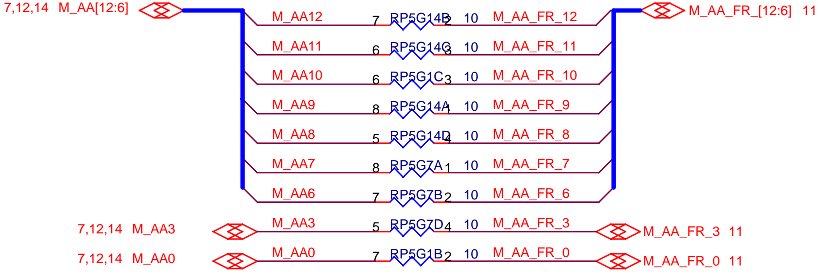
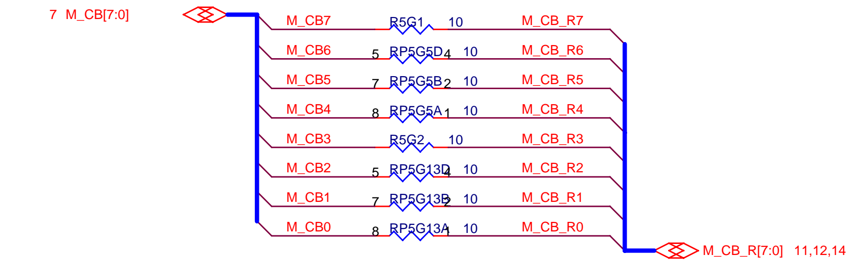
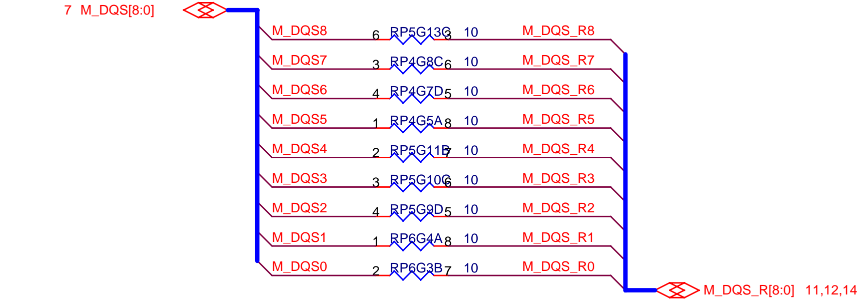
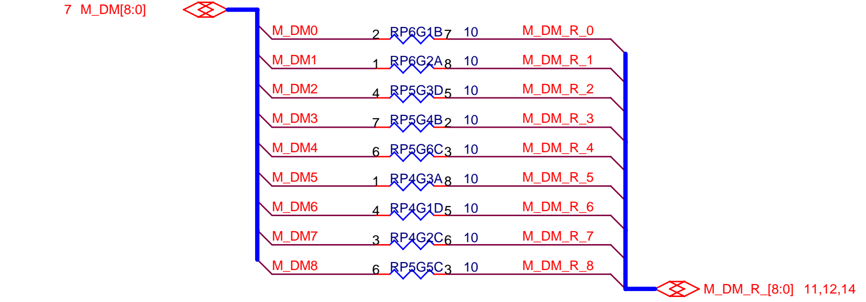
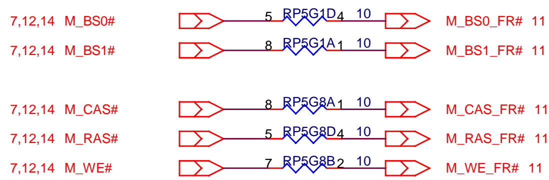


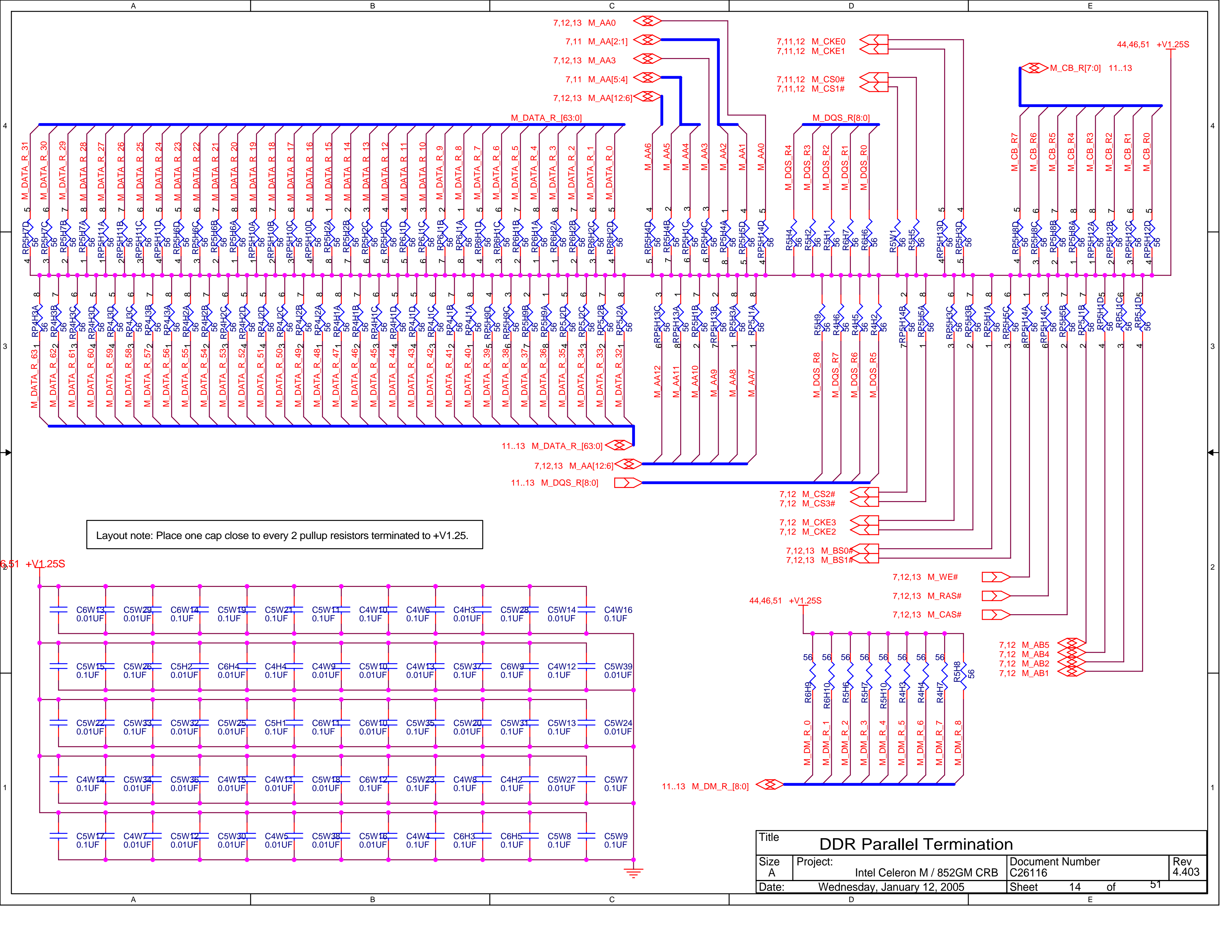








Title	DDR Series Termination		
Size: Custom	Project: Intel Celeron M / 852GM CRB	Document Number: C26116	Rev: 4.403
Date: Wednesday, January 12, 2005		Sheet 13 of 51	


7,12,13 M_AA0
7,11 M_AA[2:1]
7,12,13 M_AA3
7,11 M_AA[5:4]
7,12,13 M_AA[12:6]
7,11,12 M_CKE0
7,11,12 M_CKE1
7,11,12 M_CS0#
7,11,12 M_CS1#
44,46,51 +V1.25S
M_CB_R[7:0] 11..13
M_DATA_R_[63:0]
M_DQS_R[8:0]
11..13 M_DATA_R_[63:0]
7,12,13 M_AA[12:6]
11..13 M_DQS_R[8:0]
7,12 M_CS2#
7,12 M_CS3#
7,12 M_CKE3
7,12 M_CKE2
7,12,13 M_BS0#
7,12,13 M_BS1#
7,12,13 M_WE#
7,12,13 M_RAS#
7,12,13 M_CAS#
7,12 M_AB5
7,12 M_AB4
7,12 M_AB2
7,12 M_AB1
11..13 M_DM_R_[8:0]
Layout note: Place one cap close to every 2 pullup resistors terminated to +V1.25.
6,51 +V1.25S
Title
DDR Parallel Termination
Size A
Project: Intel Celeron M / 852GM CRB
Document Number C26116
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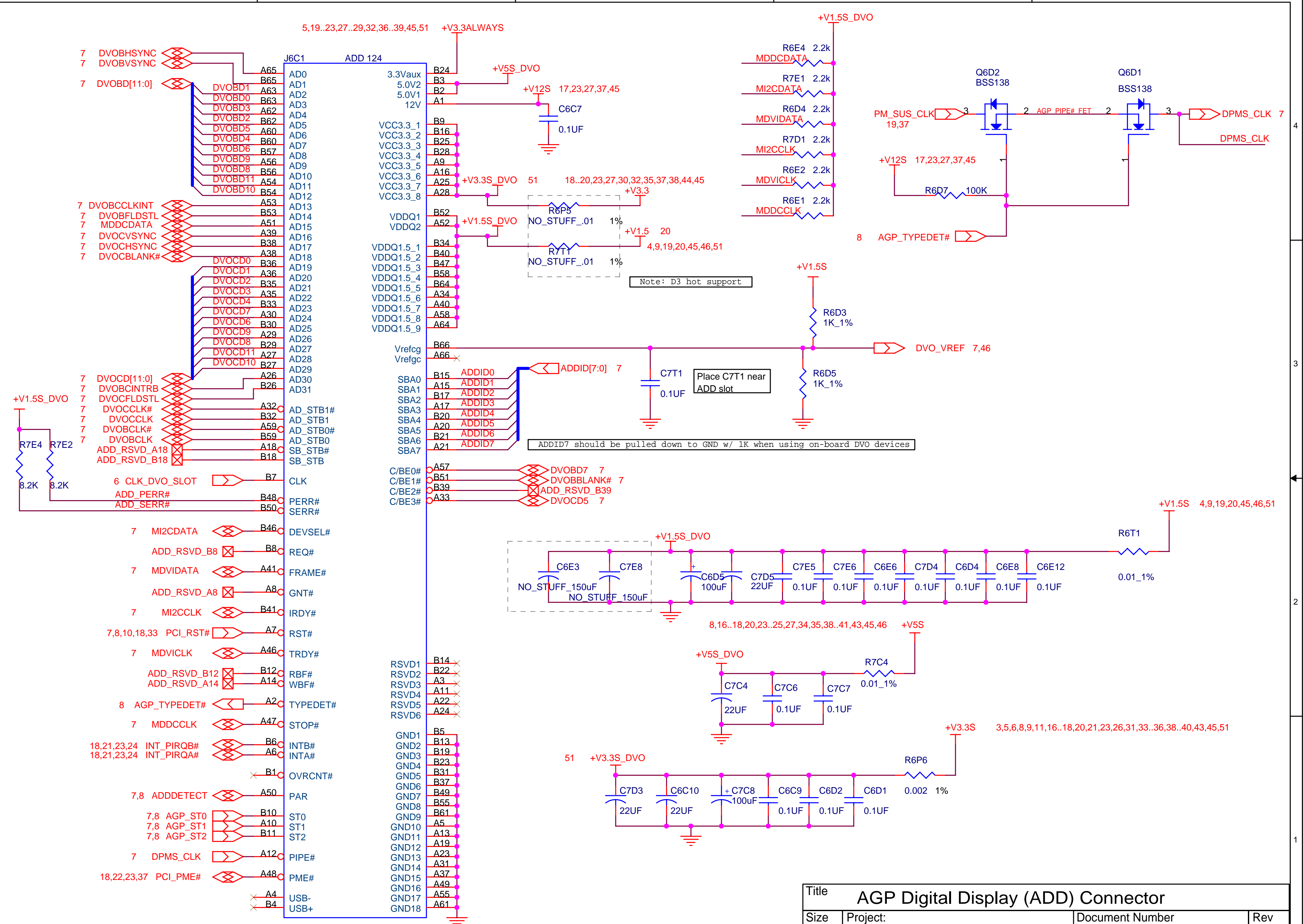


AGP Digital Display (ADD) Connector
Intel Celeron M / 852GM CRB
Document Number C26116
Rev 4.403
Wednesday, January 12, 2005
Sheet 15 of 51
J6C1 ADD 124
Note: D3 hot support
Place C7T1 near ADD slot
ADDID7 should be pulled down to GND w/ 1K when using on-board DVO devices

LVDS Interface

+V3.3S 3,5,6,8,9,11,15,17,18,20,21,23,26,31,33..36,38..40,43,45,51
+V3.3S_LVDS
R5N6 0.01_1%
Q5B2 SI2307DS
+V3.3S_LVDS_PANEL
R5N4 1M
C5N1 1000PF
C5B6 0.1UF
C5B7 22UF
R5N5 100K
LVDS_VDDEN#
LVDS_VDDEN_D#
Q5B1 BSS138
7 LVDS_VDDEN
R5N3 100K

+V3.3S 3,5,6,8,9,11,15,17,18,20,21,23,26,31,33..36,38..40,43,45,51
+V3.3S_LVDSDDC
R6N5 0.01_1%
R6N3 2.2k
R6N4 2.2k
J6B1

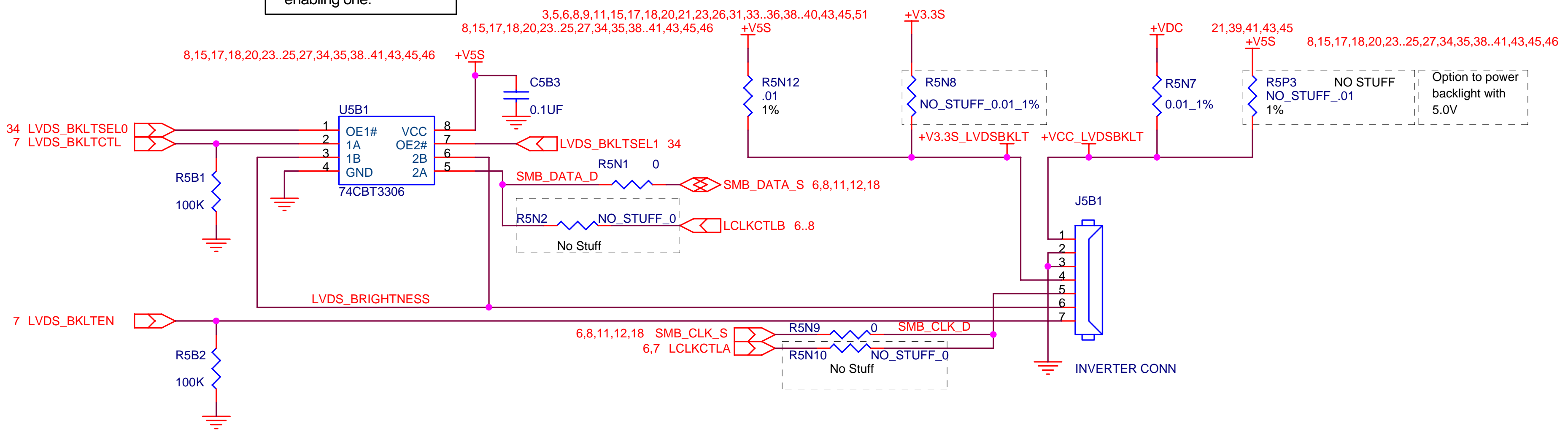
7 LVDS_DDCPCLK
7 LVDS_DDCPDATA
7 LVDS_YAM0
7 LVDS_YAP0
7 LVDS_YAM1
7 LVDS_YAP1
7 LVDS_YAM2
7 LVDS_YAP2
7 LVDS_CLKAM
7 LVDS_CLKAP
7 LVDS_YBM0
7 LVDS_YBP0
7 LVDS_YBM1
7 LVDS_YBP1
7 LVDS_YBM2
7 LVDS_YBP2
7 LVDS_CLKBM
7 LVDS_CLKBP

32 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
LVDS,CONN30

Test points for 24bpp support

7 LVDS_YAM3
7 LVDS_YAP3
R6C2 NO_STUFF_0
7 LVDS_YBM3
7 LVDS_YBP3
R6C1 NO_STUFF_0

LVDS Panel Backlight



Title	LVDS		
Size A	Project: Intel Celeron M / 852GM CRB	Document Number C26116	Rev 4.403
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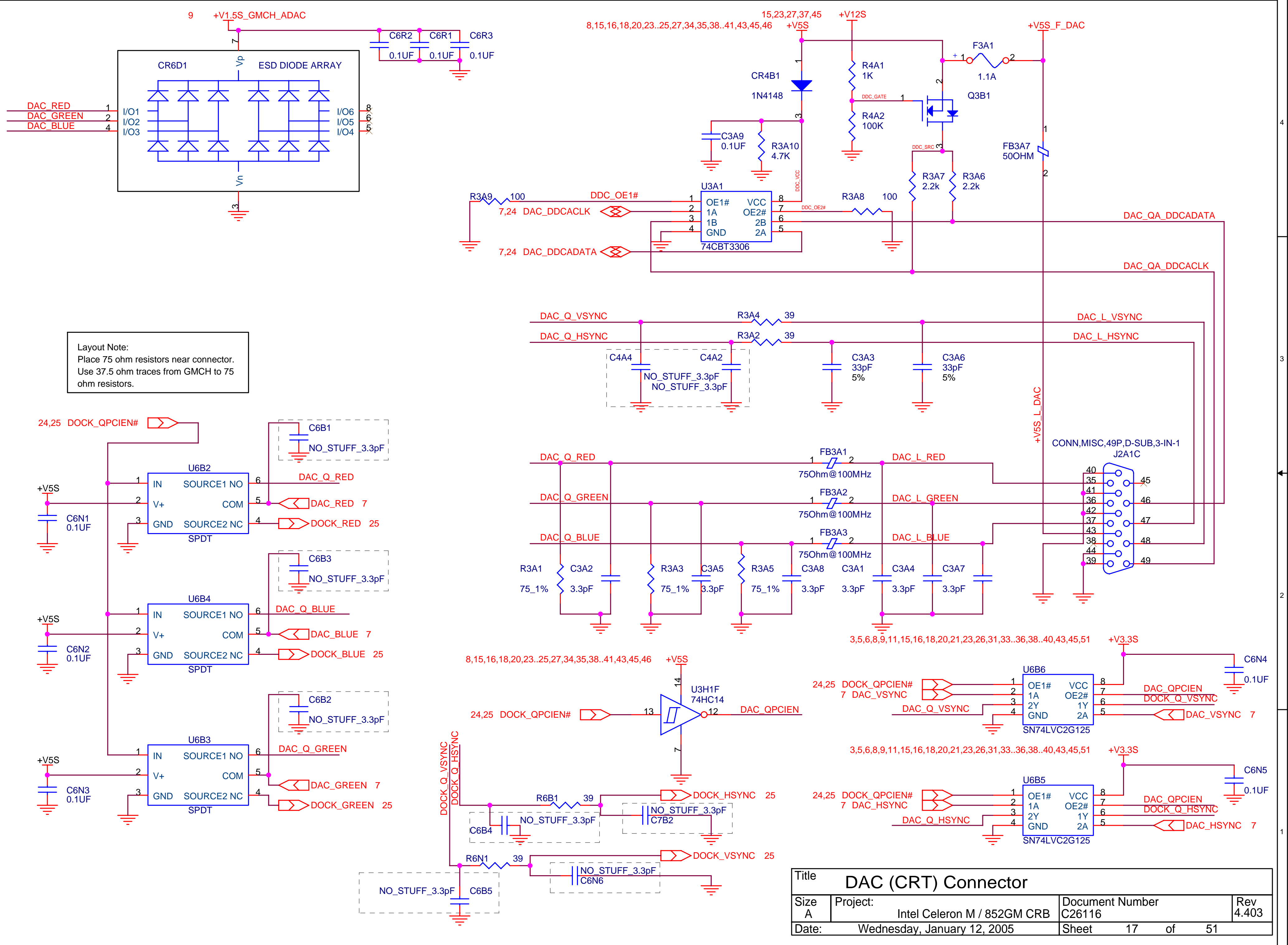

+V1.5S_GMCH_ADAC
CR6D1
ESD DIODE ARRAY
DAC_RED
DAC_GREEN
DAC_BLUE
C6R2 0.1UF
C6R1 0.1UF
C6R3 0.1UF
+V5S
+V12S
+V5S_F_DAC
CR4B1 1N4148
R4A1 1K
R4A2 100K
F3A1 1.1A
Q3B1
C3A9 0.1UF
R3A10 4.7K
FB3A7 50OHM
R3A7 2.2k
R3A6 2.2k
U3A1 74CBT3306
DDC_OE1#
DAC_DDCCLK
DAC_DDCADATA
DAC_QA_DDCADATA
DAC_QA_DDCACLK
DAC_Q_VSYNC
DAC_Q_HSYNC
DAC_L_VSYNC
DAC_L_HSYNC
Layout Note:
Place 75 ohm resistors near connector.
Use 37.5 ohm traces from GMCH to 75 ohm resistors.
DOCK_QPCIEN#
U6B2 SPDT
U6B4 SPDT
U6B3 SPDT
DAC_Q_RED
DAC_Q_GREEN
DAC_Q_BLUE
DOCK_RED
DOCK_GREEN
DOCK_BLUE
CONN,MISC,49P,D-SUB,3-IN-1
J2A1C
DAC_L_RED
DAC_L_GREEN
DAC_L_BLUE
75Ohm@100MHz
U3H1F 74HC14
DAC_QPCIEN
U6B6 SN74LVC2G125
U6B5 SN74LVC2G125
DOCK_HSYNC
DOCK_VSYNC
DOCK_Q_VSYNC
DOCK_Q_HSYNC
DAC_VSYNC
DAC_HSYNC
+V3.3S
Title
DAC (CRT) Connector
Size A
Project:
Intel Celeron M / 852GM CRB
Document Number
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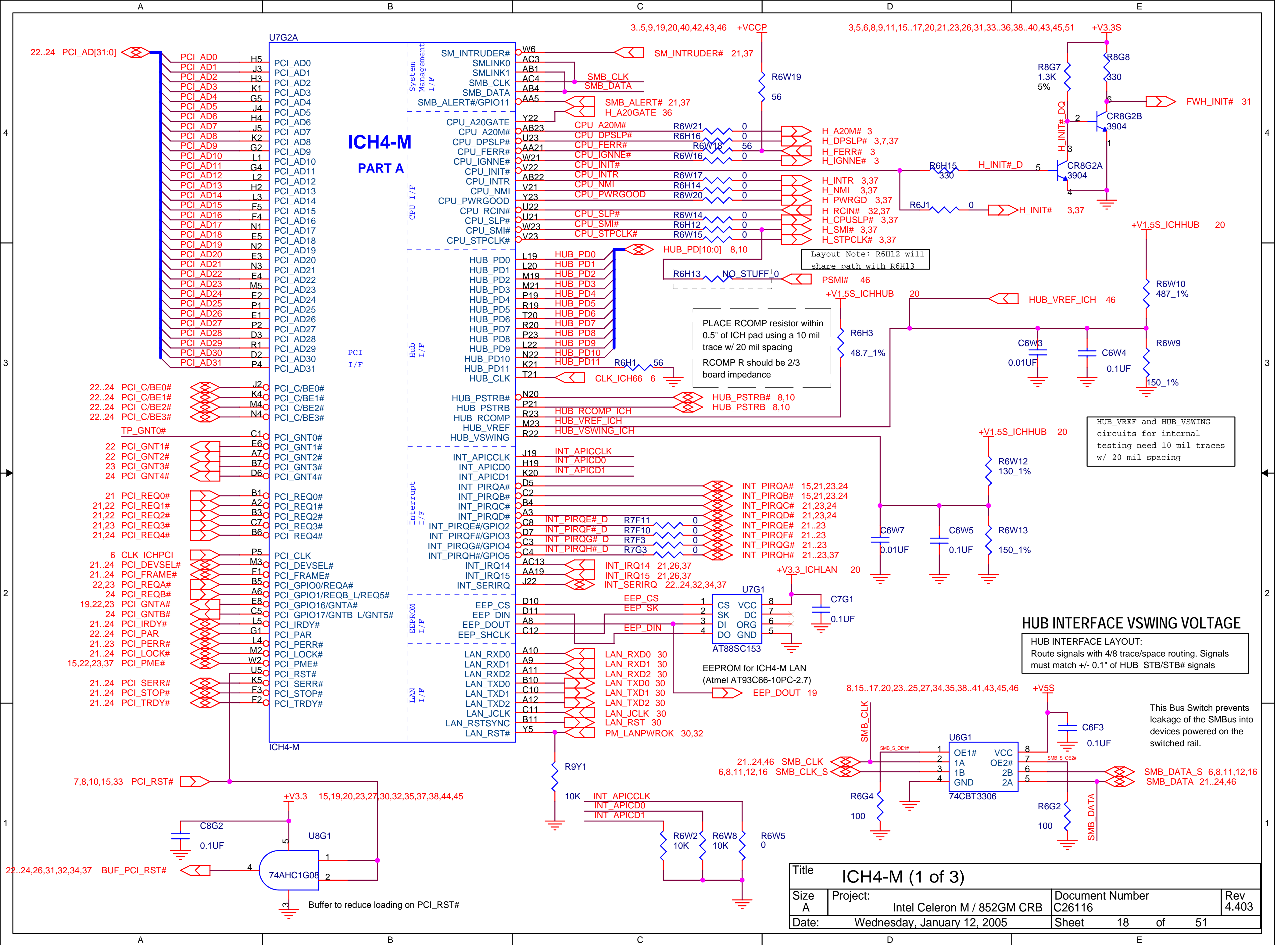

ICH4-M
PART A
U7G2A
ICH4-M
22..24 PCI_AD[31:0]
System Management I/F
SM_INTRUDER#
SMLINK0
SMLINK1
SMB_CLK
SMB_DATA
SMB_ALERT#/GPIO11
SM_INTRUDER# 21,37
SMB_ALERT# 21,37
H_A20GATE 36
CPU I/F
CPU_A20GATE
CPU_A20M#
CPU_DPSLP#
CPU_FERR#
CPU_IGNNE#
CPU_INIT#
CPU_INTR
CPU_NMI
CPU_PWRGOOD
CPU_RCIN#
CPU_SLP#
CPU_SMI#
CPU_STPCLK#
H_A20M# 3
H_DPSLP# 3,7,37
H_FERR# 3
H_IGNNE# 3
H_INTR 3,37
H_NMI 3,37
H_PWRGD 3,37
H_RCIN# 32,37
H_CPUSLP# 3,37
H_SMI# 3,37
H_STPCLK# 3,37
H_INIT# 3,37
FWH_INIT# 31
3..5,9,19,20,40,42,43,46 +VCCP
3,5,6,8,9,11,15..17,20,21,23,26,31,33..36,38..40,43,45,51 +V3.3S
Hub I/F
HUB_PD[10:0] 8,10
HUB_PSTRB# 8,10
HUB_PSTRB 8,10
HUB_RCOMP_ICH
HUB_VREF_ICH
HUB_VSWING_ICH
CLK_ICH66 6
PSMI# 46
HUB_VREF_ICH 46
+V1.5S_ICHHUB 20
Layout Note: R6H12 will share path with R6H13
NO_STUFF
PLACE RCOMP resistor within 0.5" of ICH pad using a 10 mil trace w/ 20 mil spacing
RCOMP R should be 2/3 board impedance
HUB_VREF and HUB_VSWING circuits for internal testing need 10 mil traces w/ 20 mil spacing
PCI I/F
Interrupt I/F
INT_APICCLK
INT_APICD0
INT_APICD1
INT_PIRQA# 15,21,23,24
INT_PIRQB# 15,21,23,24
INT_PIRQC# 21,23,24
INT_PIRQD# 21,23,24
INT_PIRQE# 21..23
INT_PIRQF# 21..23
INT_PIRQG# 21..23
INT_PIRQH# 21..23,37
INT_IRQ14 21,26,37
INT_IRQ15 21,26,37
INT_SERIRQ 22..24,32,34,37
EEPROM I/F
EEP_CS
EEP_SK
EEP_DIN
EEP_DOUT 19
U7G1
AT88SC153
+V3.3_ICHLAN 20
EEPROM for ICH4-M LAN (Atmel AT93C66-10PC-2.7)
LAN I/F
LAN_RXD0 30
LAN_RXD1 30
LAN_RXD2 30
LAN_TXD0 30
LAN_TXD1 30
LAN_TXD2 30
LAN_JCLK 30
LAN_RST 30
PM_LANPWROK 30,32
HUB INTERFACE VSWING VOLTAGE
HUB INTERFACE LAYOUT: Route signals with 4/8 trace/space routing. Signals must match +/- 0.1" of HUB_STB/STB# signals
8,15..17,20,23..25,27,34,35,38..41,43,45,46 +V5S
U6G1
74CBT3306
21..24,46 SMB_CLK
6,8,11,12,16 SMB_CLK_S
SMB_DATA_S 6,8,11,12,16
SMB_DATA 21..24,46
This Bus Switch prevents leakage of the SMBus into devices powered on the switched rail.
7,8,10,15,33 PCI_RST#
+V3.3 15,19,20,23,27,30,32,35,37,38,44,45
U8G1
74AHC1G08
22..24,26,31,32,34,37 BUF_PCI_RST#
Buffer to reduce loading on PCI_RST#
Title ICH4-M (1 of 3)
Size A
Project: Intel Celeron M / 852GM CRB
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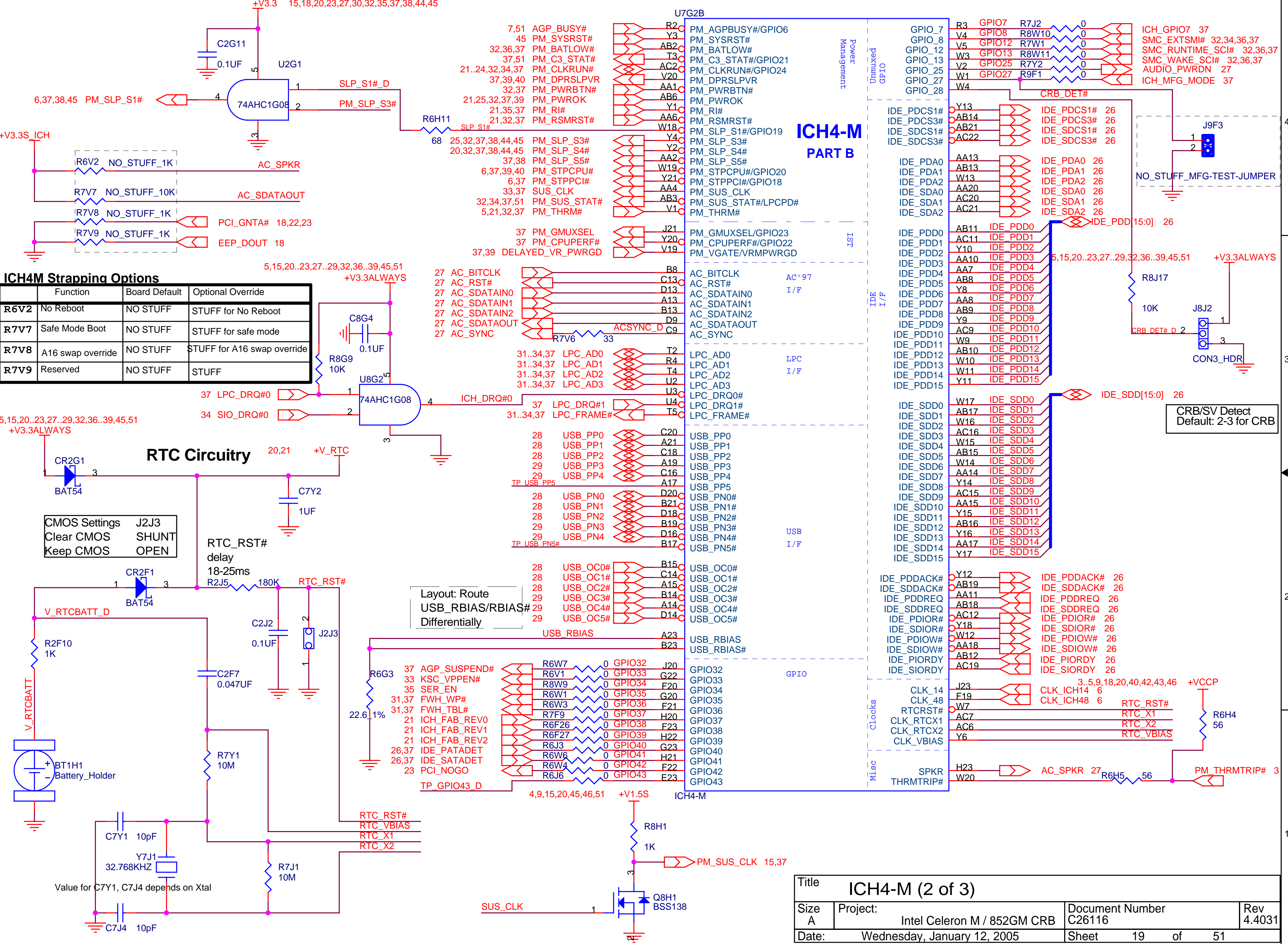


Function	Board Default	Optional Override
R6V2 No Reboot	NO STUFF	STUFF for No Reboot
R7V7 Safe Mode Boot	NO STUFF	STUFF for safe mode
R7V8 A16 swap override	NO STUFF	STUFF for A16 swap override
R7V9 Reserved	NO STUFF	STUFF

ICH4-M POWER

U7G2C ICH4-M

VCCSUS1.5_0 … VCCSUS1.5_7, VCCLAN1.5_0, VCCLAN1.5_1, VCCLAN3.3_0, VCCLAN3.3_1, VCC5REF1, VCC5REF2, VCC5REFSUS1, VCCHI_0 … VCCHI_3, VCCPLL, VCC_CPU_IO_0 … VCC_CPU_IO_2

VCC3.3_0 … VCC3.3_15, VCC1.5_0 … VCC1.5_7, VCCRTC, VCCSUS3.3_0 … VCCSUS3.3_9

+V1.5ALWAYS, +V1.5A_ICH, +V1.5_ICHLAN, +V3.3_ICHLAN, VCC5REF, +V5A_ICH, +V1.5S_ICHHUB, +VCCP, VCCPLL, +V3.3S_ICH, +V3.3S, +V1.5S_ICH, +V1.5S, +V_RTC, +V3.3ALWAYS_ICH, +V3.3ALWAYS, +V5S, +V5_ALWAYS, +V1.5, +V5

NO_STUFF_0.1UF No Stuff

Text Line Represents Short

For power measurement, cut VCCP plane & populate R6H8

NO_STUFF_0.01_1%

U8H2 MAX8888: IN, OUT, GND, POK, SHDN#

U8H3 SI3442DY

Q8J2 BSS138, Q8J3 BSS138

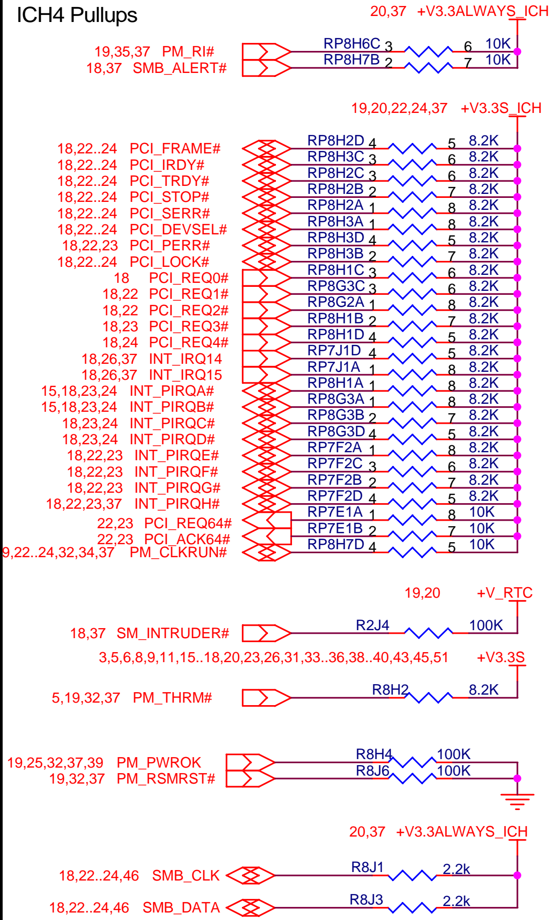
CR8J1A 3904, CR8J1B 3904, CR8G1 BAT54, CR7G2 BAT54

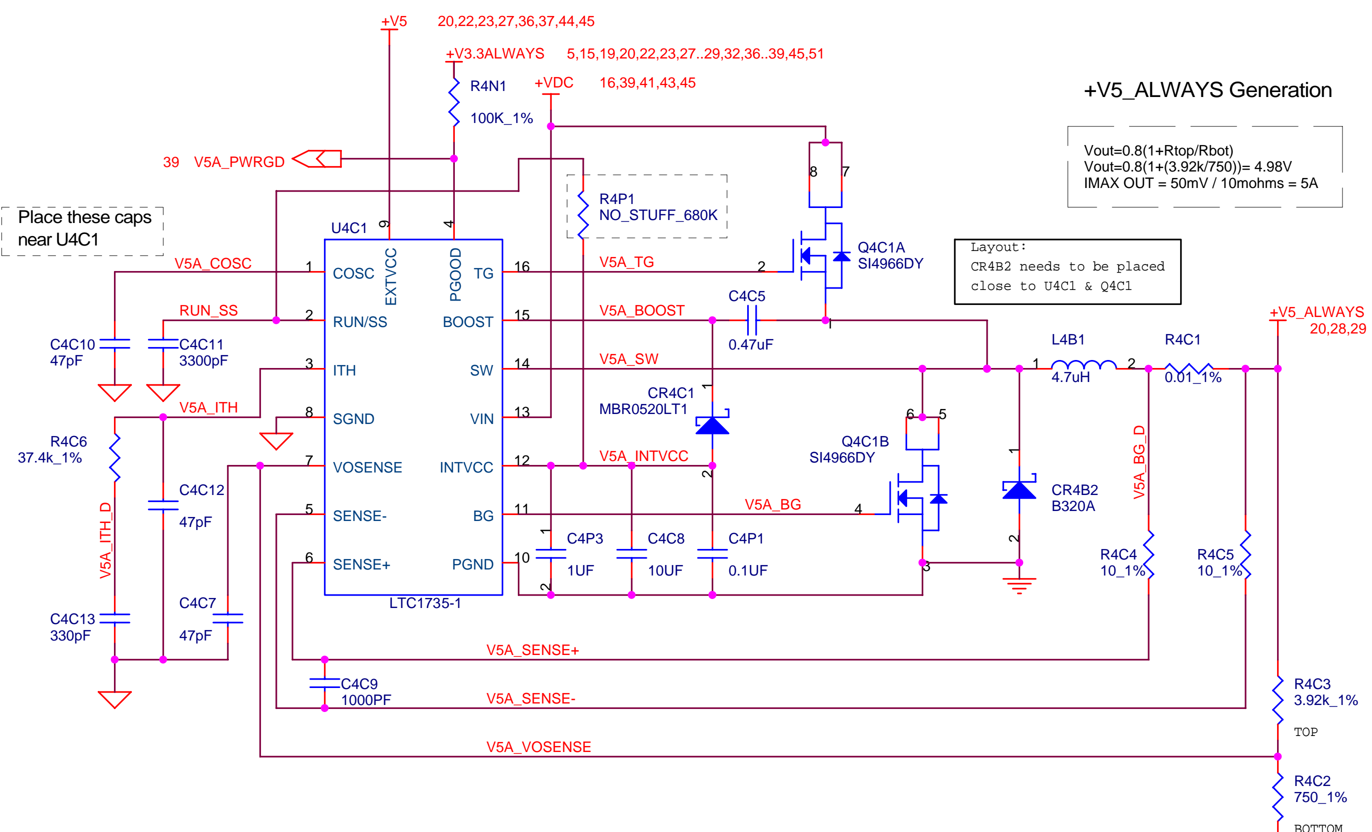
39 V1.5_PWRGD, POK_DQ, POK_D, POK, PM_SLP_S4# 19,32,37,38,44,45

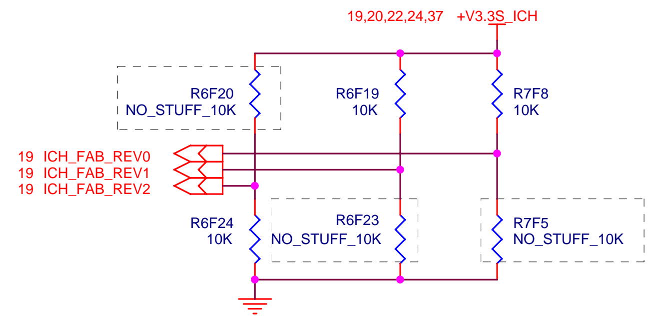
U7G2D ICH4-M

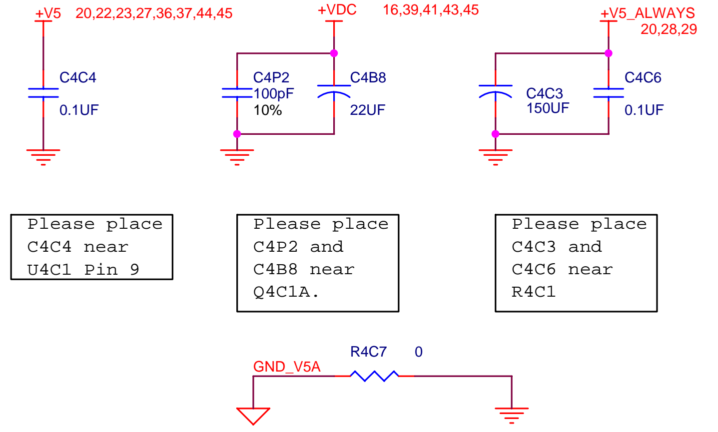
ICH4-M VSS

Title	ICH4-M (3 of 3)		
Size A	Project: Intel Celeron M / 852GM CRB	Document Number C26116	Rev 4.403
Date: Wednesday, January 12, 2005		Sheet 20 of 51	









FAB ID Strapping Table

ICH_FAB_REV 2	1	0	BOARD FAB
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

Title	ICH4-M Pullups and Testpoints		
Size A	Project: Intel Celeron M / 852GM CRB	Document Number C26116	Rev 4.403
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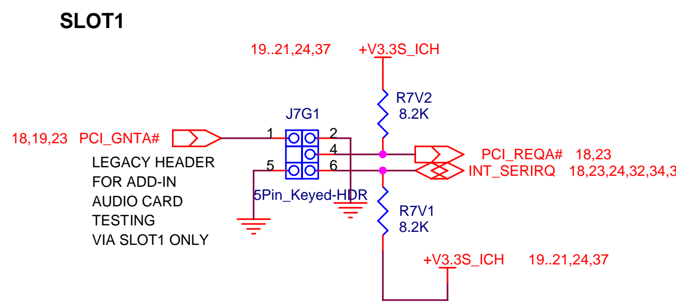
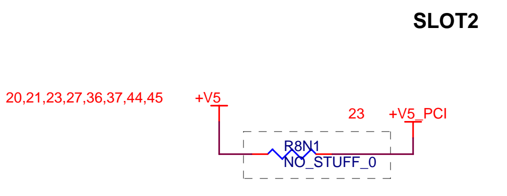
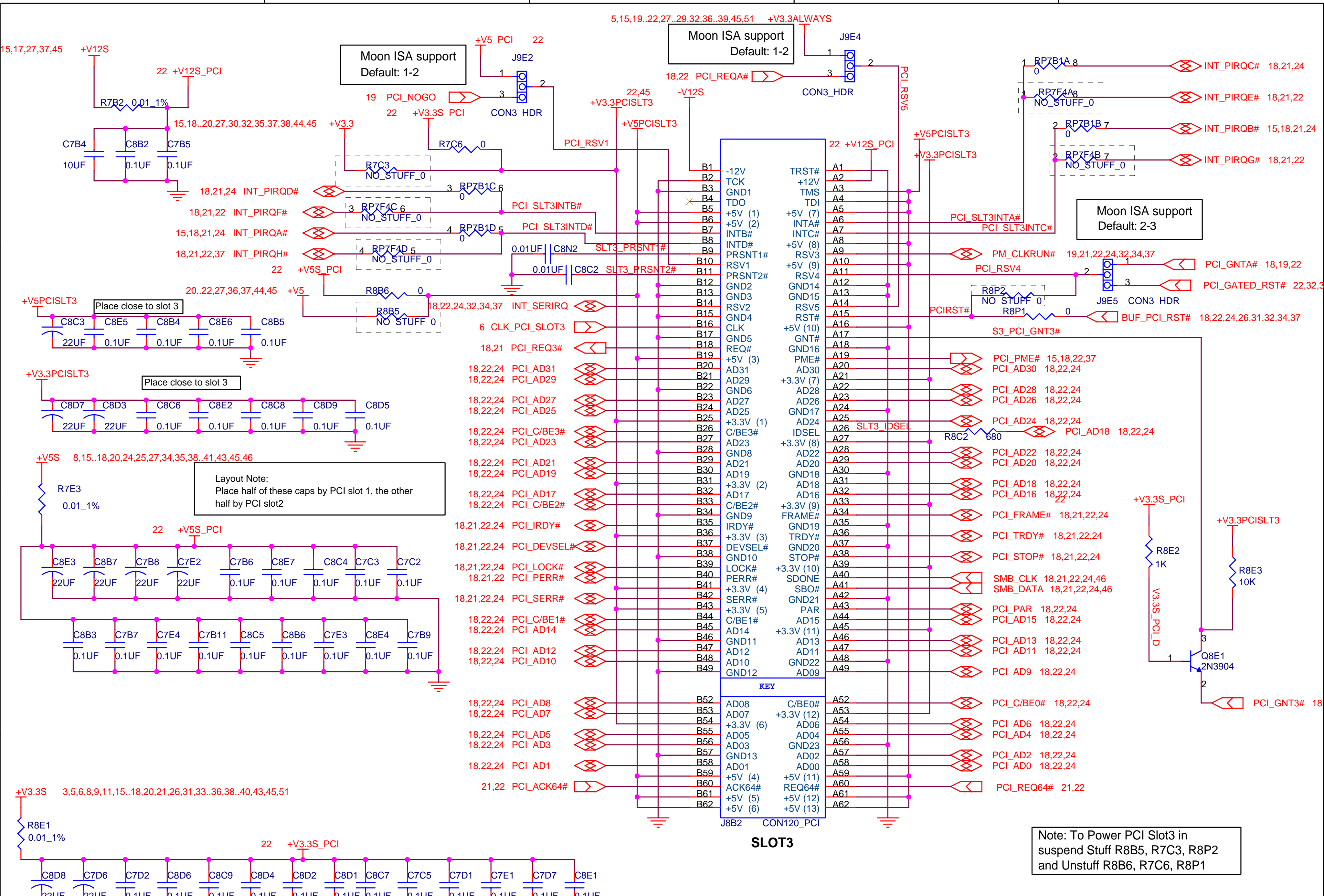
SLOT1

SLOT2





Title	PCI Slot 1 & 2		
Size A	Project: Intel Celeron M / 852GM CRB	Document Number C26116	Rev 4.403
Date: Wednesday, January 12, 2005		Sheet 22 of 51	



PCI Slot3 is farthest from processor

Title	PCI Slot 3/Moon-ISA support & Decoupling		
Size A	Project: Intel Celeron M / 852GM CRB	Document Number C26116	Rev 4.403
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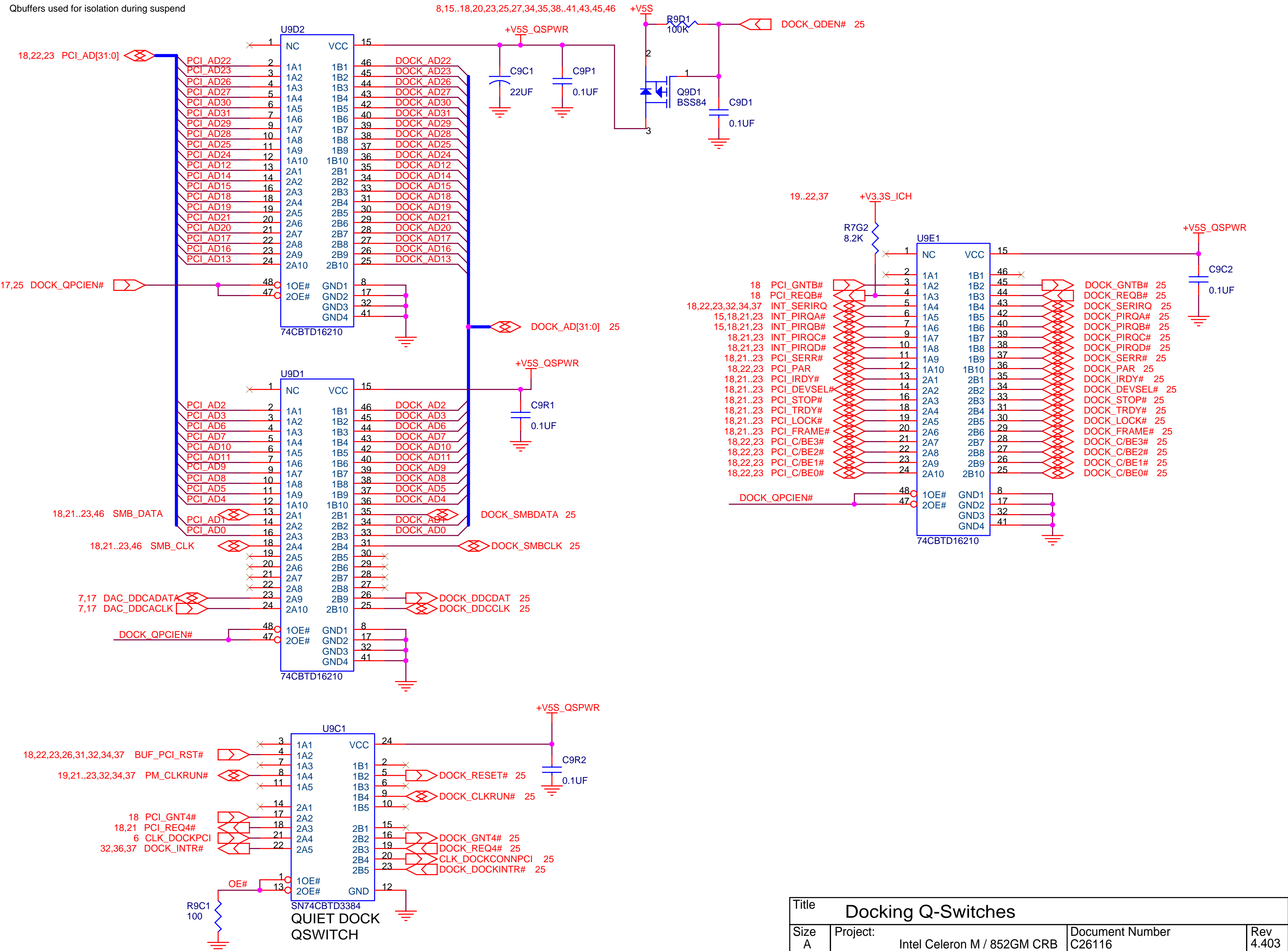

Qbuffers used for isolation during suspend
8,15..18,20,23,25,27,34,35,38..41,43,45,46
+V5S
+V5S_QSPWR
R9D1
100K
DOCK_QDEN# 25
C9C1
22UF
C9P1
0.1UF
Q9D1
BSS84
C9D1
0.1UF
U9D2
18,22,23 PCI_AD[31:0]
17,25 DOCK_QPCIEN#
74CBTD16210
DOCK_AD[31:0] 25
U9D1
C9R1
0.1UF
18,21..23,46 SMB_DATA
DOCK_SMBDATA 25
18,21..23,46 SMB_CLK
DOCK_SMBCLK 25
7,17 DAC_DDCADATA
7,17 DAC_DDCACLK
DOCK_DDCDAT 25
DOCK_DDCCLK 25
DOCK_QPCIEN#
19..22,37
+V3.3S_ICH
R7G2
8.2K
U9E1
C9C2
0.1UF
18 PCI_GNTB#
18 PCI_REQB#
18,22,23,32,34,37 INT_SERIRQ
15,18,21,23 INT_PIRQA#
15,18,21,23 INT_PIRQB#
18,21,23 INT_PIRQC#
18,21,23 INT_PIRQD#
18,21..23 PCI_SERR#
18,22,23 PCI_PAR
18,21..23 PCI_IRDY#
18,21..23 PCI_DEVSEL#
18,21..23 PCI_STOP#
18,21..23 PCI_TRDY#
18,21..23 PCI_LOCK#
18,21..23 PCI_FRAME#
18,22,23 PCI_C/BE3#
18,22,23 PCI_C/BE2#
18,22,23 PCI_C/BE1#
18,22,23 PCI_C/BE0#
DOCK_GNTB# 25
DOCK_REQB# 25
DOCK_SERIRQ 25
DOCK_PIRQA# 25
DOCK_PIRQB# 25
DOCK_PIRQC# 25
DOCK_PIRQD# 25
DOCK_SERR# 25
DOCK_PAR 25
DOCK_IRDY# 25
DOCK_DEVSEL# 25
DOCK_STOP# 25
DOCK_TRDY# 25
DOCK_LOCK# 25
DOCK_FRAME# 25
DOCK_C/BE3# 25
DOCK_C/BE2# 25
DOCK_C/BE1# 25
DOCK_C/BE0# 25
U9C1
18,22,23,26,31,32,34,37 BUF_PCI_RST#
19,21..23,32,34,37 PM_CLKRUN#
18 PCI_GNT4#
18,21 PCI_REQ4#
6 CLK_DOCKPCI
32,36,37 DOCK_INTR#
DOCK_RESET# 25
DOCK_CLKRUN# 25
DOCK_GNT4# 25
DOCK_REQ4# 25
CLK_DOCKCONNPCI 25
DOCK_DOCKINTR# 25
C9R2
0.1UF
OE#
R9C1
100
SN74CBTD3384
QUIET DOCK
QSWITCH
Title
Docking Q-Switches
Size A
Project: Intel Celeron M / 852GM CRB
Document Number C26116
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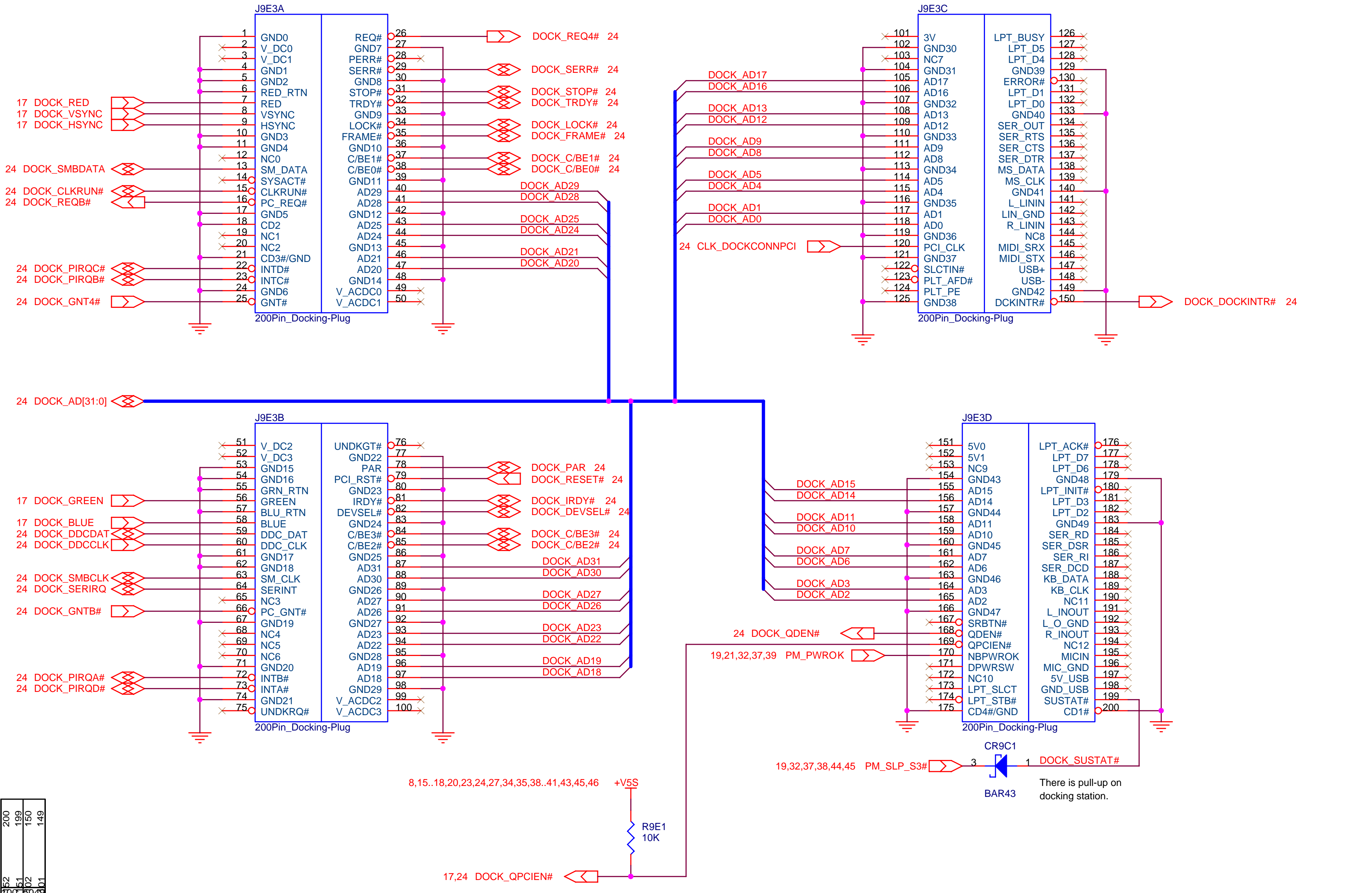
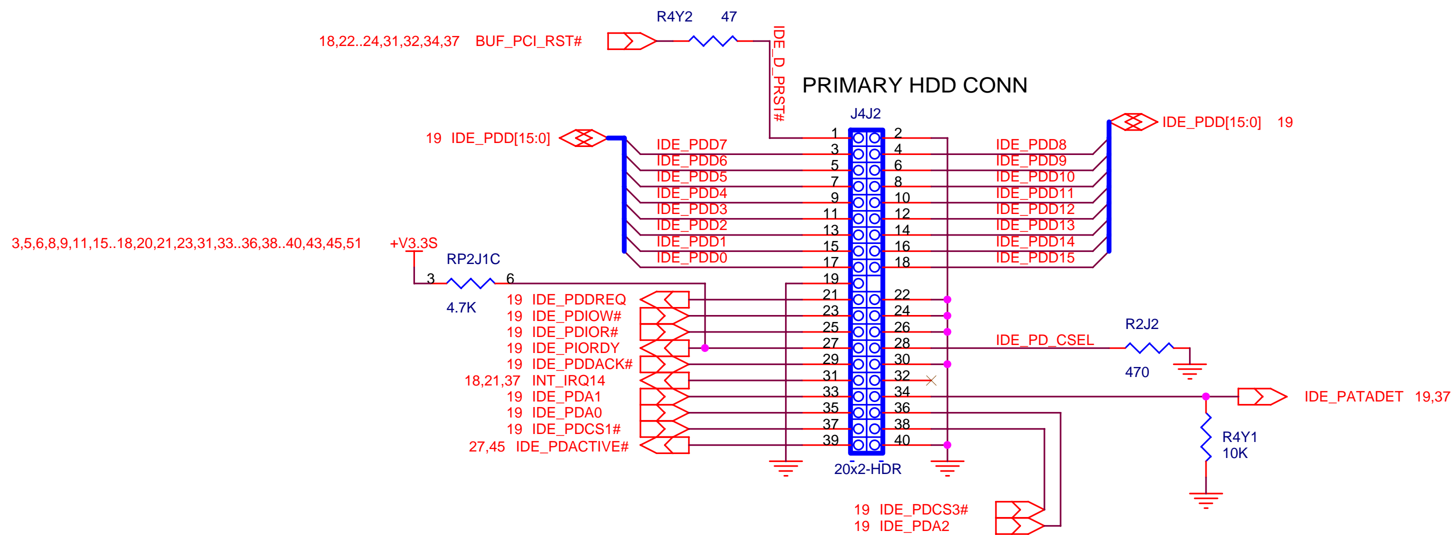
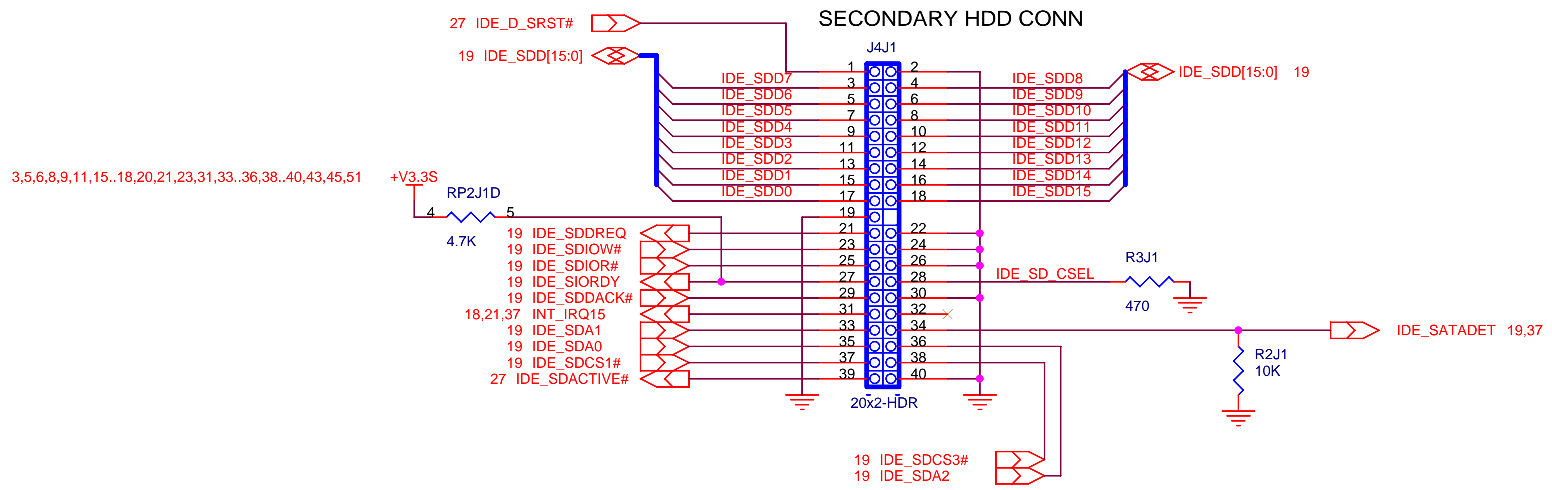
Date: Wednesday, January 12, 2005
Sheet 24 of 51



Title	Docking Connector		
Size A	Project: Intel Celeron M / 852GM CRB	Document Number C26116	Rev 4.403
Date: Wednesday, January 12, 2005		Sheet 25 of 51	





Title	IDE 1 of 2		
Size A	Project: Intel Celeron M / 852GM CRB	Document Number C26116	Rev 4.403
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Secondary IDE Power

8,15..18,20,23..25,34,35,38..41,43,45,46 +V5S
U3H1A 74HC14
C2H1 0.1UF
34,37 IDE_SPWR_EN#
IDE_SPWR_EN
U3H1E 74HC14
IDE_SPWR2_D
R2H5 1M
R2H6 390K
IDE_SPWR2
C2H2 1000PF
U2H1A SI4925DY
U2H1B SI4925DY
R2H1 NO_STUFF_0
V5S_IDE_PD
+V12S_IDE_S
+V5S_IDE_S
R2H7 0.01_1%
C2W3 0.1UF
C2J1 22UF
C2W2 0.1UF
C2H3 100uF
J2H1 4Pin_PwrConn

Note: Primary IDE Power on Turner DC/DC Module

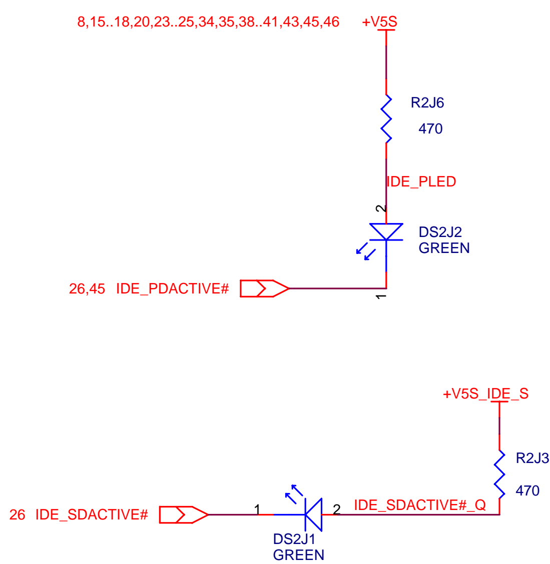
+V5S_IDE_S
R2H8 100K
SHMIDT4
R2W1 1M
C2W1 0.1UF
U3H1D 74HC14
SHMIDT2
U3H1B 74HC14
IDE_SRST#
R3H2 47
IDE_D_SRST# 26
Q3H1 BSS138
IDE_SPWR_EN#
<NO_STUFF>

15,17,23,37,45 +V12S
IDE_SPWR_EN_Q#
R2G15 1M
C2G14 1000PF
R2G14 100K
IDE_SPWR_EN_D#
IDE_SPWR_EN
Q3G1 2N7002
Q2G4 SI2307DS
+V12S_IDE_S

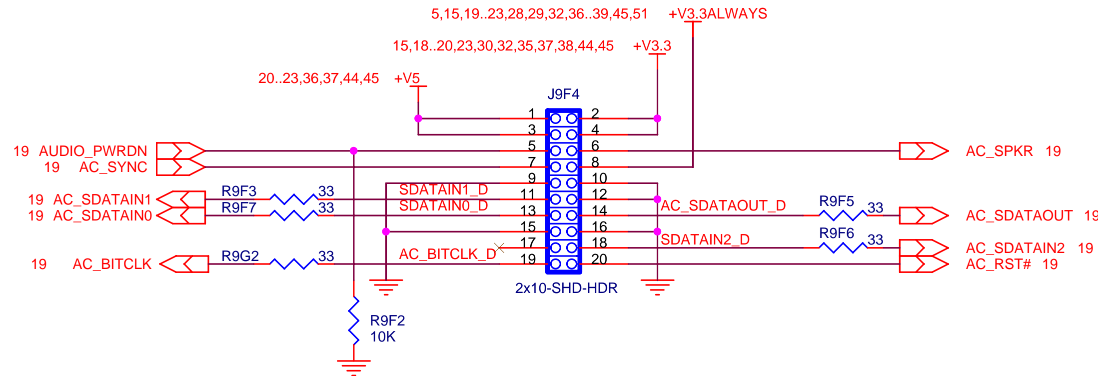
SPARE GATE
8,15..18,20,23..25,34,35,38..41,43,45,46 +V5S
U3H1C 74HC14
SHMIDT3
R3H1 0
TP_SHMIDT_C

For Secondary IDE Drive Only

IDE Activity LEDs

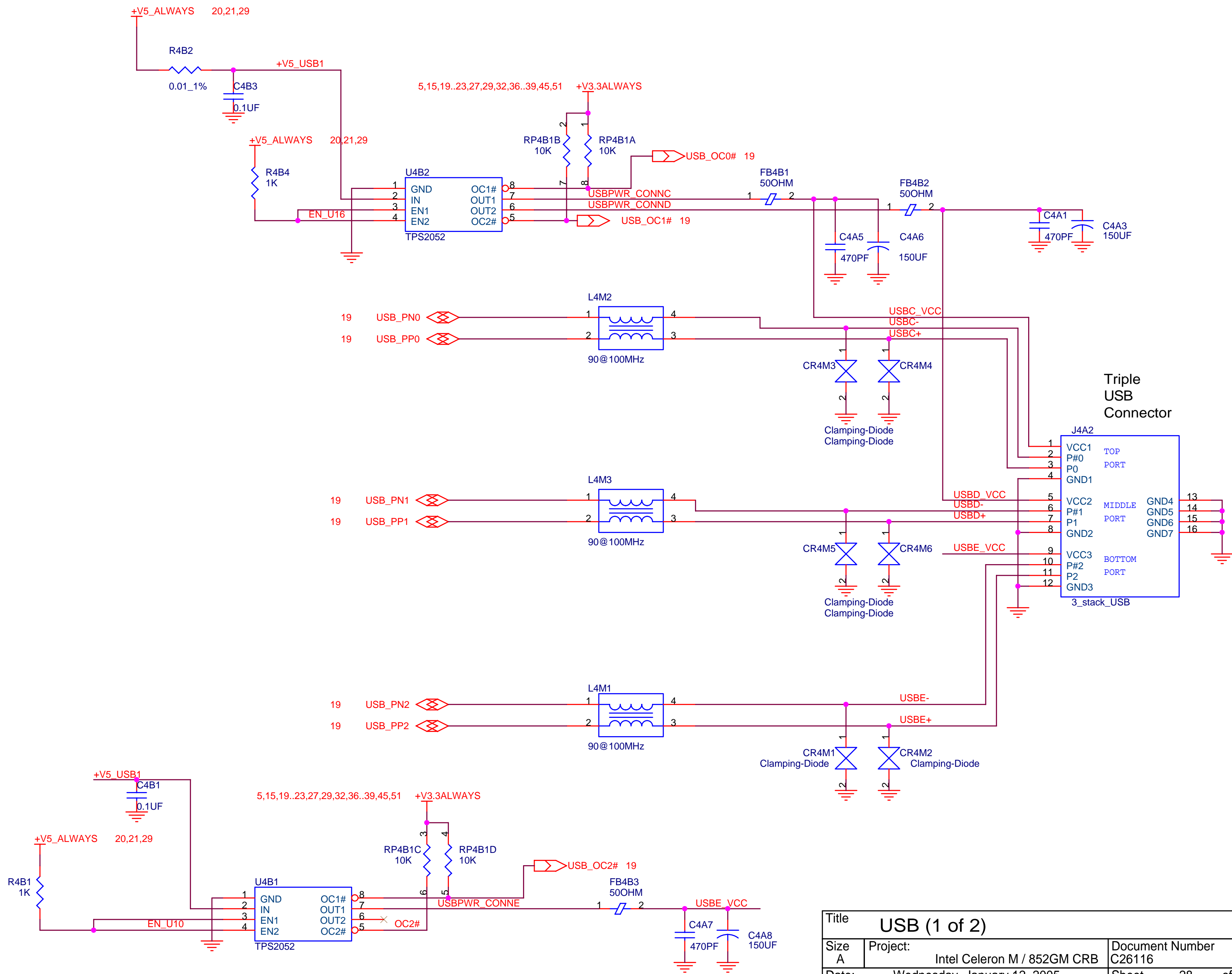


MDC Interposer Header



Layout Note:
Place R9F3, R9F7 and R9G2
0.1 to 0.4 inches from MDC
header based on topology

Title	IDE 2 of 2 / MDC INTERPOSER		
Size A	Project: Intel Celeron M / 852GM CRB	Document Number C26116	Rev 4.403
Date:	Wednesday, January 12, 2005	Sheet 27 of 51	



Title	USB (1 of 2)		
Size A	Project: Intel Celeron M / 852GM CRB	Document Number C26116	Rev 4.403
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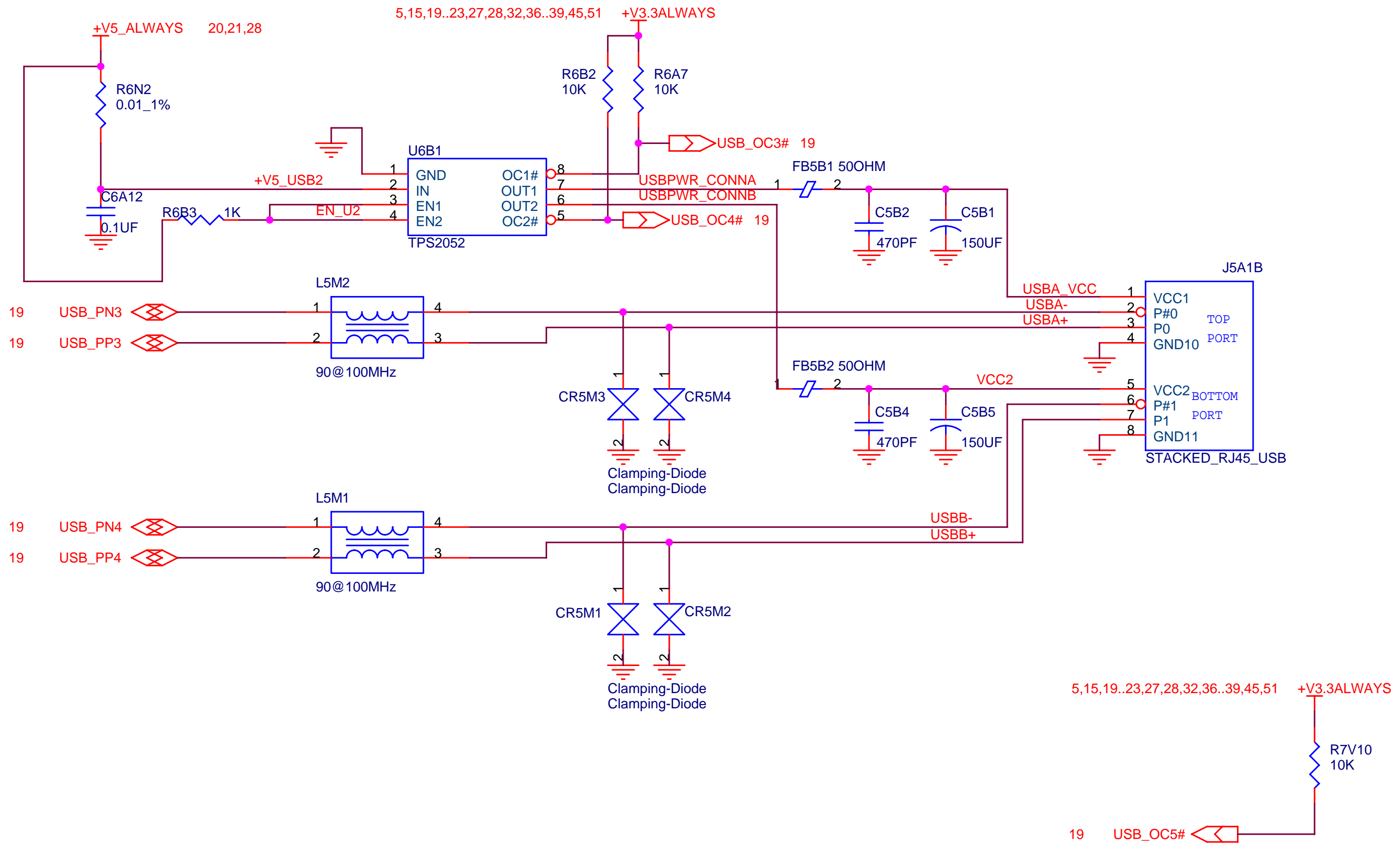
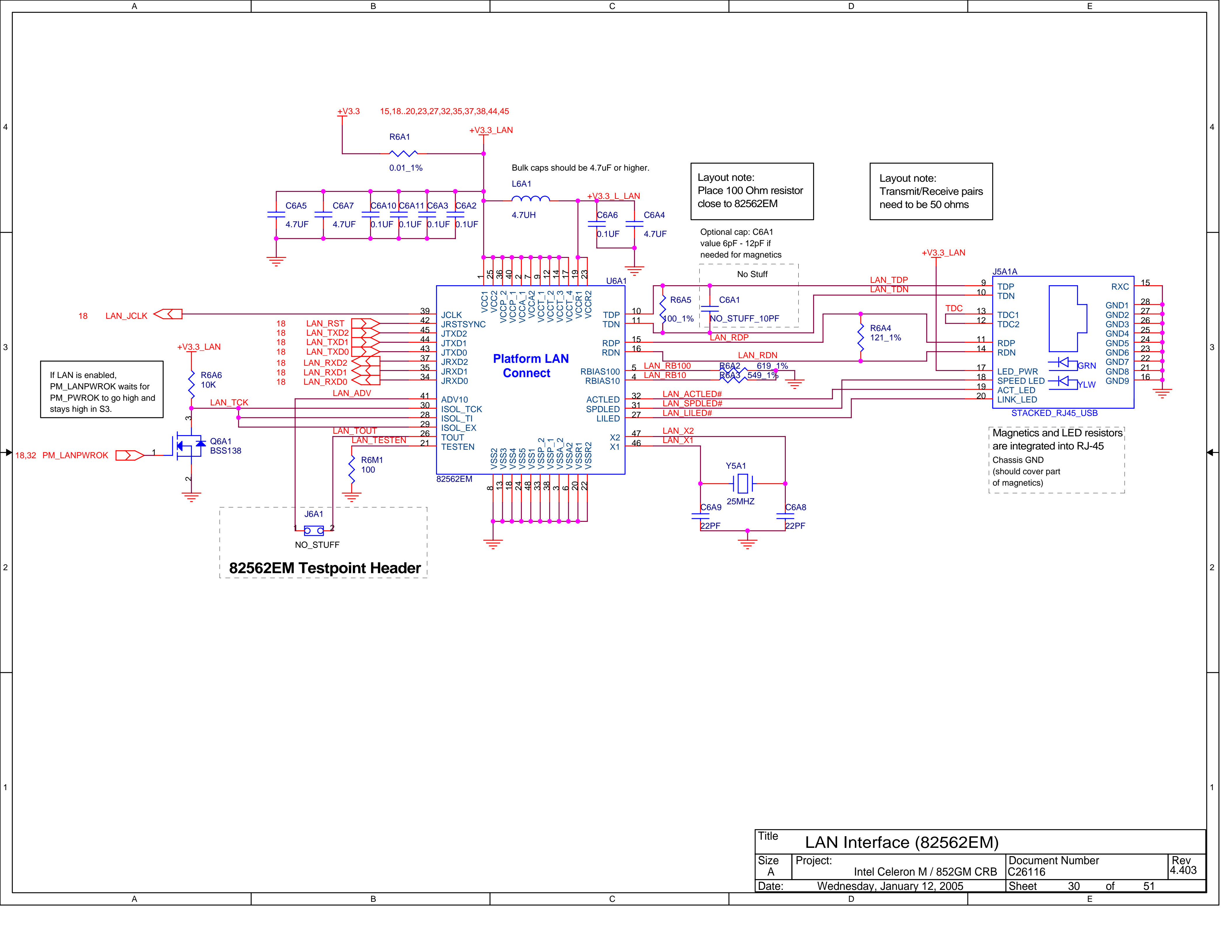


Title	USB Connector (2 of 2)		
Size A	Project: Intel Celeron M / 852GM CRB	Document Number C26116	Rev 4.403
Date: Wednesday, January 12, 2005		Sheet 29 of 51	



+V3.3
15,18..20,23,27,32,35,37,38,44,45
R6A1
0.01_1%
+V3.3_LAN
Bulk caps should be 4.7uF or higher.
L6A1
4.7UH
+V3.3_L_LAN
C6A5 4.7UF
C6A7 4.7UF
C6A10 0.1UF
C6A11 0.1UF
C6A3 0.1UF
C6A2 0.1UF
C6A6 0.1UF
C6A4 4.7UF
Layout note:
Place 100 Ohm resistor close to 82562EM
Layout note:
Transmit/Receive pairs need to be 50 ohms
Optional cap: C6A1 value 6pF - 12pF if needed for magnetics
No Stuff
C6A1
NO_STUFF_10PF
R6A5
100_1%
R6A4
121_1%
U6A1
Platform LAN Connect
82562EM
LAN_JCLK
LAN_RST
LAN_TXD2
LAN_TXD1
LAN_TXD0
LAN_RXD2
LAN_RXD1
LAN_RXD0
LAN_ADV
LAN_TCK
LAN_TOUT
LAN_TESTEN
LAN_TDP
LAN_TDN
LAN_RDP
LAN_RDN
LAN_RB100
LAN_RB10
R6A2 619_1%
R6A3 549_1%
LAN_ACTLED#
LAN_SPDLED#
LAN_LILED#
LAN_X2
LAN_X1
Y5A1
25MHZ
C6A9 22PF
C6A8 22PF
J5A1A
STACKED_RJ45_USB
TDP
TDN
TDC1
TDC2
RDP
RDN
LED_PWR
SPEED LED
ACT_LED
LINK_LED
RXC
GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND8 GND9
GRN
YLW
TDC
Magnetics and LED resistors are integrated into RJ-45
Chassis GND (should cover part of magnetics)
If LAN is enabled, PM_LANPWROK waits for PM_PWROK to go high and stays high in S3.
R6A6 10K
Q6A1 BSS138
18,32 PM_LANPWROK
R6M1 100
J6A1
NO_STUFF
82562EM Testpoint Header
Title LAN Interface (82562EM)
Size A
Project: Intel Celeron M / 852GM CRB
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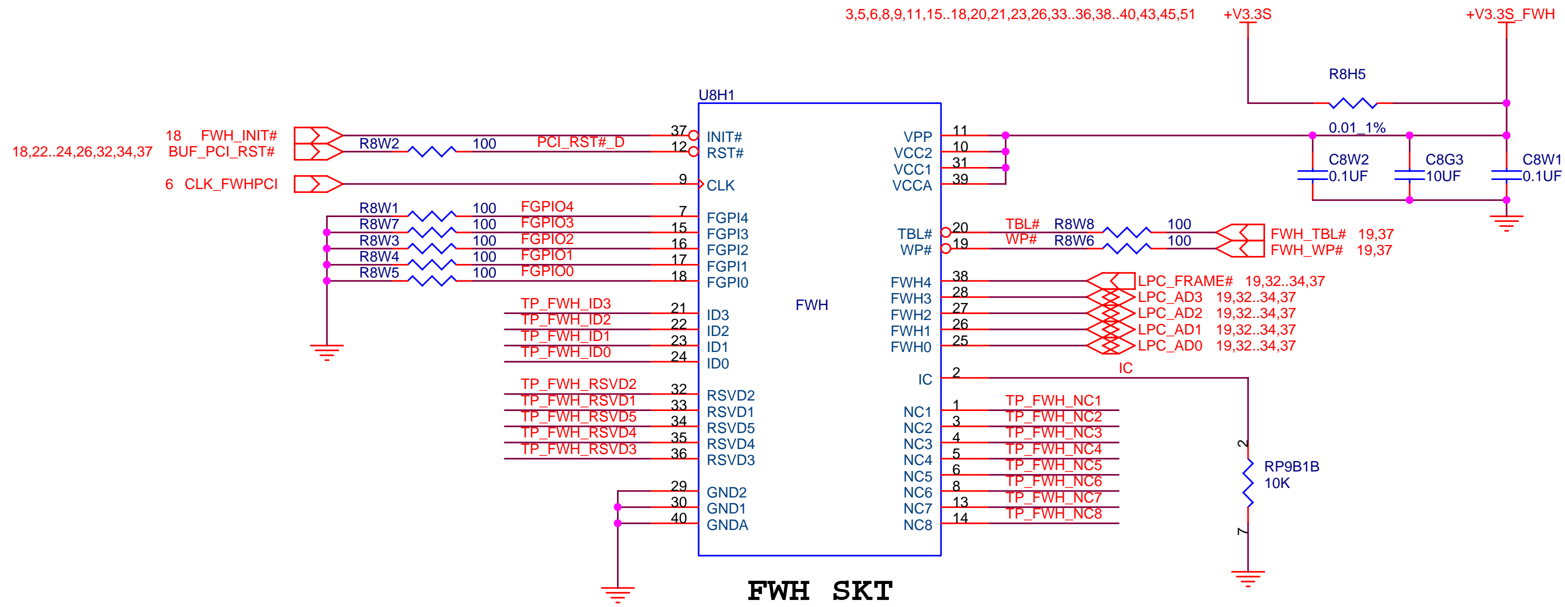

FWH sits in the
FWH_TSOP_Socket,
Not on the board

Title	FWH		
Size A	Project: Intel Celeron M / 852GM CRB	Document Number C26116	Rev 4.403
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KSC	J8A2
Enable	1-2 (Default)
Disable	2-3

Decode KBC Addresses	J9A1
Enable 60h & 64h	No Shunt (Default)
Disable	Shunt

Boot Mode Programming Straps

P90-P92 needs to be at VCC for boot mode programming. They are already pulled up in the design. MD0, MD1 needs to be at Vss. Jumper for J9B1 needs to be populated. System needs to supply +V3ALWAYS to flash connector.

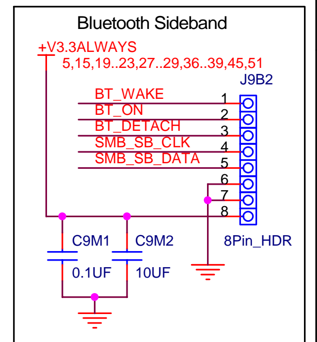
J9B1 — Shunt to program

U9B1 H8S/2149F-Z

Stuff R9A4 only for in-ckt programming

LID SWITCH

VIRTUAL BATTERY



J9A4 Measurement Point

GATE OFF PCIRST# during S3

Programming Interface

Note: for flash progamming, must use TX1 and RX1, which are pin97 and pin98.

KSC Testpoint Header

Testpoint Header

Title	System Management and Keyboard Controller		
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SMC SUSPEND TIMER

NMI Jumper
NOTE: Shunt J8A1 for
SMC Programming

Circuitry provides an interrupt to the SMC every 1s while in suspend (this allows the SMC to complete housekeeping functions while suspended)

1Hz Clock	J8A1
Disable	Shunt (Default)
Enable	No Shunt

Spare gates

PORT 80-83 DISPLAY

PORT 80, 82

PORT 81, 83

High Nibble (Left)

Low Nibble (Right)

High Nibble (Left)

Low Nibble (Right)

Port	J9H1
82-83	Shunt
80-81	No Shunt (Default)

Title	SMC Suspend Timer and Port 80 LEDs		
Size: A	Project: Intel Celeron M / 852GM CRB	Document Number: C26116	Rev: 4.403
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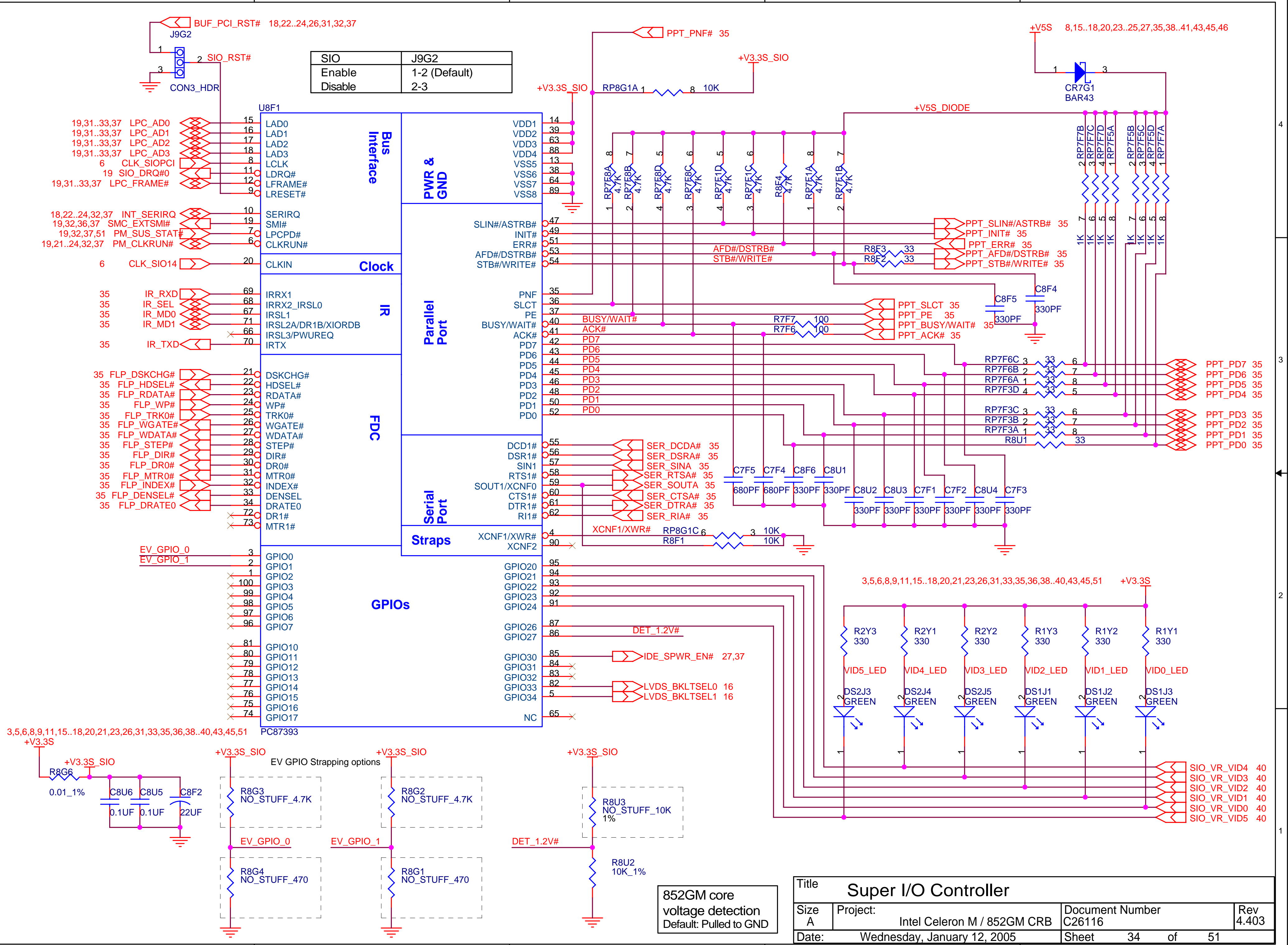

Title	Super I/O Controller		
Size A	Project: Intel Celeron M / 852GM CRB	Document Number C26116	Rev 4.403
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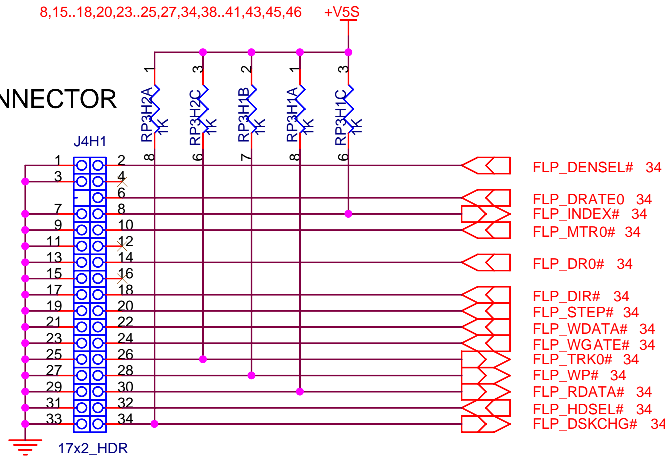

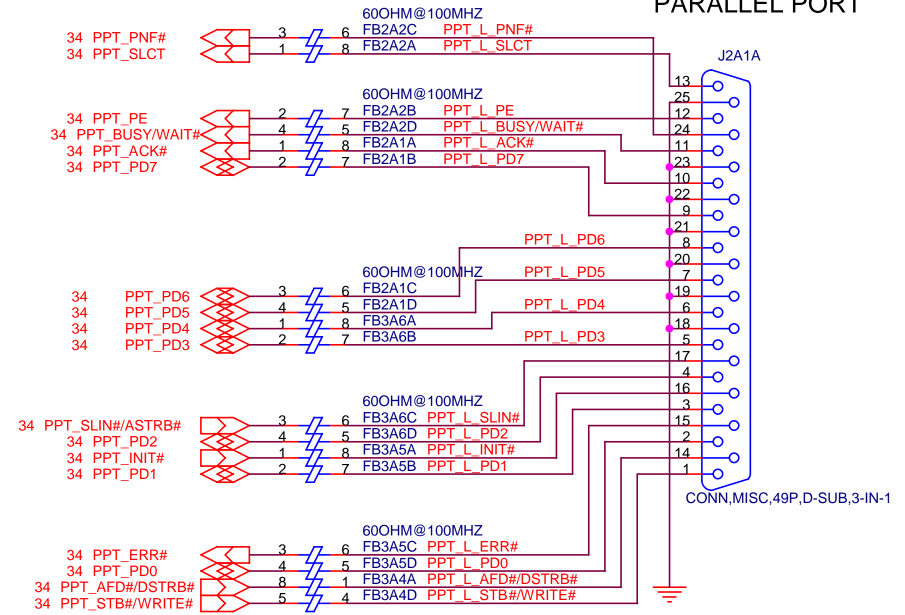

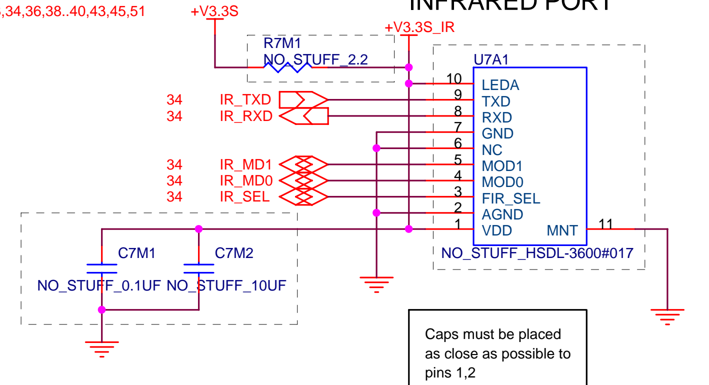

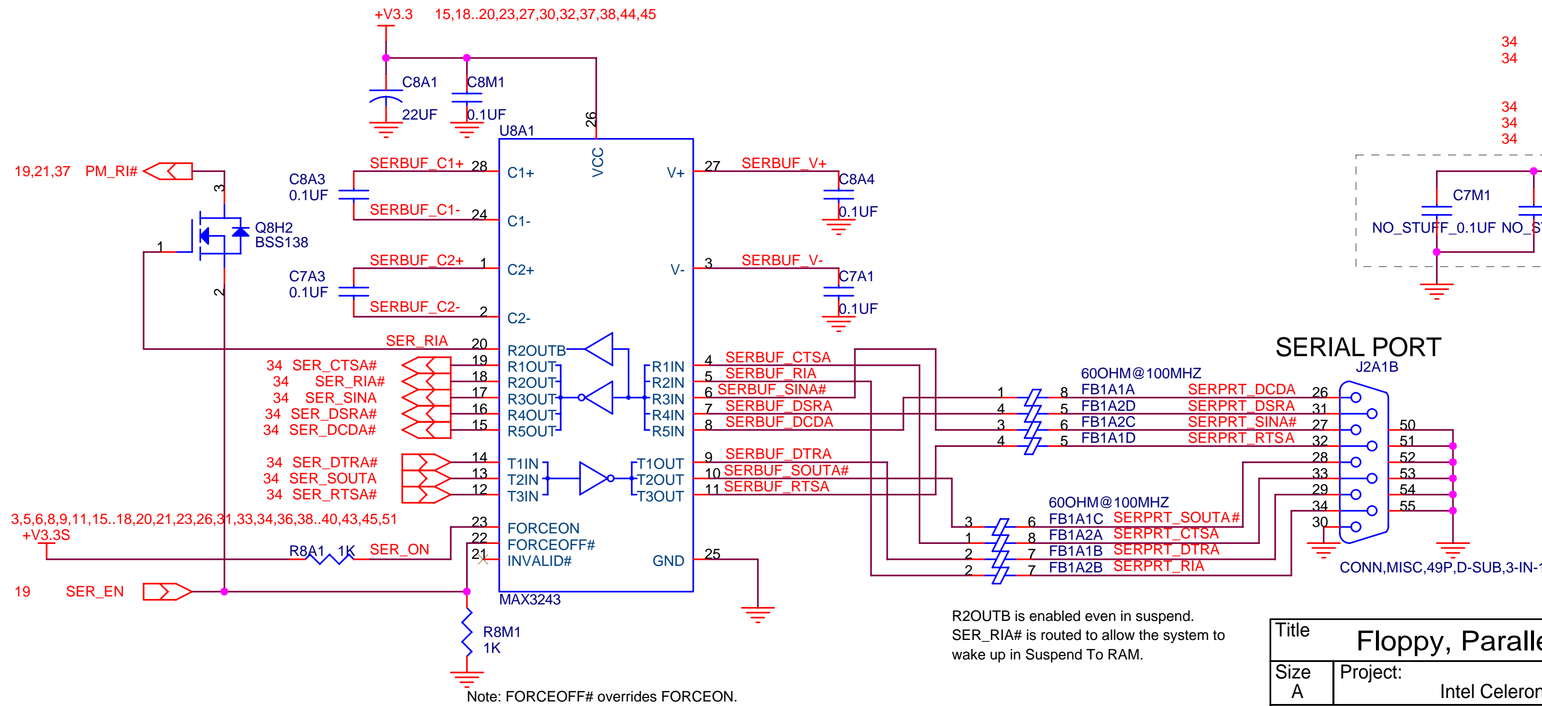

Title	Floppy, Parallel, Serial, and IR Ports		
Size A	Project: Intel Celeron M / 852GM CRB	Document Number C26116	Rev 4.403
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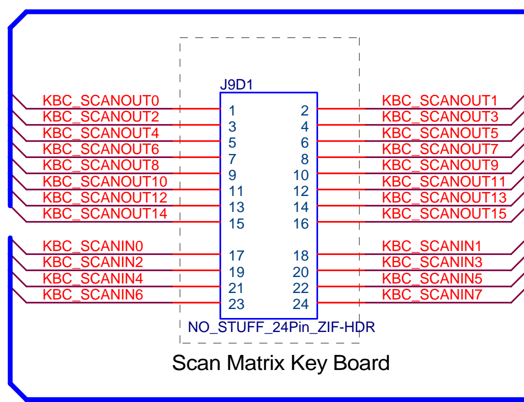
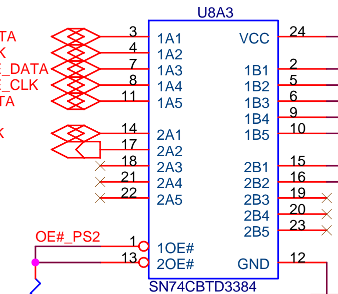
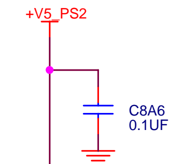


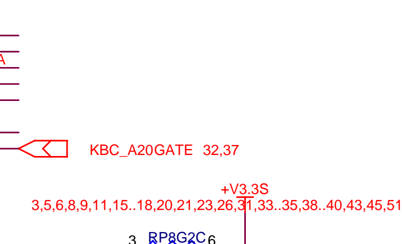
KBC_SCANOUT[15:0] 32

KBC_SCANIN[7:0] 32

CBTD has integrated diode for 5V to 3.3V voltage translation



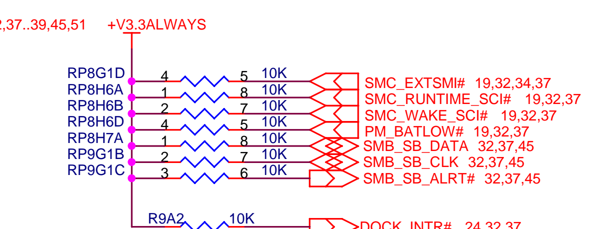




R8A5 100

+V3.3S
3,5,6,8,9,11,15..18,20,21,23,26,31,33..35,38..40,43,45,51
RP8G2C 8.2K

5,15,19..23,27..29,32,37..39,45,51 +V3.3ALWAYS



+V5_PS2 RP1B1B 4.7K GP_CLK FB1A9 60ohm@100MHz CP1A1B 47PF

+V5_PS2 F1A1 1.1A PS2_PWR_L FB1A6 31Ohm@100MHz L_PS2_PWR

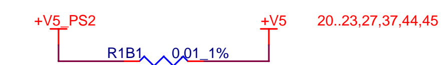
L_GPDATA FB1A4 60ohm@100MHz +V5_PS2 RP1B2A 4.7K GP_DATA C1A2 47pF

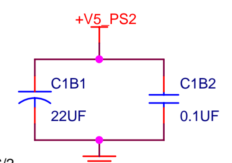
+V5_PS2 RP1B2D 4.7K KBD_CLK FB1A8 60ohm@100MHz CP1A1C 47PF L_GPCLK L_KBD_CLK

J1A1 DUAL_PS2 L_KBD_DATA FB1A3 60ohm@100MHz +V5_PS2 RP1B2B 4.7K KBD_DATA C1A1 47pF

+V5_PS2 RP1B2C 4.7K MOUSE_CLK FB1A7 60ohm@100MHz CP1A1D 47PF L_MOUSE_CLK

L_MOUSE_DATA FB1A5 60ohm@100MHz +V5_PS2 RP1B1A 4.7K MOUSE_DATA CP1A1A 47PF





If a PS/2 "breakout" connector is used,the keyboard PS/2 connector can be used for both a PS/2 keyboard and a second PS/2 mouse. Otherwise, the keyboard PS/2 connector will only support a PS/2 keyboard.

Title	Keyboard and Mouse Connectors		
Size A	Project: Intel Celeron M / 852GM CRB	Document Number C26116	Rev 4.403
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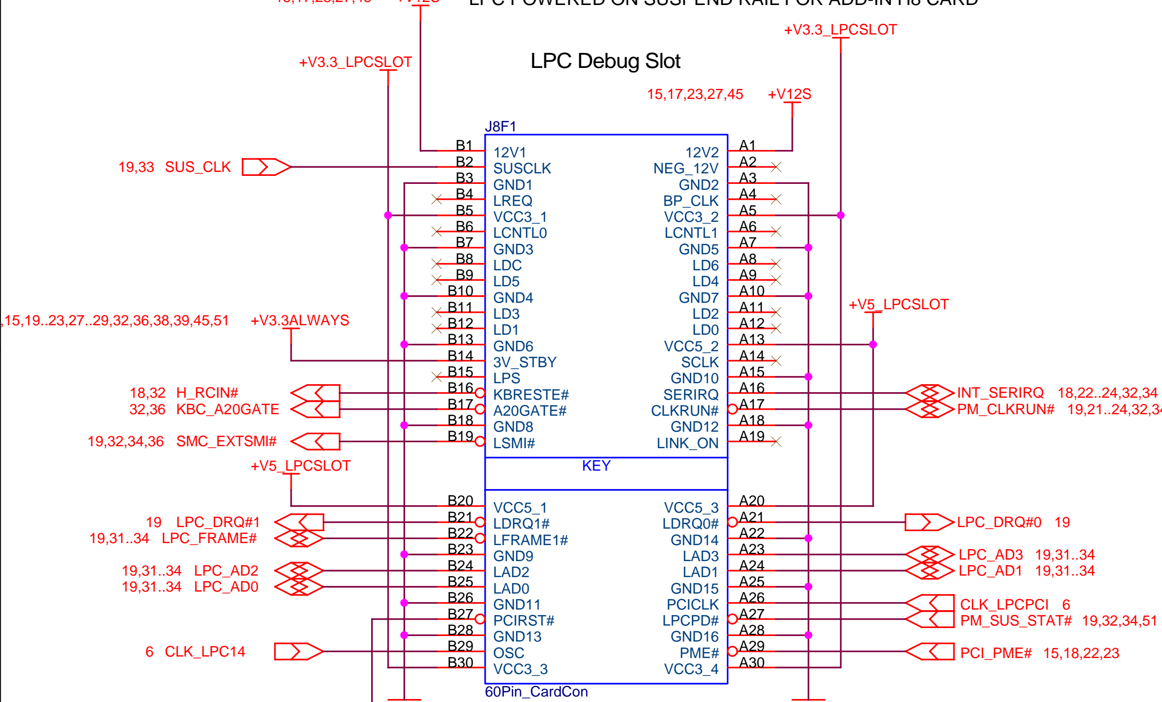
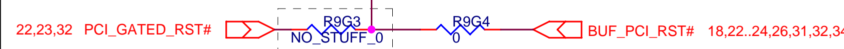
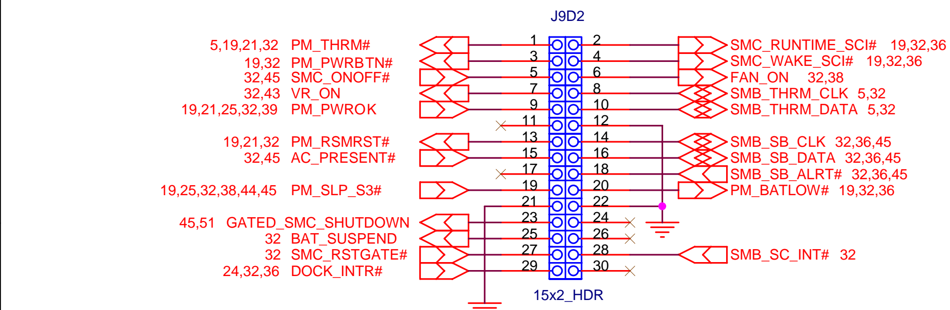
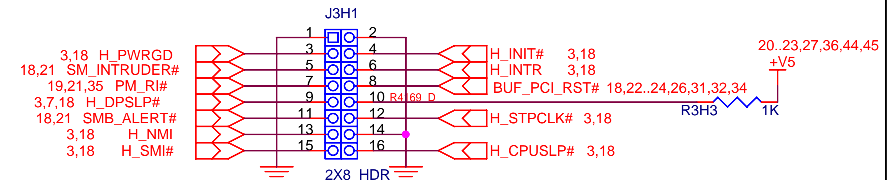
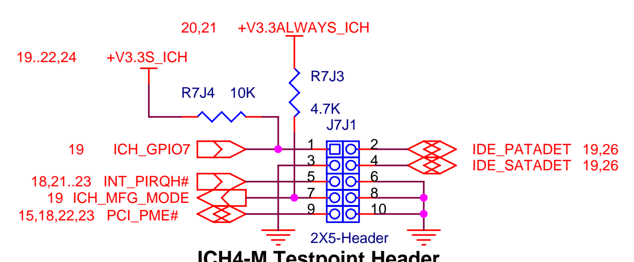
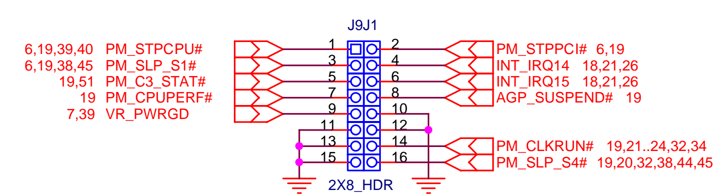


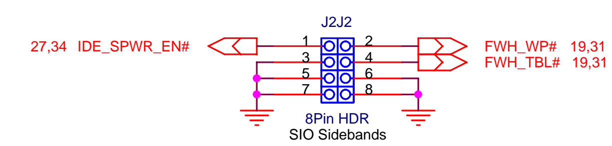




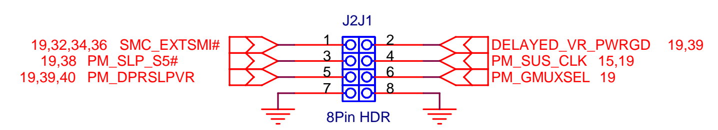


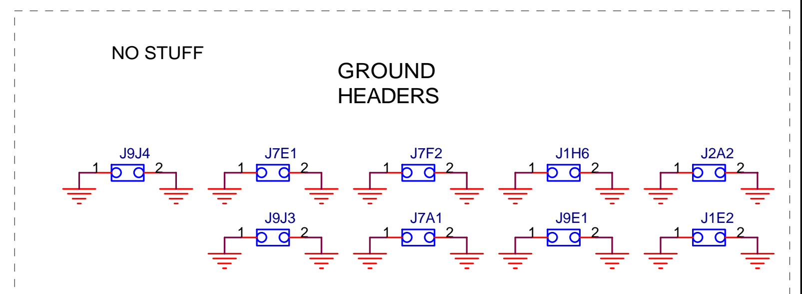






TEST HEADER





Title	LPC Slot & Debug Headers		
Size A	Project: Intel Celeron M / 852GM CRB	Document Number C26116	Rev 4.403
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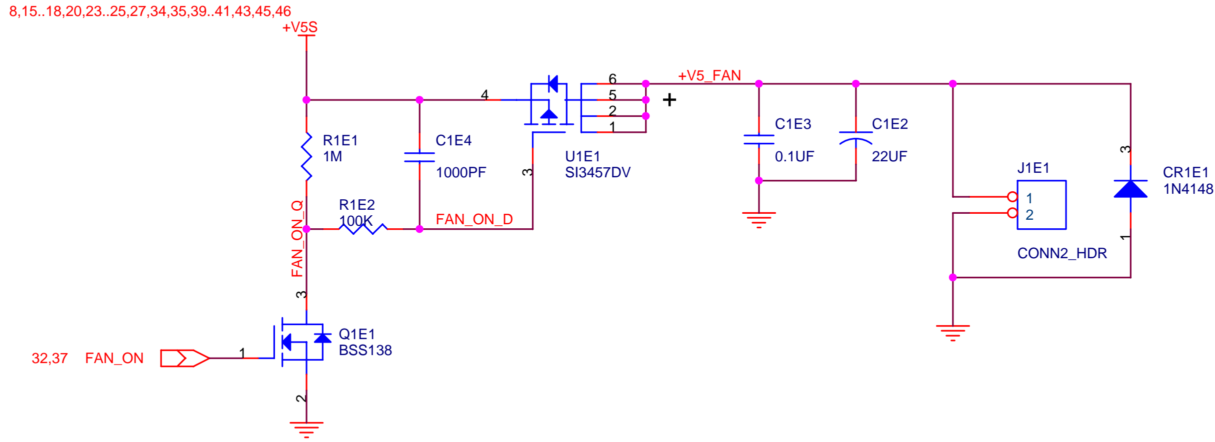
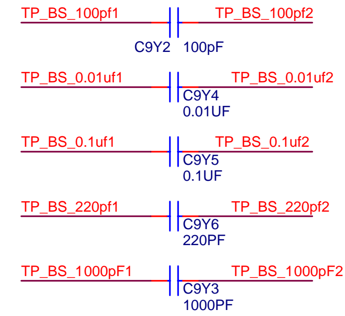
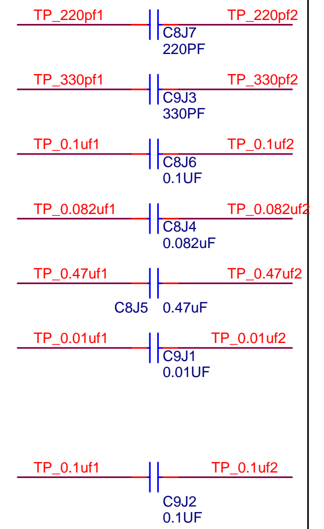
Fan Power Control







System State LEDs

5,15,19..23,27..29,32,36,37,39,45,51
+V3.3ALWAYS
19,37 PM_SLP_S5#
Q2G6
SI2307DS
S5_LED_C
R2H3
68
S5_LED_A
LED for S5
DS2H1
GREEN

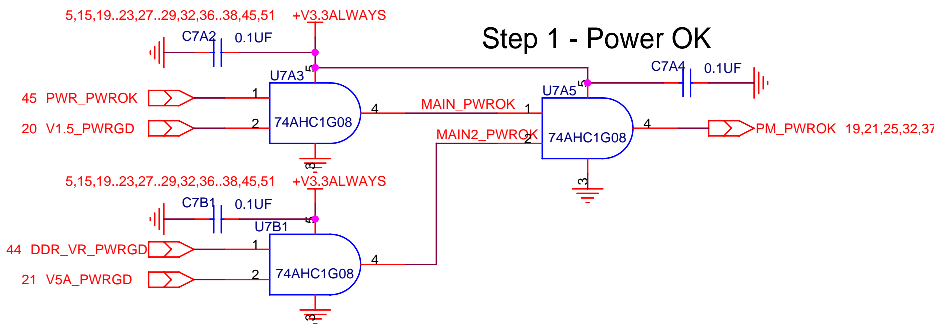
5,15,19..23,27..29,32,36,37,39,45,51
+V3.3ALWAYS
19,20,32,37,44,45 PM_SLP_S4#
Q2G2
SI2307DS
S4_LED_C
R2H4
68
S4_LED_A
LED for S4
DS2H2
GREEN
19,37 PM_SLP_S5#
Q2G3
BSS138

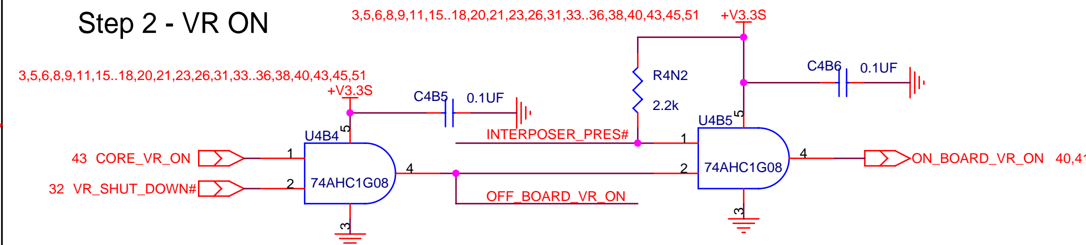
15,18..20,23,27,30,32,35,37,44,45
+V3.3
19,25,32,37,44,45 PM_SLP_S3#
Q2G5
SI2307DS
PM_SUSLEDPWR
R2H2
68
PM_SUSLED
LED for S3
DS1H2
GREEN

3,5,6,8,9,11,15..18,20,21,23,26,31,33..36,39,40,43,45,51
+V3.3S
PM_SLP_S1#
6,19,37,45
Q1G2
SI2307DS
S1_LED_C
R1H2
68
S1_LED_A
LED for S1
DS1H3
GREEN

3,5,6,8,9,11,15..18,20,21,23,26,31,33..36,39,40,43,45,51
+V3.3S
R1H1
68
SO_LED_A
LED for S0
DS1H1
GREEN
SO_LED_C
PM_SLP_S1#
6,19,37,45
Q1G1
BSS138

Title	Fan Circuit, Test Capacitors and System State LEDs		
Size A	Project: Intel Celeron M / 852GM CRB	Document Number C26116	Rev 4.403
Date: Wednesday, January 12, 2005		Sheet 38 of 51	





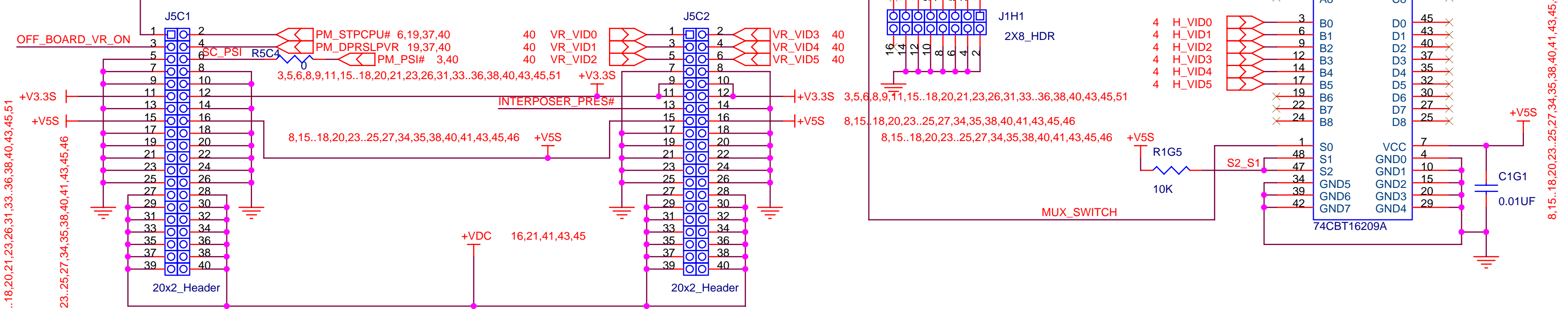
Step 3 - Power Good

VR PWRGD CIRCUIT

Note: J1H1 enables Manual VID strapping

With pin 13 high, B input goes to C output. With pin 13 low, A input goes to C output.

Input	Output	S2	S1	S0
A	C	1	1	0
B	C	1	1	1

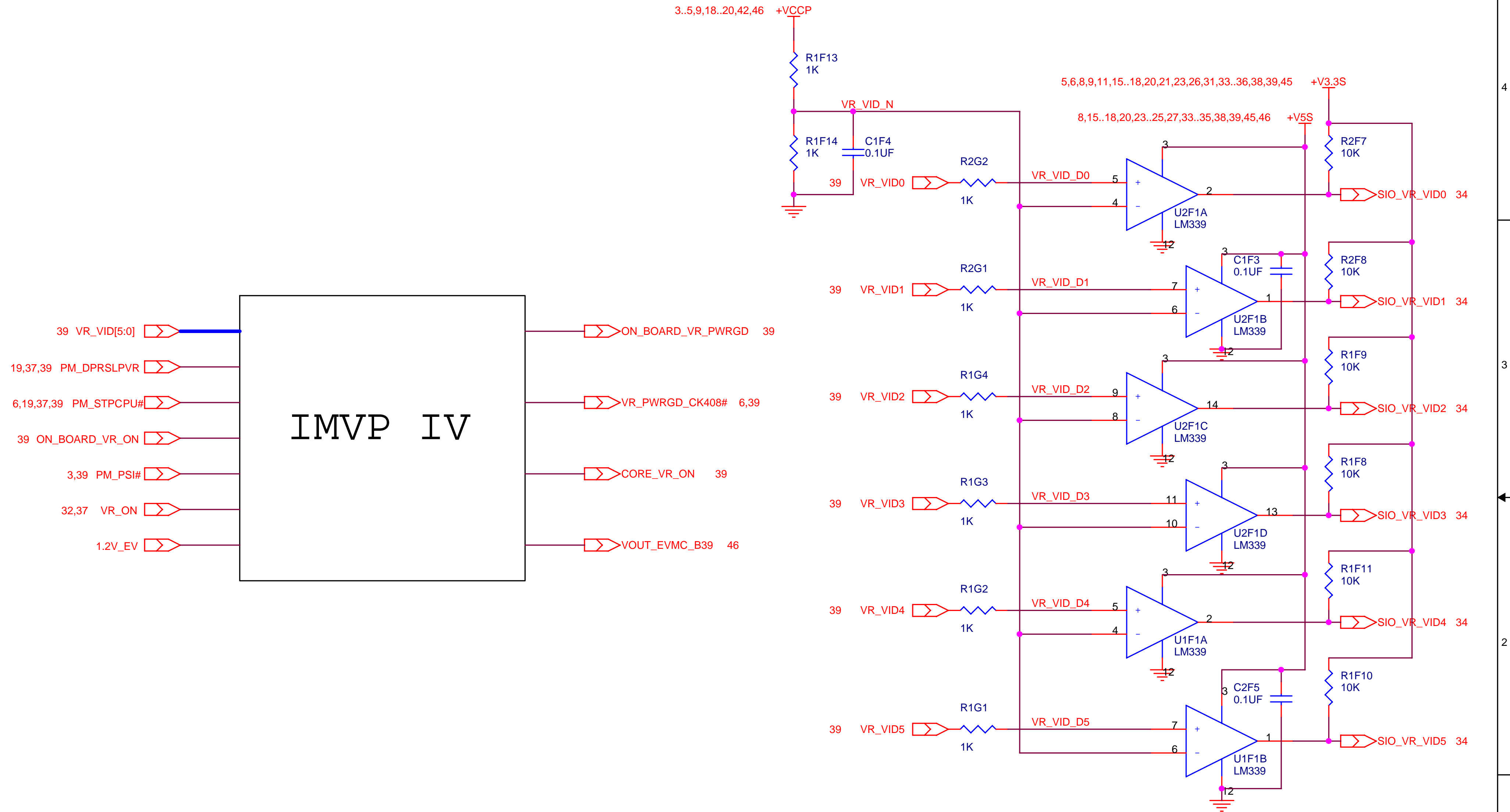


Connector 1 (rows A,B)

VR Interposer Headers

Connector 2 (rows C,D)

Title	Processor VR Interposer Support & Power Circuitry		
Size A	Project: Intel Celeron M / 852GM CRB	Document Number C26116	Rev 4.403
Date:	Wednesday, January 12, 2005	Sheet 39 of 51	



Title	IMVP-IV & Mux Buffer		
Size A	Project: Intel Celeron M / 852GM CRB	Document Number C26116	Rev 4.403
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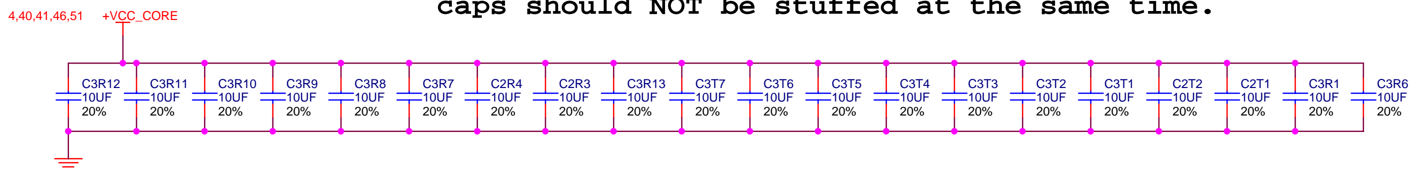
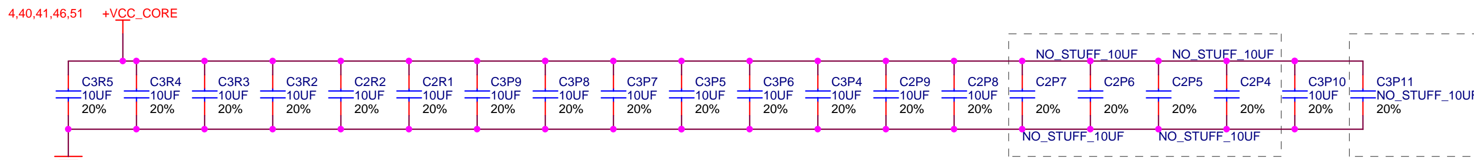
Blank

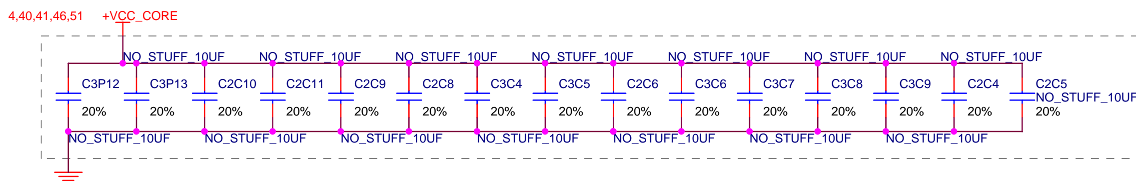
Title			
Size B	Project: Intel Celeron M / 852GM CRB	Document Number C26116	Rev 4.403
Date: Wednesday, January 12, 2005		Sheet 41 of 51	

VCore HF and Bulk Decoupling

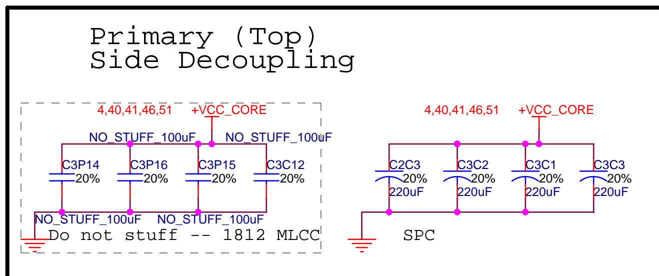
This solution will allow any of the decoupling options. All caps should NOT be stuffed at the same time.



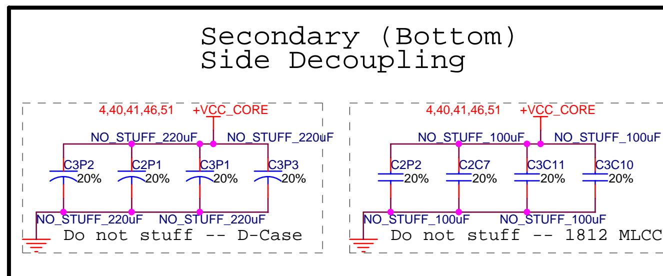




Primary (Top) Side Decoupling

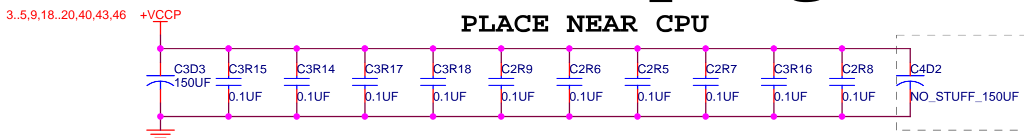


Secondary (Bottom) Side Decoupling

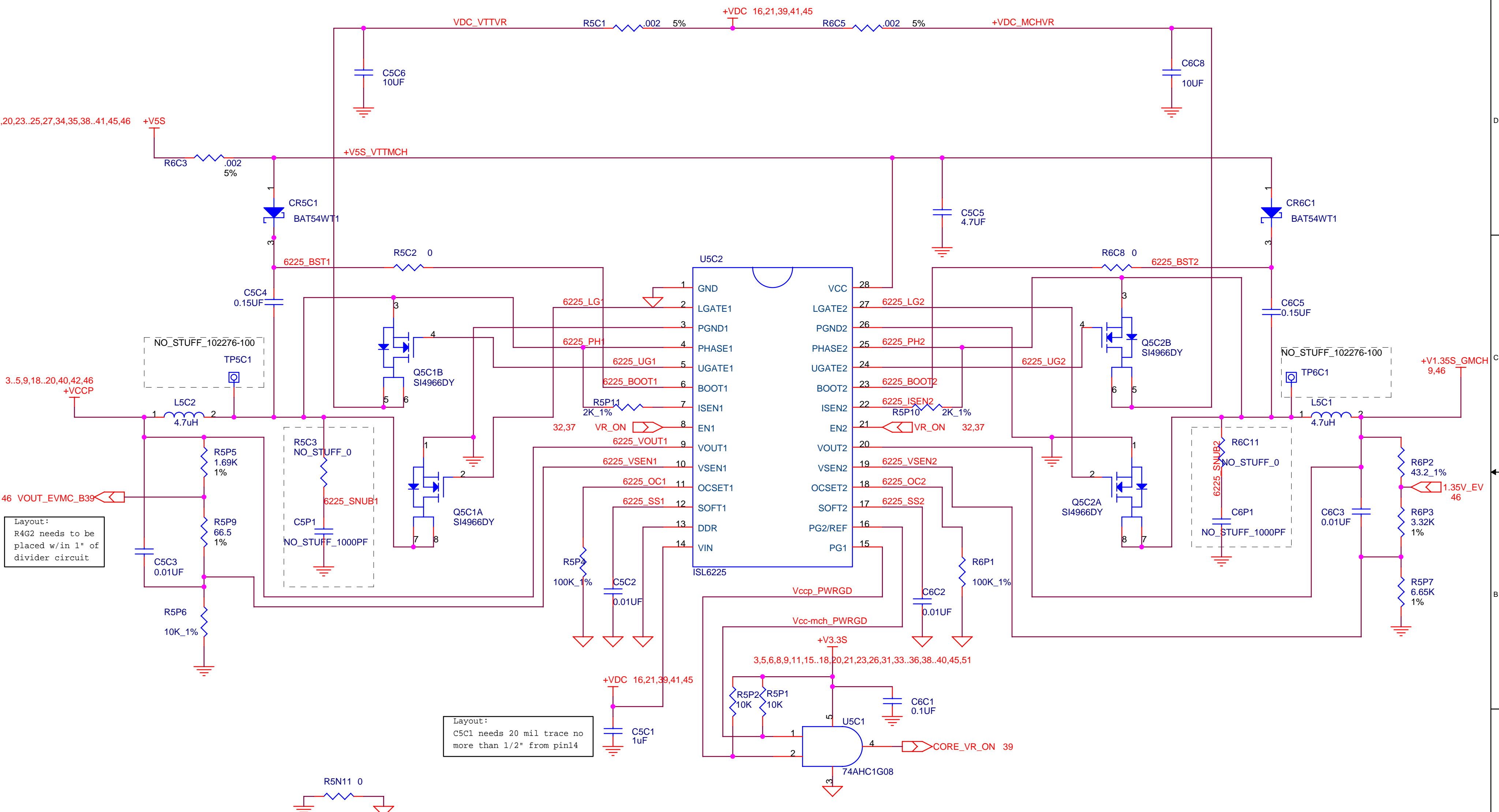


VCCP Decoupling

PLACE NEAR CPU



Title	Processor Decoupling		
Size B	Project: Intel Celeron M / 852GM CRB	Document Number C26116	Rev 4.403
Date:	Wednesday, January 12, 2005	Sheet 42 of 51	


VDC_VTTVR
R5C1 .002 5%
+VDC 16,21,39,41,45
R6C5 .002 5%
+VDC_MCHVR
C5C6 10UF
C6C8 10UF
8,20,23..25,27,34,35,38..41,45,46 +V5S
R6C3 .002 5%
+V5S_VTTMCH
CR5C1 BAT54WT1
CR6C1 BAT54WT1
C5C5 4.7UF
6225_BST1
R5C2 0
R6C8 0
6225_BST2
C5C4 0.15UF
C6C5 0.15UF
U5C2
GND
LGATE1
PGND1
PHASE1
UGATE1
BOOT1
ISEN1
EN1
VOUT1
VSEN1
OCSET1
SOFT1
DDR
VIN
VCC
LGATE2
PGND2
PHASE2
UGATE2
BOOT2
ISEN2
EN2
VOUT2
VSEN2
OCSET2
SOFT2
PG2/REF
PG1
ISL6225
6225_LG1
6225_PH1
6225_UG1
6225_BOOT1
R5P11 2K_1%
32,37 VR_ON
6225_VOUT1
6225_VSEN1
6225_OC1
6225_SS1
6225_LG2
6225_PH2
6225_UG2
6225_BOOT2
6225_ISEN2
R5P10 2K_1%
VR_ON 32,37
6225_VSEN2
6225_OC2
6225_SS2
Q5C1B SI4966DY
Q5C1A SI4966DY
Q5C2B SI4966DY
Q5C2A SI4966DY
NO_STUFF_102276-100
TP5C1
TP6C1
3..5,9,18..20,40,42,46 +VCCP
L5C2 4.7uH
L5C1 4.7uH
+V1.35S_GMCH 9,46
R5C3 NO_STUFF_0
6225_SNUB1
C5P1 NO_STUFF_1000PF
R6C11 NO_STUFF_0
6225_SNUB2
C6P1 NO_STUFF_1000PF
R5P5 1.69K 1%
46 VOUT_EVMC_B39
R5P9 66.5 1%
C5C3 0.01UF
R5P6 10K_1%
Layout:
R4G2 needs to be placed w/in 1" of divider circuit
R5P4 100K_1%
C5C2 0.01UF
C6C2 0.01UF
R6P1 100K_1%
C6C3 0.01UF
R6P2 43.2_1%
1.35V_EV 46
R6P3 3.32K 1%
R5P7 6.65K 1%
Vccp_PWRGD
Vcc-mch_PWRGD
+V3.3S
3,5,6,8,9,11,15..18,20,21,23,26,31,33..36,38..40,45,51
+VDC 16,21,39,41,45
R5P2 10K
R5P1 10K
C6C1 0.1UF
U5C1
74AHC1G08
CORE_VR_ON 39
C5C1 1uF
Layout:
C5C1 needs 20 mil trace no more than 1/2" from pin14
R5N11 0
Intel 852GM GMCH VR Controller
Title Intel 852GM GMCH VR and VCCP
Size B
Project: Intel Celeron M / 852GM CRB
Document Number C26116
Rev 4.403
Date: Wednesday, January 12, 2005
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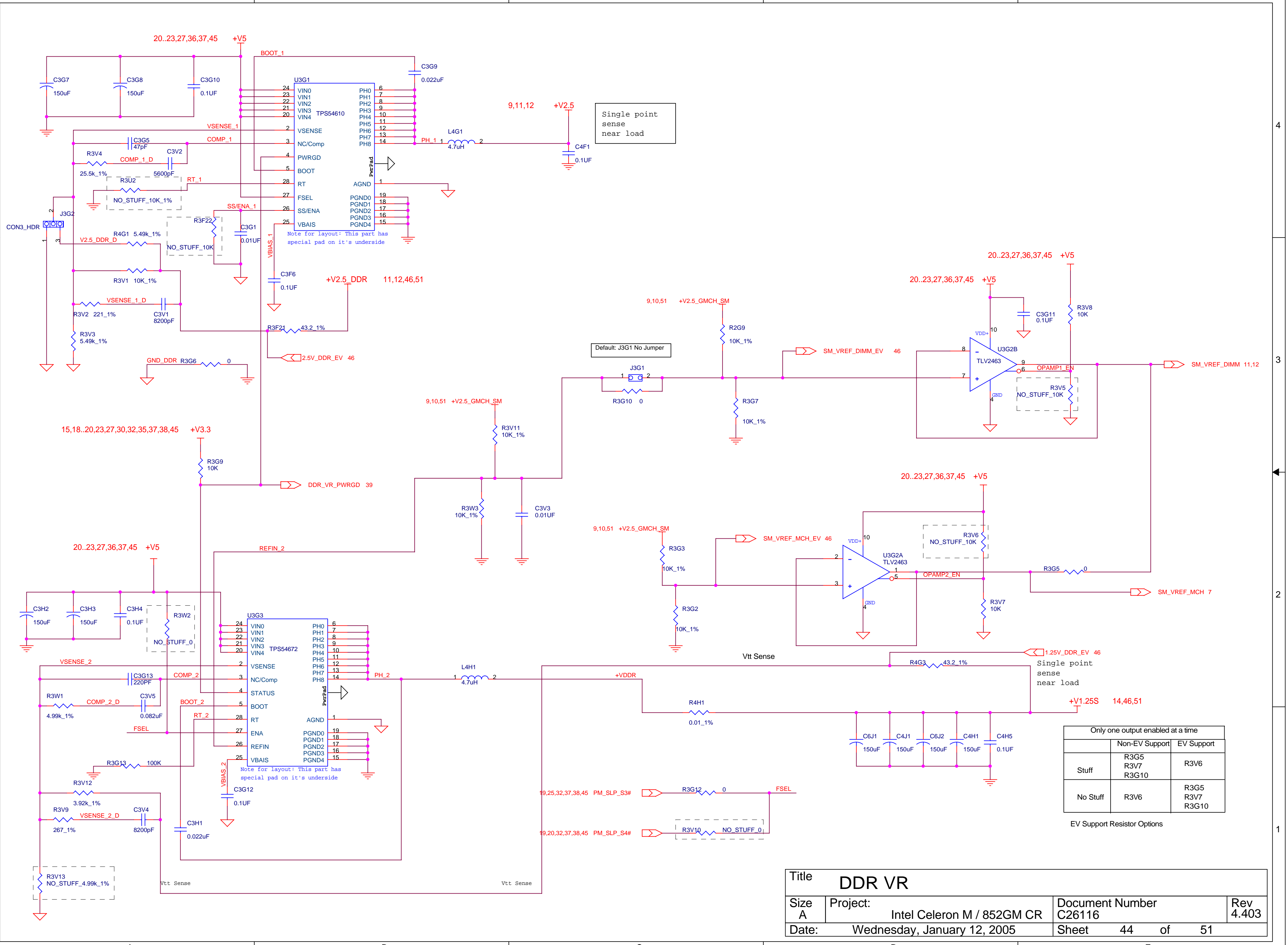

	Non-EV Support	EV Support
Stuff	R3G5 R3V7 R3G10	R3V6
No Stuff	R3V6	R3G5 R3V7 R3G10

Title	DDR VR		
Size A	Project: Intel Celeron M / 852GM CR	Document Number C26116	Rev 4.403
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HDM Connector Assembly (base board)

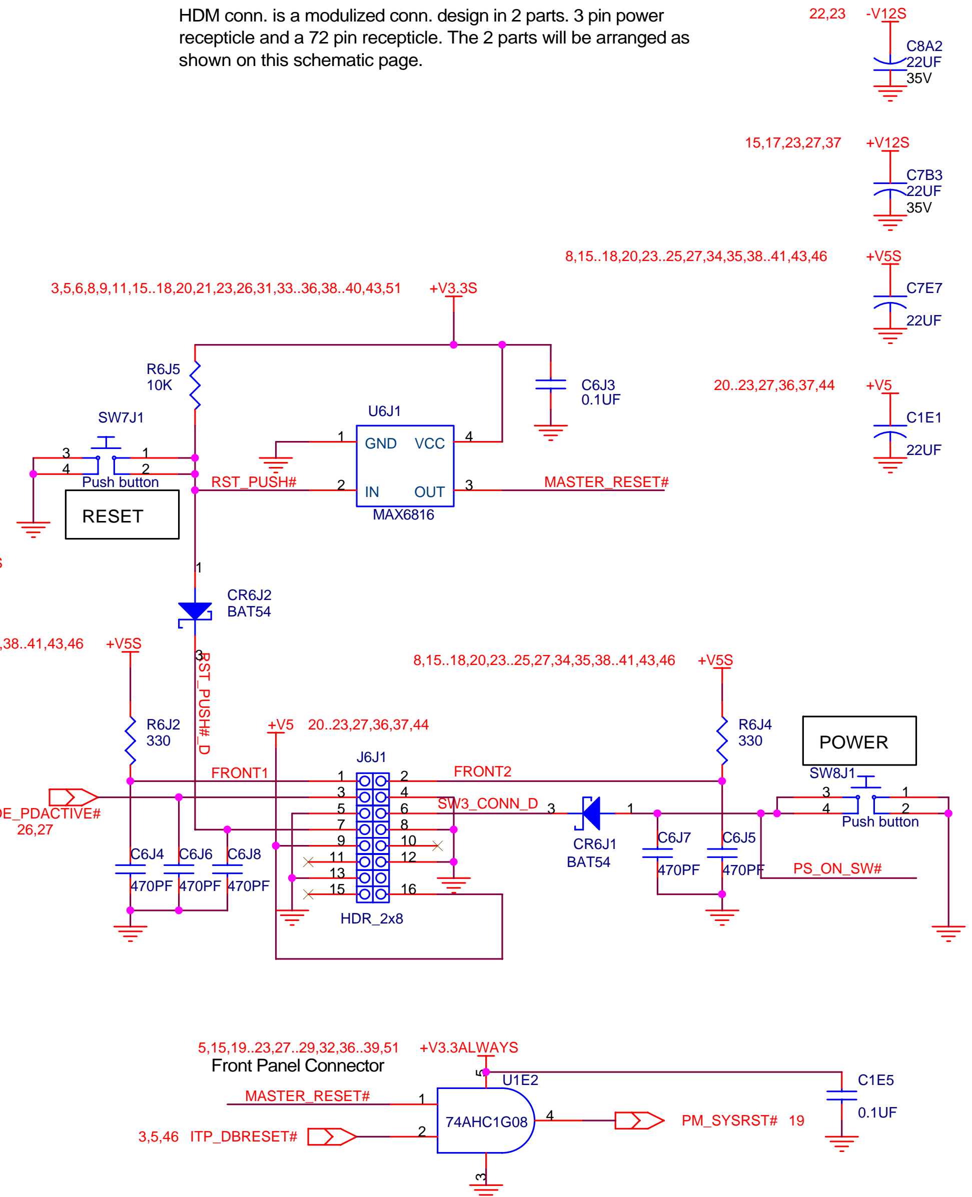
J1B1
A1 A2 A3 A4
D1 D2 D3 D4
F1 F2 F3 F4
16,21,39,41,43 +VDC
3Pin_RECEPTICLE
CON3,RCPTL,TH,700000-667.Normal

4 +V1.8S
J1B2
A1 A2 A3 A4
D1 D2 D3 D4
F1 F2 F3 F4
4,9,15,19,20,46,51 +V1.5S
3,5,6,8,9,11,15..18,20,21,23,26,31,33..36,38..40,43,51
+V3.3S
R1C1 0.002 1%
+V3.3S_TURNER
C1C1 22UF
3Pin_RECEPTICLE
CON3,RCPTL,TH,700000-667.Normal

J1C1
8,15..18,20,23..25,27,34,35,38..41,43,46 +V5S
+V5S_TURNER
R1D1 0.01_1%
32,37 AC_PRESENT#
37,51 GATED_SMC_SHUTDOWN
32,37 SMC_ONOFF#
32,36,37 SMB_SB_CLK
32,36,37 SMB_SB_DATA
32,36,37 SMB_SB_ALRT#
19,20,32,37,38,44 PM_SLP_S4#
19,25,32,37,38,44 PM_SLP_S3#
6,19,37,38 PM_SLP_S1#
39 PWR_PWROK
PS_ON_SW#
8,15..18,20,23..25,27,34,35,38..41,43,46
15,17,23,27,37 +V12S
+V12S_TURNER
R1C4 0.01_1%
+V2.5_TURNER
22,23 -V12S
R1C3 0.01_1%
-V12S_TURNER
+V3.3ALWAYS
5,15,19..23,27..29,32,36..39,51
R1D2 0.002 1%
+V3.3A_TURNER
C1D1 22UF
1.5V_EV 46
A1–A12, B1–B12, C1–C12
F12–F1, E12–E1, D12–D1
72Pin_RECEPTICLE(male)
CON72,RCPTL,TH,700000-668.Normal

J1D1
A1 A2 A3 A4
D1 D2 D3 D4
F1 F2 F3 F4
20..23,27,36,37,44 +V5
+V5_TURNER
R1D3 0.01_1%
+V3.3 15,18..20,23,27,30,32,35,37,38,44
R1D5 0.01_1%
+V3.3_TURNER
3Pin_RECEPTICLE
CON3,RCPTL,TH,700000-667.Normal

HDM conn. is a modulized conn. design in 2 parts. 3 pin power recepticle and a 72 pin recepticle. The 2 parts will be arranged as shown on this schematic page.



5,15,19..23,27..29,32,36..39,51 +V3.3ALWAYS
Front Panel Connector
U1E2
MASTER_RESET#
3,5,46 ITP_DBRESET#
74AHC1G08
PM_SYSRST# 19
C1E5 0.1UF

Title	DC/DC Connector		
Size A	Project: Intel Celeron M / 852GM CRB	Document Number C26116	Rev 4.403
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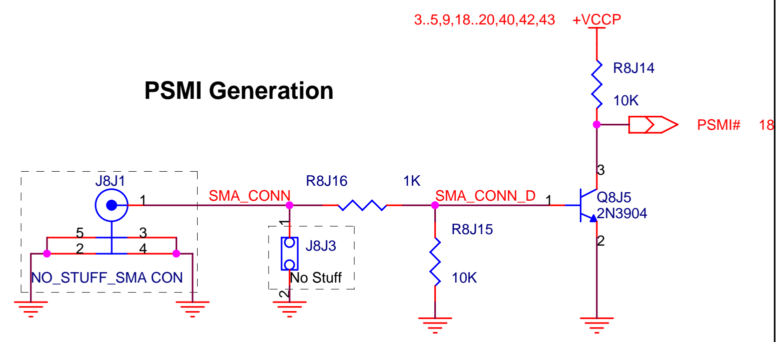

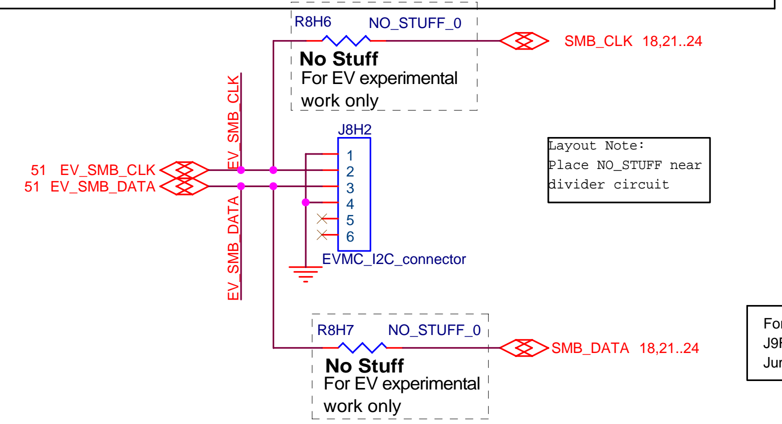

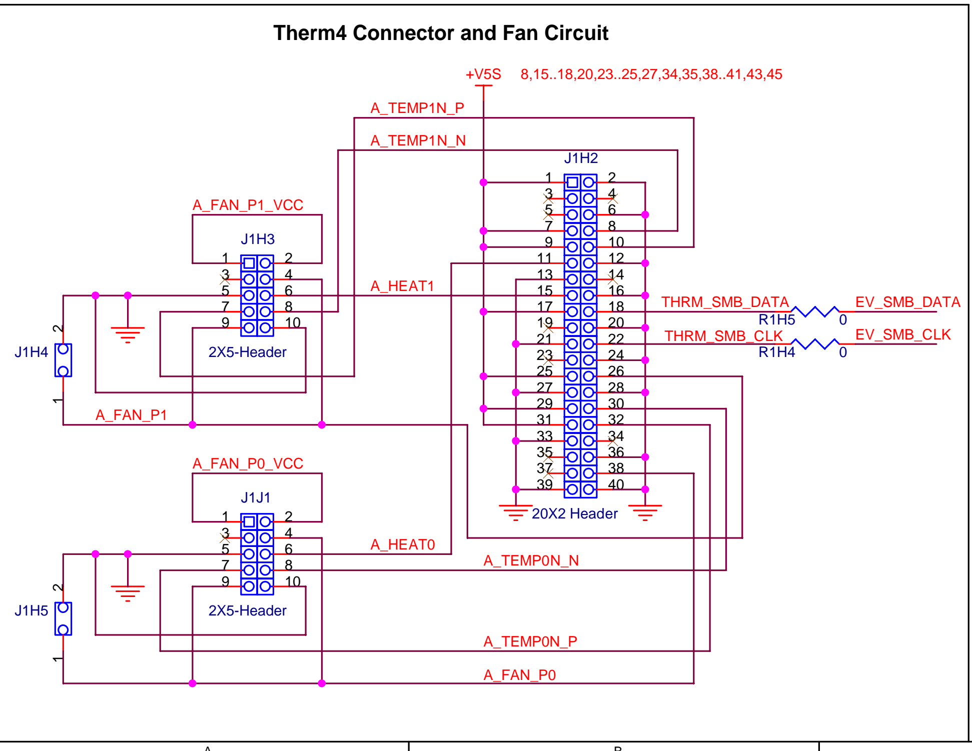

9 +V2.5_GMCH_TXLVDS
F8H1 1.1A
R8H3 0
R8J12 0
GND_DDR
+2.5V_EVMC_IN
+2.5V_EVMC_SENSE
+2.5V_EVMC_GND_SENSE
J8H1
6Pin_HDR

EVMC Schmoo Header

```
Layout Note:
Resistors: R3G4,R6T6,R6P4,R4D1,R6R1,
R5T3,R5R11,R5P8,R4G2,R3G8,R4E3,R6W11,
R3G1,R1C2 should be placed by the risistor
divider networks not near the EVMC slot.
```

```
Layout Note:
Place NO_STUFF near
divider circuit
```

+V1.35S_GMCH 9,43
44 SM_VREF_MCH_EV
8,10 MCH_HLVREF
R3G4 NO_STUFF_0 SM_VREF_MCH_EV_D
R6T6 NO_STUFF_0 MCH_HLVREF_D
43 1.35V_EV
3 H_GTLREF
7,15 DVO_VREF
8,10 MCH_HDVREF
R6P4 NO_STUFF_0 1.35V_EV_D
R4D1 NO_STUFF_0 H_GTLREF_D
R6R1 NO_STUFF_0 DVO_VREF_D
R5T3 NO_STUFF_0 MCH_HDVREF_D
8,10 MCH_HXSWING
R5R11 NO_STUFF_0 MCH_HXSWING_D
11,12,44,51 +V2.5_DDR
3..5,9,18..20,40,42,43 +VCCP
14,44,51 +V1.25S
J9E6 CON3_HDR
MCH_HLVREF_D
DVO_VREF_D
EVMC_AD25
J9F6 CON3_HDR

For J9F6, J9F7, J9F5, J9F2, J9F1
Jumper 1-2 for EV support

VOUT_EVMC_B39 43
R5P8 NO_STUFF_0
1.25V_DDR_EV 44
R4G2 NO_STUFF_267_1%
1.25V_DDR_EV_D
R3G8 NO_STUFF_0
SM_VREF_DIMM_EV_D
SM_VREF_DIMM_EV 44
8,10 MCH_HYSWING
R4E3 NO_STUFF_0
MCH_HYSWING_D

IMVP-4Strap_VID1 39
IMVP-4Strap_VID2 39
IMVP-4Strap_VID3 39
HUB_VREF_ICH_D R6W11 NO_STUFF_0 HUB_VREF_ICH 18
IMVP-4Strap_VID4 39
IMVP-4Strap_VID5 39
2.5V_DDR_EV_D R3G1 NO_STUFF_0 2.5V_DDR_EV 44
J9F7 SM_VREF_MCH_EV_D
EVMC_A21
R9F4 NO_STUFF_0 +VCC_CORE 4,40..42,51
CON3_HDR
J9F5 H_GTLREF_D
HUB_VREF_ICH_D
EVMC_A33
CON3_HDR
J9F2 MCH_HDVREF_D
MCH_HYSWING_D
EVMC_A37
CON3_HDR
J9F1 SM_VREF_DIMM_EV_D
EVMC_A39 +V1.5S
4,9,15,19,20,45,51
CON3_HDR
1.5V_EV_D R1C2 NO_STUFF_0 1.5V_EV 45

Pin	Signal	Signal	Pin
B1	-12V	TRST#	A1
B2	TCK	+12V	A2
B3	GND1	TMS	A3
B4	TDO	TDI	A4
B5	+5V (1)	+5V (7)	A5
B6	+5V (2)	INTA#	A6
B7	INTB#	INTC#	A7
B8	INTD#	+5V (8)	A8
B9	PRSNT1#	RSV3	A9
B10	RSV1	+5V (9)	A10
B11	PRSNT2#	RSV4	A11
B12	GND2	GND14	A12
B13	GND3	GND15	A13
B14	RSV2	RSV5	A14
B15	GND4	RST#	A15
B16	CLK	+5V (10)	A16
B17	GND5	GNT#	A17
B18	REQ#	GND16	A18
B19	+5V (3)	PME#	A19
B20	AD31	AD30	A20
B21	AD29	+3.3V (7)	A21
B22	GND6	AD28	A22
B23	AD27	AD26	A23
B24	AD25	GND17	A24
B25	+3.3V (1)	AD24	A25
B26	C/BE3#	IDSEL	A26
B27	AD23	+3.3V (8)	A27
B28	GND8	AD22	A28
B29	AD21	AD20	A29
B30	AD19	GND18	A30
B31	+3.3V (2)	AD18	A31
B32	AD17	AD16	A32
B33	C/BE2#	+3.3V (9)	A33
B34	GND9	FRAME#	A34
B35	IRDY#	GND19	A35
B36	+3.3V (3)	TRDY#	A36
B37	DEVSEL#	GND20	A37
B38	GND10	STOP#	A38
B39	LOCK#	+3.3V (10)	A39
B40	PERR#	SDONE	A40
B41	+3.3V (4)	SBO#	A41
B42	SERR#	GND21	A42
B43	+3.3V (5)	PAR	A43
B44	C/BE1#	AD15	A44
B45	AD14	+3.3V (11)	A45
B46	GND11	AD13	A46
B47	AD12	AD11	A47
B48	AD10	GND22	A48
B49	GND12	AD09	A49
	KEY		
B52	AD08	C/BE0#	A52
B53	AD07	+3.3V (12)	A53
B54	+3.3V (6)	AD06	A54
B55	AD05	AD04	A55
B56	AD03	GND23	A56
B57	GND13	AD02	A57
B58	AD01	AD00	A58
B59	+5V (4)	+5V (11)	A59
B60	ACK64#	REQ64#	A60
B61	+5V (5)	+5V (12)	A61
B62	+5V (6)	+5V (13)	A62

J9G1 CON120_PCI

EVMC SLOT

J9J2 Jumper for EV support
EVMC_REQ64# J9J2
3,5,45 ITP_DBRESET#

Label on Silk Screen
Do Not Use This Slot
For PCI Operations

Title	EVMC SLOT		
Size A	Project: Intel Celeron M / 852GM CRB	Document Number C26116	Rev 4.403
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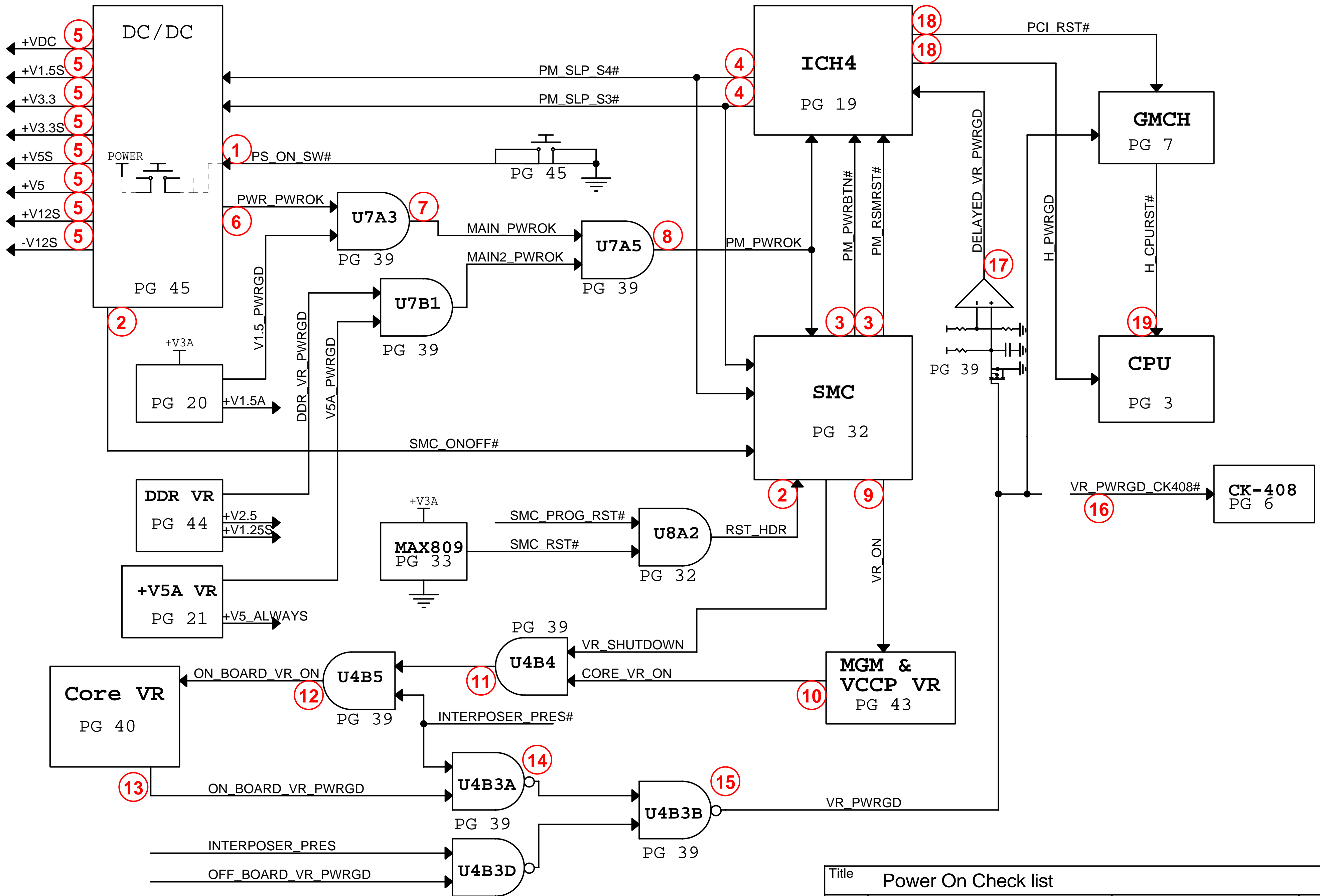
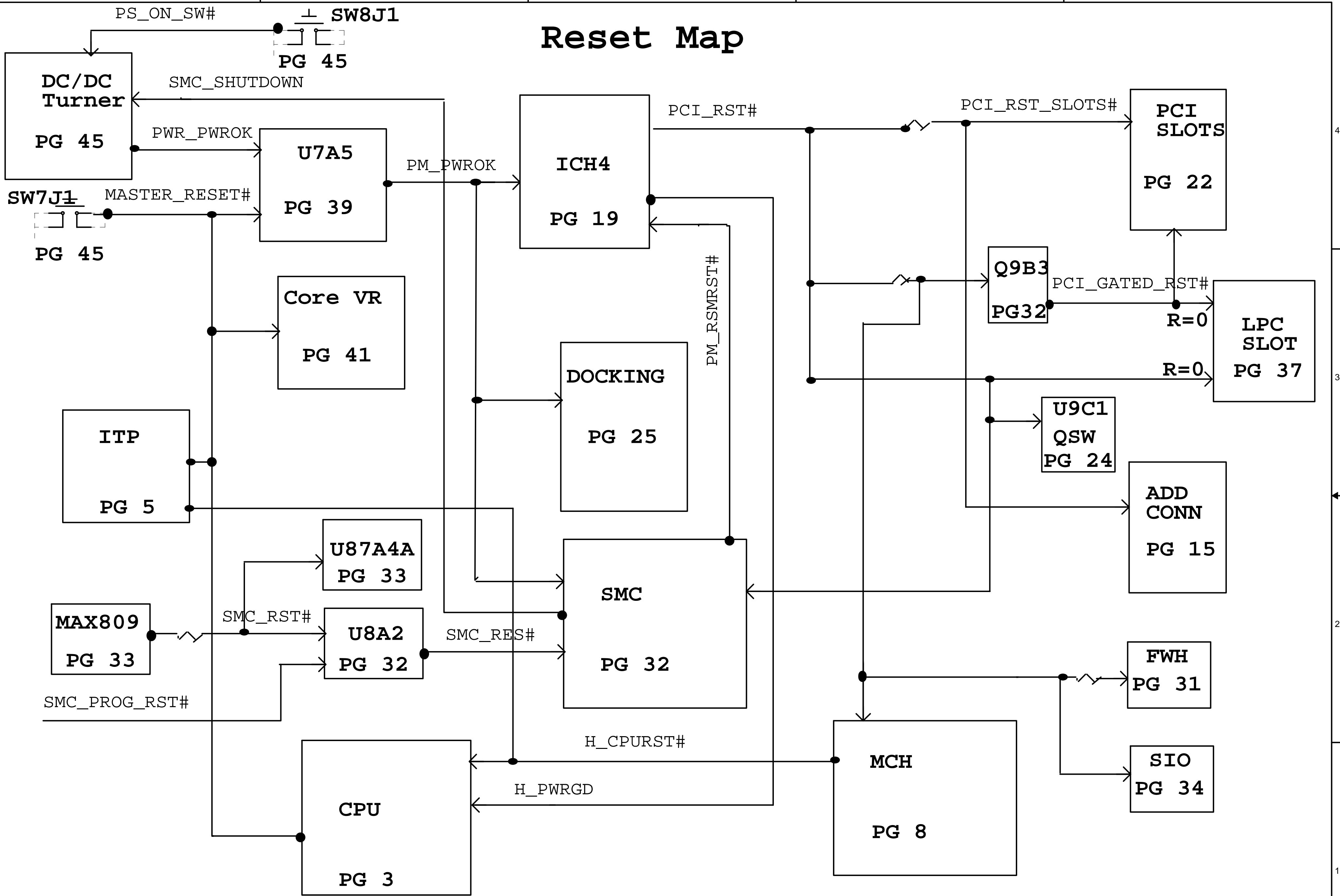
Power On Sequence



Title	Power On Check list		
Size A	Project: Intel Celeron M / 852GM CRB	Document Number C26116	Rev 4.403
Date: Wednesday, January 12, 2005		Sheet 47 of 51	



Title	Reset Map		
Size A	Project: Intel Celeron M / 852GM CRB	Document Number C26116	Rev 4.403
Date: Wednesday, January 12, 2005		Sheet 48 of 51	