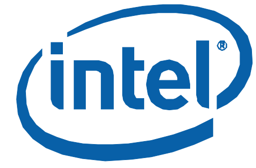
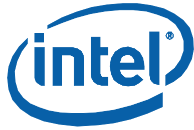


Voltage Regulator-Down (VRD) 11.1

Processor Power Delivery Design Guidelines

September 2009

Document Number: 322172-001



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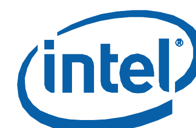

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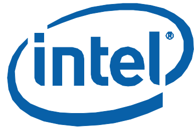

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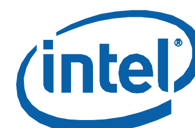

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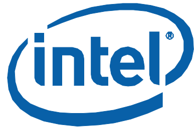

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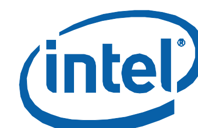

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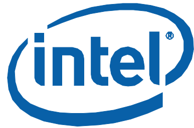

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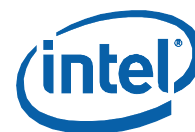

Revision History

Revision Number	Description	Date
-001	• Initial release.	September 2009

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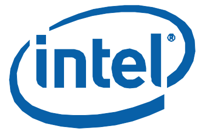
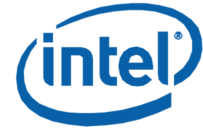




1 VRD 11.1 Common Information

This chapter contains information common to all platforms implementing VRD 11.1. Chapters 2 and beyond contain VRD11.1 information unique to a given platform. Refer to both chapters 1 and the appropriate follow-on chapter relevant to the platform under design.

1.1 Applications

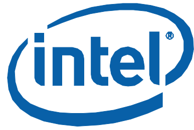
This document defines the power delivery feature set necessary to support Intel processor V_{CC} power delivery requirements for desktop and UP server/workstation computer systems using the LGA1366, LGA1156, and LGA775 sockets. This includes design recommendations for DC to DC regulators, which convert the input supply voltage to a processor consumable V_{CC} voltage along with specific feature set implementation such as thermal monitoring and dynamic voltage identification.

Hardware solutions for the V_{CC} regulator are dependent upon the processors to be supported by a specific motherboard. V_{CC} regulator design on a specific board must meet the specifications of all processors supported by that board. The voltage regulator configuration for a given processor is defined in that processor datasheet. In some instances, this data is not published and the proper mapping of processor to VRD configuration can be found from an authorized Intel representative.

The voltage regulator-down (VRD) designation of this document refers to a regulator with all components mounted directly on the motherboard for intent of supporting a single processor.

VR11.1 incorporates all of the VR11 functions with the following changes:

- Iout feature to support LGA1366, and LGA1156 processors.
- Power on configuration (POC), market segment identification (MSID) functions multiplexed onto VID lines during start up.
- VID_SELECT, VR_FAN and VR10 VID support are removed.
- A Power State Indicator (PSI#) input has been added.
- Single step D-VID added for processor C-state entry and exit.



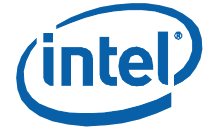
1.2 Terminology

Table 1-1. Feature Support Terminology

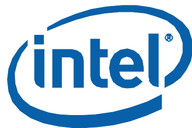
Categories	Description
REQUIRED	An essential feature of the design that must be supported to ensure correct processor and VRD functionality.
EXPECTED	A feature to ensure correct VRD and processor functionality that can be supported using an alternate solution. The feature is necessary for consistency among system and power designs and is traditionally modified only for custom configurations. The feature may be modified or expanded by system OEMs if the intended functionality is fully supported.
PROPOSED	A feature that adds optional functionality to the VRD and, therefore, is included as a design target. May be specified or expanded by system OEMs.
OPTIONAL	A feature that is not required for processor operation; however, specific platforms or OEMs may request this feature or function.

Table 1-2. Glossary

Term	Description
AVP	Adaptive voltage positioning
BJT	Bi-Polar Junction Transistor
CMRR	Common-mode rejection ratio.
DAC	Digital to Analog Converter.
DCR	Direct Current Resistance.
D-VID	Dynamic Voltage Identification. A low power mode of operation where the processor instructs the VRD to operate at a lower voltage.
ESL	Effective series inductance.
ESR	Effective series resistance.
FET	Field Effect Transistor.
FR4	A type of printed circuit board (PCB) material.
HVM	High volume manufacturing.
I_{CC}	Processor current.
Itt	Bus current associated with the V_{TT} supply.
LGA1156 socket	The surface mount Zero Insertion Force (ZIF) socket designed to accept the processors in LGA1156 land grid array packages.



Term	Description
LGA1366 socket	The surface mount Zero Insertion Force (ZIF) socket designed to accept the processors in LGA1366 land grid array packages.
LGA775 socket	The surface mount Zero Insertion Force (ZIF) socket designed to accept the processors in LGA775 land grid array packages.
Loadline	A mathematical model that describes voltage current relationship given system impedance (R_{LL}). The loadline equations is V_{CC} = VID – I*R_{LL}. In this document, the loadline is referenced at the socket unless otherwise stated. The loadline defines the characteristic impedance of the motherboard power delivery circuit to the node of regulation. In conjunction with mid-frequency decoupling, bulk decoupling, and robust power plane routing, design compliance to this parameter ensures that the processor voltage specifications are satisfied.
MLCC	Multi-layer ceramic capacitor.
MOSFET	Metal Oxide Semiconductor Field Effect Transistor.
OCP	Over current protection.
OVP	Over voltage protection.
Processor Datasheet	A document that defines the processor electrical, mechanical, and thermal specifications.
PROCHOT#	Under thermal monitoring, the VRD asserts this processor input to indicate an over-temperature condition has occurred. Assertion of this signal places the processor in a low power state, thereby cooling the voltage regulator.
PWM	Pulse width modulation.
RDS-ON	FET source to drain channel resistance when bias on.
R_{LL}	Loadline impedance. Defined as the ratio: Voltage droop/current step. This is the loadline slope.
RSS	Root Sum Square. A method of adding statistical variables.
Slope	Loadline resistance. See R_{LL}.
Static Loadline	DC resistance at the defined regulation node. Defined as the quotient of voltage and current (V/I) under steady state conditions. This value is configured by proper tuning of the PWM controller voltage positioning circuit.
Thermal Monitor	A feature of the voltage regulator that places the processor in a low power state when critical VRD temperatures are reached, thereby reducing power and VRD temperature.
TOB	Vcc regulation tolerance band. Defines the voltage regulator's 3-σ voltage variation across temperature, manufacturing variation, and aging factors. Must be ensured by design through component selection. Defined at processor maximum current and maximum VID levels.



Term	Description
Transient Loadline	Equal to dV/di or Vdroop/Istep and is controlled by switching frequency, decoupling capacitor selection, motherboard layout parasitics.
UVLO	Under-voltage lock-out
Vcc	Processor core voltage defined in the processor datasheet.
VID	Voltage Identification: A code supplied by the processor that determines the reference output voltage to be delivered to the processor Vcc lands. At zero amperes and the tolerance band at + 3-σ, VID is the voltage at the processor.
VR_TDC	Voltage Regulator Thermal Design Current. The sustained DC current which the voltage regulator must support under the system defined cooling solution.
VRD	Voltage regulator down. A VR circuit resident on the motherboard.
VRM	Voltage regulator module that is socketed to a motherboard.
V_{TT}	Voltage provided to the processor to initiate power up and drive I/O buffer circuits.

1.3 Processor V_{CC} Requirements

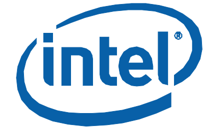
1.3.1 Voltage and Current (REQUIRED)

An 8-bit VID code supplied by the processor to the VRD determines a reference output voltage as described in Section 1.6.1. The loadlines described in subsequent parts of this document show the relationship between V_{CC} and I_{CC} for the processor.

Intel performs testing against multiple software applications and software test vectors to identify valid processor V_{CC} operating ranges. Failure to satisfy the loadline, loadline tolerance band, and overshoot voltage specifications may invalidate Intel warranties and lead to premature processor failure, intermittent system lock-up, and/or data corruption.

1.3.2 Loadline Definitions (REQUIRED)

To maintain processor reliability and performance, platform DC voltage regulation and transient-droop noise levels must always be contained within the Vccmin and Vccmax loadline boundaries (known as the loadline window). Loadline compliance must be ensured across component manufacturing tolerances, thermal variation, and age degradation. Loadline boundaries are defined by the following equations in conjunction with the V_{CC} regulator design parameter values defined in the subsequent sections of this document. Loadline voltage tolerance is defined in Section 1.3.4. In these equations, VID, R_{LL}, and TOB are known. Plotting V_{CC} while varying I_{CC} from 0 A to Iccmax establishes the Vccmax and Vccmin loadlines. Vccmax establishes the maximum DC loadline boundary. Vccmin establishes the minimum AC and DC voltage



boundary. Short transient bursts above the Vccmax loadline are permitted; this condition is defined in Section 1.3.7.

Table 1-3. Loadline Equations

Loadline	Equation
Equation 1: Vccmax Loadline	V_{CC} = VID – (R_{LL}* I_{cc})
Equation 2: Vcctyp Loadline	V_{CC} = VID – TOB – (R_{LL}* I_{cc})
Equation 3: Vccmin loadline	V_{CC} = VID – 2*TOB – (R_{LL}* I_{cc})

Loadline recommendations are established to provide guidance for satisfying processor loadline specifications, which are defined in processor datasheets. Loadline requirements must be satisfied at all times and may require adjustment in the loadline value. The processor loadlines are defined in the applicable processor datasheet.

VRD designs must be loadline compliant across the full tolerance band window to avoid data corruption, system lock-up, and reduced performance. When validating a system's loadline, a single measurement is statistically insignificant and cannot represent the response variation seen across the entire high volume manufacturing population of VRD designs. A typical loadline may fit in the specification window; however, designs residing elsewhere in the tolerance band distribution may violate the specifications. Figure 1-1 Example A shows a loadline that is contained in the specification window and, this single instance, complies with Vccmin and Vccmax specifications. The positioning of this loadline will shift up and down as the tolerance drifts from typical to the design limits. Figure 1-1 Example B shows that Vccmax limits will be violated as the component tolerances shift the loadline to the upper tolerance band limits. Figure 1-1 Example C shows that the Vccmin limits will be violated as the component tolerances shift the loadline to the lower tolerance band limits.

To satisfy specifications across high volume manufacturing variation, a typical loadline must be centered in the loadline window and have a slope equal to the value specified in the subsequent sections of this document that apply to the processor being used. Figure 1-2 Example A shows a loadline that meets this condition. Under full 3-σ tolerance band variation, the loadline slope will intercept the Vccmax loadline (Figure 1-2 Example B) or Vccmin loadline (Figure 1-2 Example C) limits.

Figure 1-1. Examples of High Volume Manufacturing Loadline Violations

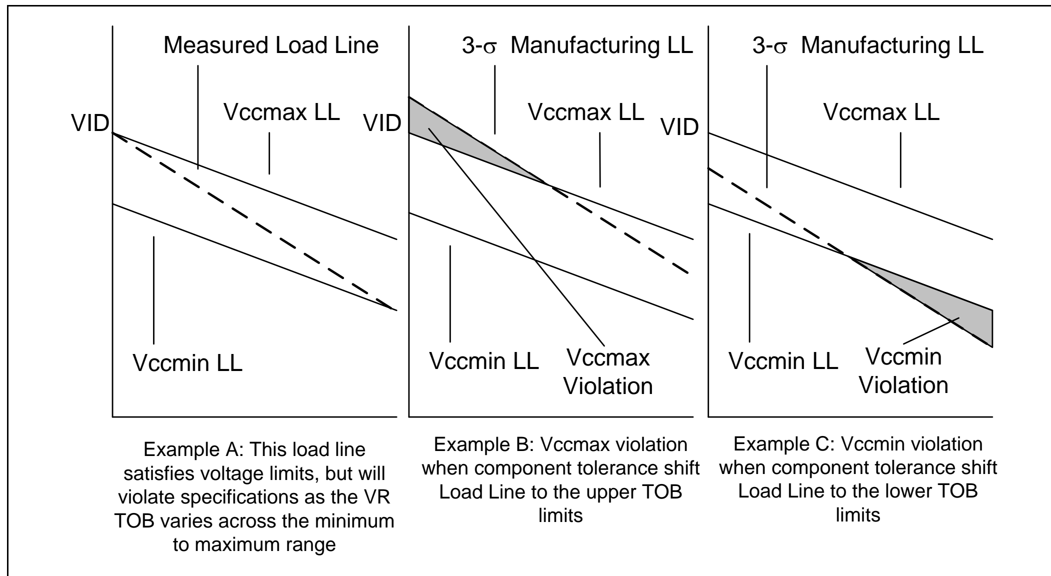
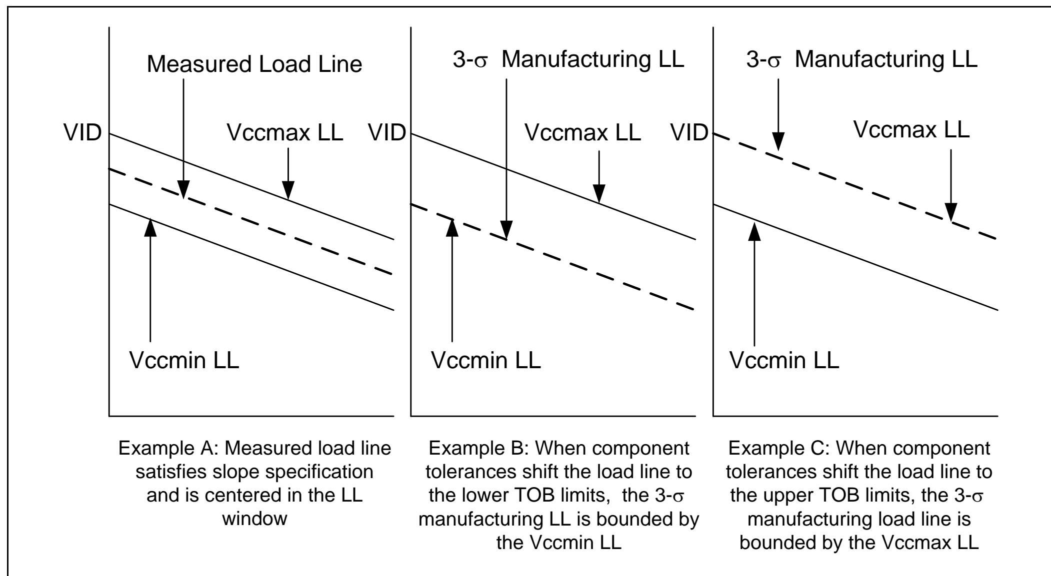


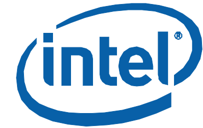
Figure 1-2. High Volume Manufacturing Compliant Loadline



1.3.3 VRD Output Filter (REQUIRED)

Desktop processor voltage regulators include an output filter consisting of large bulk decoupling capacitors to compensate for large transient voltage swings and small value ceramic capacitors to provide mid-frequency decoupling. This filter must be designed to stay within loadline specifications across tolerances due to age degradation, manufacturing variation, and temperature drift.

The VRD output filter needs to be designed for the VR controller that is used. Different controllers can have different filter requirements for meeting the loadline requirements.



1.3.3.1 Bulk Decoupling

Bulk decoupling is necessary to maintain V_{CC} within loadline limits prior to the VRD controller response. Design analysis shows that bulk decoupling requirements will vary with the number of VRD phases and the FET switching frequency.

The D-VID mode of operation is directly impacted by the choice of bulk capacitors and output inductor value in the VRD output filter. It is necessary to minimize V_{CC} settling time during D-VID operation to hasten the speed of core power reduction. The speed of recovery is directly related to the RCL time constant of the output filter. To ensure an adequate thermal recovery time, it is recommended to design the output filter with a minimal output inductor value and a minimal amount of bulk capacitance with minimum ESR, while providing a sufficient amount of decoupling to maintain loadline and ripple requirements. At this time, high-density aluminum poly capacitors with 5 mΩ average ESR have been identified as the preferred solution. Failure to satisfy the V_{CC} settling time requirements defined in Section 1.3.6 may invalidate processor thermal modes.

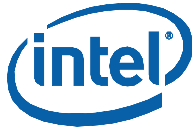
1.3.3.2 Mid-frequency Decoupling

The output filter includes mid-frequency decoupling to ensure ripple and package noise is suppressed to specified levels. Ripple limits are defined in Section 1.3.4.4 and package noise limits are defined in appropriate processor datasheets in the form of a processor loadline.

High Mid-frequency noise and ripple suppression are best minimized by 10 μF, 22 μF, or 47 μF multi-layer ceramic capacitors (MLCCs). It is recommended to maximize the MLCC count in the socket cavity to help suppress transients induced by processor packaging hardware. Remaining MLCCs should be first placed adjacent to the socket edge in the region between the socket cavity and the voltage regulator.

Intel recommends a mid-frequency filter consisting of MLCCs distributed uniformly through the socket cavity region. The cavity-capacitor ESL value needs to be low enough to ensure the VR filter impedance is at or below the loadline target up to F_{break} frequency as described in subsequent sections of this document relating to the processor the VR is being designed for. To ensure functionality with all Intel processors, adoption of the reference solution accompanied by full processor loadline validation is strongly recommended.

Noise is directly dependent upon the processor core frequency, so the filter must ensure adequate decoupling to support all frequencies the board is to support. Impedance measurements as described in subsequent sections of this document relating to the processor the VR is being designed for will help the designer analyze the MLCC decoupling solution.



1.3.4 TOB — Voltage Tolerance Band (REQUIRED)

Processor loadline specifications must be ensured across component process variation, system temperature extremes, and age degradation limits. The VRD topology and component selection must maintain a 3-σ tolerance of the VRD Tolerance Band around the typical loadline. The critical parameters include voltage ripple, VRD controller tolerance, and current sense tolerance under both static and transient conditions. Individual tolerance components will vary among designs; the processor requires only that the total error stack-up stay within the defined VR configuration tolerance band under the conditions defined in the subsequent sections of this document relating to the processor the VR is being designed for.

1.3.4.1 PWM Controller Requirements

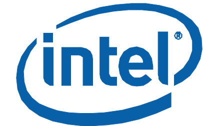
To ensure designers can satisfy the required VRD tolerance band across all modes of operation, PWM controller vendors must publish data and collateral that is critical for satisfying design requirements. This includes support of the following:

- The PWM vendor is to define equations for calculating the VRD TOB with Inductor DCR sensing and resistor sensing. The equation is to include all parameter dependencies such as AVP tolerance, age degradation, thermal drift, sense element DC and AC accuracy, etc under 3-σ variation. These equations are to be published in the PWM controller data sheet. The vendor is to distribute and support a tolerance band calculator that communicates the VRD TOB for each valid VID under each VID table.
- Total PWM controller DC set point accuracy is typically <0.5% over temperature, component age, and lot to lot variation over the 1.0–1.6 V VID range. DAC error may be larger for voltages below 1 V under the assumption that the required Vmin TOB requirements are always satisfied. Typical low voltage accuracy is $\pm$ 5 mV for 0.8 V – 1.0 V VID and $\pm$ 8 mV for 0.5–0.8 V VID. Each vendor is to publish PWM controller DAC accuracy by VID value in the component data sheet.
- The PWM controller must support voltage amplitudes read across sense elements with a DCR of 0.1–2.0 mΩ. PWM controller vendors must define the minimum sense signal voltage necessary to satisfy PWM signal to noise ratio requirements. These requirements are to be published by the vendor in their PWM controller datasheet.

1.3.4.2 Loadline Thermal Compensation (REQUIRED)

Thermal compensation allows the voltage regulator to respond to temperature drift in VRD electrical parameters. It is required to ensure that regulators using inductor current sensing maintain a stable voltage over the full range of load current and system temperatures.

If thermal compensation is not included, the output voltage of the regulator will droop as the resistance of the sense element increases with temperature. With the increased resistance, the regulator falsely detects an increase in load current and regulates to a lower voltage. Thermal compensation prevents this thermally induced voltage droop by adjusting the feedback path based on the temperature of the regulator. This is accomplished by placing a thermistor in the feedback network, tuned with a resistor network to negate the effects of the increased resistance of the sense element.



The thermal compensation circuit is to be validated by running the regulator at the Voltage Regulator Thermal Design Current (VRTDC) and minimum required air flow for 30 to 45 minutes. This is to ensure the board is thermally stable and system temperatures have reached a maximum steady state condition. If the thermal compensation has been properly implemented, the output voltage will only drift 1–2 mV from its coolest temperature condition. If the thermal compensation has not been properly implemented, the voltage can droop in the tens of mV range.

1.3.4.3 Dynamic Voltage Identification (D-VID) TOB

During the D-VID (see Section 1.3.6) mode of operation, VRD tolerance band requirements must be satisfied. Minimum voltage cannot fall below the values predicted by Equation 3 assuming any possible VID setting along with the R_{LL} a TOB values defined in the V_{CC} Regulator Design Parameters Tables in the appropriate subsequent sections of this document. Current values to be used for assessing TOB during dynamic VID should be linearly scaled with voltage. For example, if a 90 A of current is defined at a VID of 1.1 V and the functional VID value is 0.6 V, then the TOB should be calculated assuming (0.6 V/1.1 V) x 90 A = 49 A.

Vccmax VRD TOB can be relaxed during dynamic VID. Positive tolerance variation is permitted and is to be bounded by the voltages predicted by Equation 1, where VID is the standard VID value in regulation when not in the D-VID mode.

1.3.4.4 Ripple Voltage (Required)

To meet tolerance band specifications, high and low frequency ripple is to be limited to 10 mV peak to peak. Measurements must be taken carefully to ensure that superposition of high frequency with low frequency oscillations do not sum to a value greater than 10 mV peak to peak. Measurements are to be taken with a 20 MHz band limited oscilloscope. Ripple testing is to be performed at 5 A minimum loading and at VR TDC. When PSI# is asserted and the VR is operating in the PSI# mode, the ripple voltage can be 20 mV peak to peak.

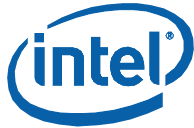
1.3.4.5 Sense Topology Requirements

VRD designers must construct a sense topology that ensures compliance to tolerance band specifications under standard operation and under the D-VID mode of operation. This includes selection of sense elements and supporting components that satisfy tolerance requirements with the chosen PWM controller and ripple amplitude.

Inductor DCR or resistor sensing topologies are required to satisfy tolerance band requirements. Current sensing across MOSFET Rds-on is not suitable for loadline AVP functions due to the large variation in this parameter. Evaluation of this sense method has shown that the TOB requirements cannot be satisfied unless expensive, <10% tolerance MOSFETs are chosen.

1.3.4.6 Error Amplifier Specification (EXPECTED)

The PWM error amplifier should be designed with a sufficient gain bandwidth product to ensure duty cycle saturation does not occur with large signal current transients. Typical target closed loop VR bandwidths of 30–200 kHz (20% of switching frequency target) are expected in VR11.1 system designs. The output of the error amplifier should also have high slew rates to avoid duty cycle saturation. Performance limitations must be included in the VRD TOB equations.



1.3.4.7 PWM Operating Frequency (EXPECTED)

VR11.1 PWM must be designed to work across a wide range of switching frequencies. For the desktop and UP server/workstation market, this can range from 200 kHz up to 1 MHz and corresponding loop bandwidths of 30 kHz to 250 kHz respectively. The tolerance of the PWM oscillator should be <10%. Performance limitations must be included in the VRD TOB equations.

1.3.5 Stability (REQUIRED)

The VRD must be unconditionally stable under all DC and transient conditions across the voltage and current ranges defined in the V_{CC} Regulator Design Parameters Tables in the appropriate subsequent sections of this document. The VRD must also operate in a no-load condition.

1.3.6 Dynamic Voltage Identification (REQUIRED)

1.3.6.1 Dynamic-Voltage Identification Functionality

VRD11.1 architecture includes the Dynamic Voltage Identification (D-VID) feature set, which enables the processor to reduce power consumption and processor temperature. Reference VID codes are dynamically updated by the processor to the VRD controller using the VID bus when a low power state is initiated. VID codes are updated sequentially in either 12.5 mV or 6.25 mV steps. The 6.25 mV steps can be transmitted every 1.25 μs and 12.5 mV steps can be transmitted every 2.5 μs until the final voltage code is encountered. The VR should settle within 5 mV of the final value within 15 μs for a D-VID event over 50 mV and within 5 μs for events less than 50 mV in magnitude.

LGA775 processors that will use VR11.1 based PWM controllers will have single step upward DVID jumps on the order of 100s of mV up to a maximum of 250 mV . Downward DVID jumps should decay with the processor load current, the VR is not required to pull down the output voltage. If the PWM receives a single step upward DVID jump, it should regulate to the new output voltage target with a minimum slew rate of 10 mV/us. The PWM should not false trip the OCP or OVP monitors during walking or single step DVID events. The output voltage shall settle to within 5 mV of the target voltage in less than 8 us. For the 250 mV step, the VR must complete the transition in 25 us (transition time) + 8 us (settling time) = 33 us total time.

During a D-VID event, the processor load may not be capable of absorbing output capacitor energy when the VID reference is lowered. As a result, reverse current may flow into the AC-DC regulator's input filter, potentially charging the input filter to a voltage above the over voltage value. Upon detection of this condition, the AC-DC regulator will react by shutting down the AC-DC regulator supply voltage. The VRD and AC-DC filter must be designed to ensure this condition does not occur. In addition, reverse current into the AC-DC regulator must not impair the operation of the VRD, the AC-DC supply, or any other part of the system.

Under all functional conditions, including D-VID, the V_{CC} supply must satisfy loadline and overshoot constraints to avoid data corruption, system lock-up events, or system blue-screen failures.

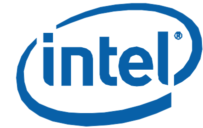
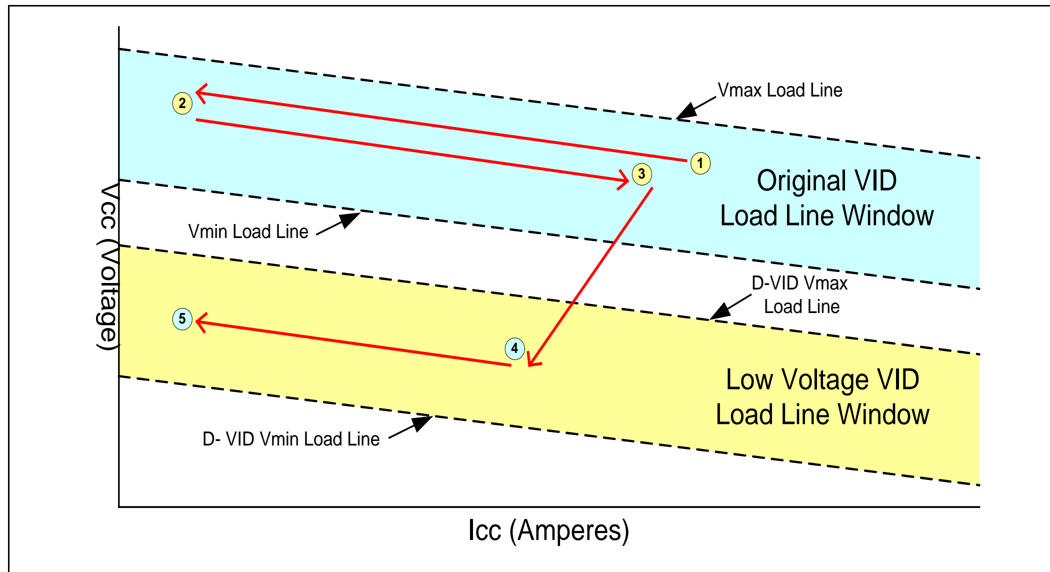


Figure 1-3. Processor D-VID Loadline Transition States

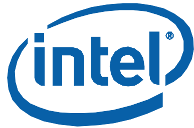


1.3.6.2 D-VID Validation

Intel processors are capable of generating numerous D-VID states and the VRD must be designed to properly transition to and function at each possible VID voltage. However, exhaustive validation of each state is unnecessary and impractical. Validation can be simplified by verifying the VRD conforms to socket loadline requirements, tolerance band specifications, and D-VID timing requirements. Then, by default, each processor D-VID state will be valid. The key variables for V_{CC} under D-VID conditions are processor loading, starting VID, ending VID, and V_{CC} slew rate. The V_{CC} slew rate is defined by VRD bulk decoupling, the output inductors, the switching FET resistance and the processor load. This indicates that the V_{CC} slewing will have an exponential behavior, where the response to code 'n+1' takes longer to settle than code 'n'. As a result, a test from maximum to minimum and from minimum to maximum will be sufficient to ensure slew rate requirements and VID code regulation.

To ensure support for any valid VID reference, testing should be performed from the maximum table entry of 1.6 V to the minimum VID table value. For VR11.1, use 0.5 V for the minimum value. The VRD must ensure that the full table transition occurs within 15 microseconds of the final VID code transmission. Slew rate timing is referenced from 0.4 V on the rising edge of the initial VID code to the time the final voltage is settled within 5 mV of the final V_{CC} value. Intel testing has noted a 10% change to the V_{CC} slew rate between VRD no load (5 A) and full load (VR TDC) conditions. For this reason, the V_{CC} slewing must be tested under both loading conditions.

During the D-VID test defined in the previous paragraph, V_{CC} droop and undershoot amplitudes must be limited to avoid processor damage and performance failures. If the processor experiences a voltage undershoot due to D-VID transitions, an application initiated di/dt droop can superimpose with this event and potentially violate minimum voltage specifications. Droop during this D-VID test must be limited to 5 mV. This value was derived by calculating VRD tolerance band improvements at the low D-VID current and voltage values.



1.3.6.2.1 VR11.1 Validation Summary for 6.25 mV VID Resolution

This exercise tests VRD11.1 functionality with 6.25 mV VID resolution. Consult Figure 1-4 and Figure 1-5 for graphic representation of validation requirements.

1. Constraints:
    a. 1.1 V ±5 mV transition must occur within 233.75 μs (see Figure 1-4).
    b. Start time is referenced to 0.4 V on the rising edge of the initial D-VID code.
    c. End time is referenced to the steady state Vcc voltage after the final D-VID code.
    d. Undershoot during maximum to minimum VID transition must be limited to 5 mV. This 5 mV is included within the ±5 mV tolerance on the final VID value defined under test condition a.
    e. Care must be taken to avoid motherboard and component heat damage resulting from extended operations with high current draw.

2. Validation exercises:
    a. D-VID transition must be validated against above constraints from a starting VID of 1.6 V to an ending VID of 0.5 V with an applied 5 A Load.
    b. D-VID transition must be validated against above constraints from a starting VID of 1.6 V to an ending VID of 0.5 V with an applied VR TDC Load.
    c. D-VID transition must be validated against above constraints from a starting VID of 0.5 V to an ending VID of 1.6 V with an applied 5 A Load.
    d. D-VID transition must be validated against above constraints from a starting VID of 0.5 V to an ending VID of 1.6 V with an applied VR TDC Load.

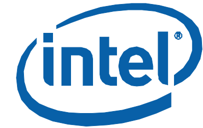


Figure 1-4. VRD11.1 D-VID Transition Timing States (6.25 mV VID Resolution)

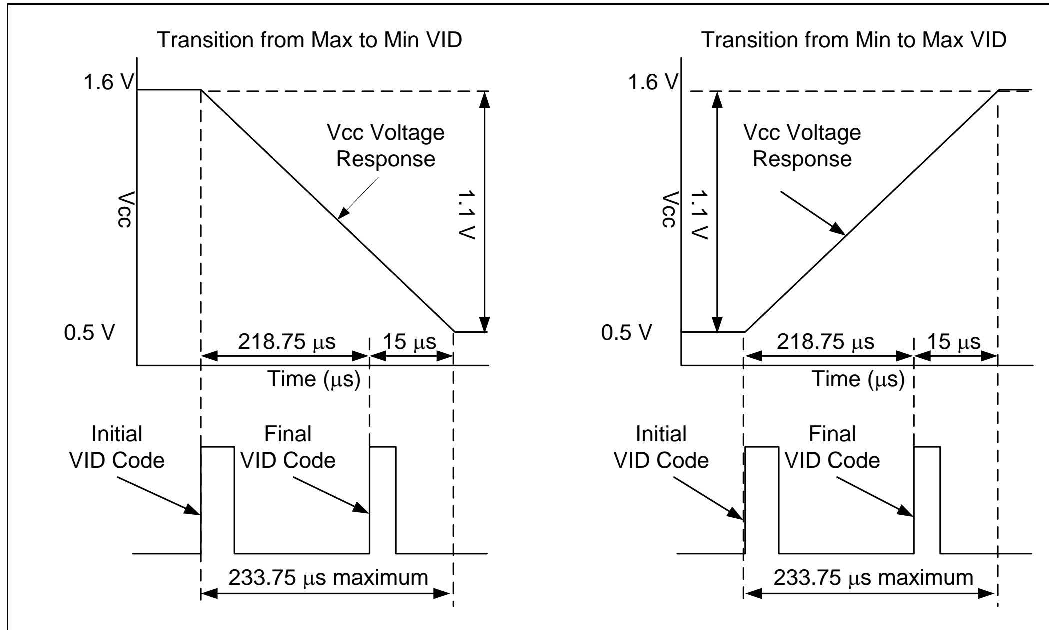
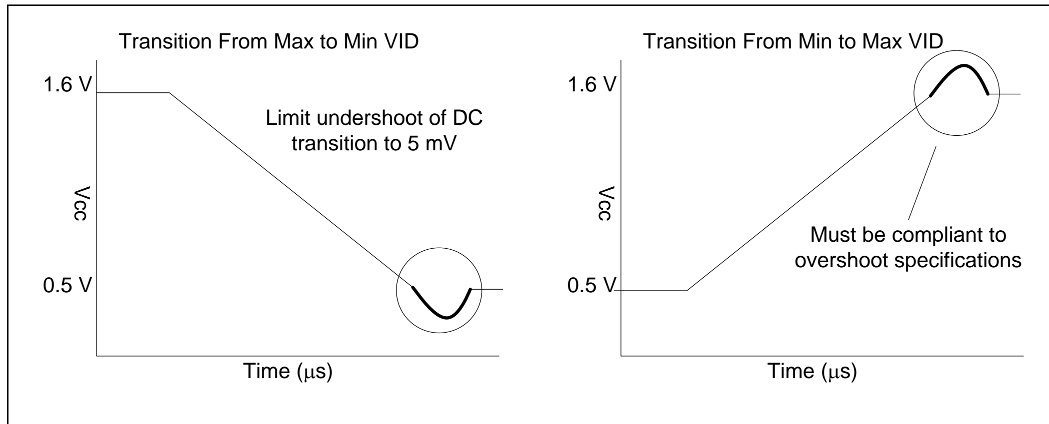
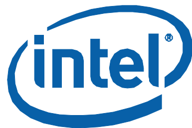


Figure 1-5. Overshoot and Undershoot During Dynamic VID Validation



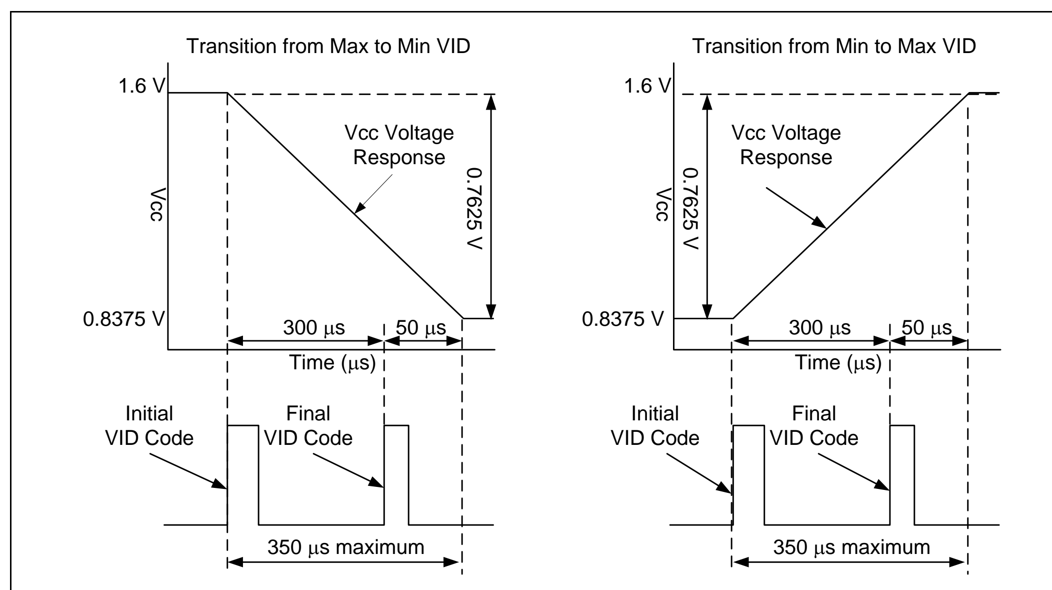


1.3.6.2.2 VR11 Validation Summary for 12.5 mV VID Resolution

This exercise tests VRD11 functionality with 12.5 mV VID resolution. Consult Figure 1-6 and Figure 1-7 for graphic representation of validation requirements.

1. Constraints:
    a. 0.7625 V ±5 mV transition must occur within 350 µs (see Figure 1-6).
    b. Start time is referenced to 0.4 V on the rising edge of the initial D-VID code.
    c. End time is referenced to the steady state V_{CC} voltage after the final D-VID code.
    d. Undershoot during maximum to minimum VID transition must be limited to 5 mV. This 5 mV is included within the ±5 mV tolerance on the final VID value defined under test condition a.
    e. Care must be taken to avoid motherboard and component heat damage resulting from extended operations with high current draw.
2. Validation exercises
    a. D-VID transition must be validated against above constraints from a starting VID of 1.6 V to an ending VID of 0.8375 V with an applied 5A Load.
    b. D-VID transition must be validated against above constraints from a starting VID of 1.6 V to an ending VID of 0. 8375 V with an applied VR TDC Load.
    c. D-VID transition must be validated against above constraints from a starting VID of 0.8375 V to an ending VID of 1.6 V with an applied 5 A Load.
    d. D-VID transition must be validated against above constraints from a starting VID of 0.8375 V to an ending VID of 1.6 V with an applied VR TDC Load.

Figure 1-6. VRD11 DVID Transition Timing States (12.5 mV VID Resolution)



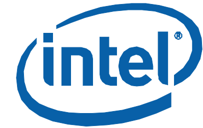
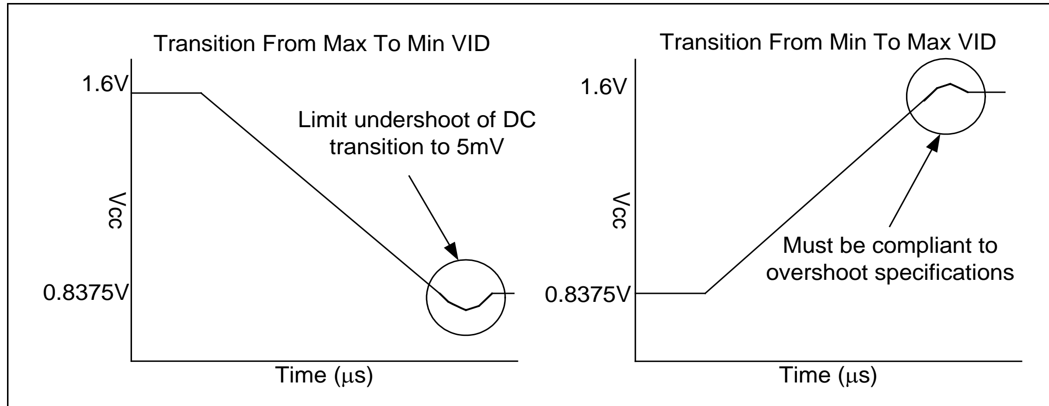


Figure 1-7 Overshoot and Undershoot during Dynamic VID Validation



1.3.7 Processor V_{CC} Overshoot (REQUIRED)

1.3.7.1 Specification Overview

Intel desktop processors in VRD11.1 systems are capable of tolerating short transient overshoot events above VID on the V_{CC} supply that will not impact processor lifespan or reliability. Maximum processor V_{CC} overshoot, V_{OS}, cannot exceed VID+V_{OS_MAX}. Overshoot duration, T_{OS}, cannot stay above VID for a time more than T_{OS_MAX}. See Table 1-4 and Table 1-5 for details.

Table 1-4. V_{CC} Overshoot Terminology Table

Parameter	Definition
V_{OS}	Measured peak overshoot voltage
V_{OS_MAX}	Maximum specified overshoot voltage allowed above VID
T_{OS}	Measured overshoot time duration
T_{OS_MAX}	Maximum specified overshoot time duration above VID
Vzc	Zero current voltage: The voltage where the measured loadline intercepts the voltage axis
Vzco	Zero current offset from VID: Vzco = VID – Vzc

Table 1-5. V_{CC} Overshoot Specifications

Parameter	Specification
VOS_MAX	50 mV
TOS_MAX	25 µs
VOS	Maximum = VID + VOS_MAX
TOS	Maximum = TOS_MAX

Maximum overshoot is validated by monitoring the voltage across the recommended test lands (defined in Section 1.3.2) while applying a current load release across the

socket V_{CC} and V_{SS} land field. Amperage values for performing this validation under each VRD design configuration are identified in Table 1-6. The platform voltage regulator output filter must be stuffed with a sufficient quality and number of capacitors to ensure that overshoot stays above VID for a time no longer than T_{OS_MAX} and never exceeds the maximum amplitude of VID+V_{OS_MAX}. Measurements are to be taken using an oscilloscope with a 20 MHz bandwidth. Boards in violation must be redesigned for compliance to avoid processor damage.

Table 1-6. Intel® Processor Current Release Values For Overshoot Testing

VR Configuration	Starting Current	Ending Current	Dynamic Current Step
1156_VR_CONFIG_09A	55 A	5 A	50 A
1156_VR_CONFIG_09B	80 A	5 A	75 A
1366_VR_CONFIG_08B	105 A	5 A	100 A
775_VR_CONFIG_04A	60 A	5 A	55 A
775_VR_CONFIG_04B	100 A	5 A	95 A
775_VR_CONFIG_05A	70 A	5 A	65 A
775_VR_CONFIG_05B	100 A	5 A	95 A
775_VR_CONFIG_06	55 A	5 A	50 A

To prevent processor damage, VRD designs should comply to overshoot specifications across the full loadline tolerance band window (see Section 1.3.2). When validating a system's overshoot, a single measurement is statistically insignificant and cannot represent the response variation seen across the entire high volume manufacturing population of VRD designs. A typical design may fit in the loadline window; however designs residing elsewhere in the tolerance band distribution may violate the V_{CC} overshoot specifications. Figure 1-9 provides an illustration of this concept. A typical board will have the V_{CC} zero current voltage (Vzc) centered in the loadline window at VID-TOB; for this example consider waveform A and assume TOB is 19 mV. Now assume that the VRD has maximum overshoot amplitude of VOS_MAX = 50 mV above VID. Under this single case, the overshoot aligns with the specification limit and there is zero margin to violation. Under manufacturing variation Vzc can drift to align with VID (waveform B). This drift will shift the overshoot waveform by the same voltage level. Since waveform A has zero overshoot amplitude margin, this increase in Vzc due to manufacturing drift will yield a 19 mV overshoot violation which will reduce the processor life span. To address this issue in validation, a voltage margining technique can be employed to ensure overshoot amplitudes stay below a safe value. This technique translates the specification baseline from VID to a VRD validation baseline of Vzc + VOS_MAX, which defines a test limit for specification compliance across the full TOB range:

Equation 4. Overshoot Voltage Limit

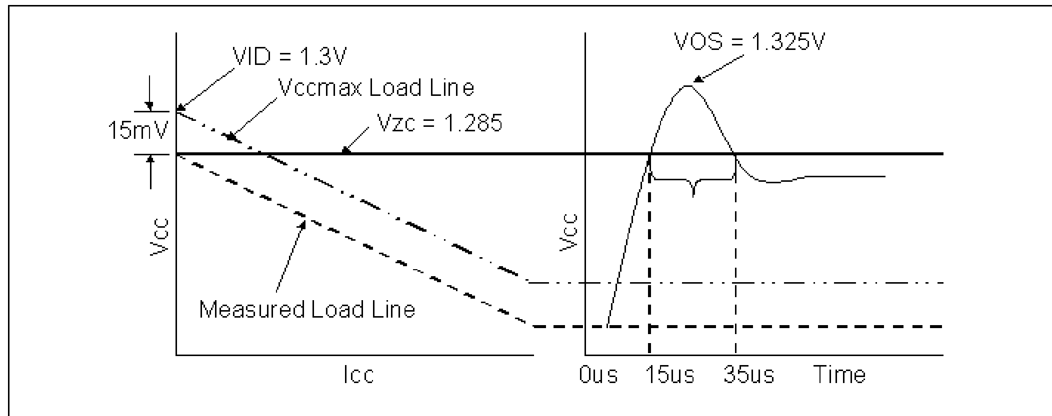
$$V_{OS} < Vzc + VOS_MAX$$

This equation is to be used during validation to ensure overshoot is in compliance to specifications across high volume manufacturing variation. In addition, the overshoot duration must be reference to Vzc and cannot exceed this level for more than 25 µs.

Figure 1-8. Graphical Representation of Overshoot Parameters

Figure 1-9. Processor Overshoot in High Volume Manufacturing

Figure 1-10. Example V_{CC} Overshoot Waveform



1.3.8 Example: Socket V_{CC} Overshoot Test

To pass the overshoot specification, the amplitude constraint of Equation 4 and time duration requirement of TOS_MAX must be satisfied. This example references Figure 1-10.

Amplitude Test Constraint: Overshoot amplitude, VOS, must be less than Vzc + VOS_MAX

Input parameters

- VOS= 1.325 V – Obtained from direct measurement
- V_{ZC} = 1.285 V – Obtained from direct measurement
- VOS_Max = 0.050 V – An Intel specified value

Amplitude Analysis

- V_{ZC} + VOS_MAX = 1.285 V + 0.050 V = 1.335 V
- VOS = 1.325 < 1.335 V

Amplitude Test Satisfied

Time Duration Test Constraint: Overshoot duration above Vzc must be less than 25 µs

Input Parameters

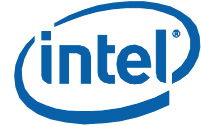
- Initial crossing of overshoot: 15 µs – Obtained from direct measurement
- Final crossing of overshoot: 35 µs – Obtained from direct measurement
- TOS_MAX = 25µs – An Intel specified value

Overshoot Duration Analysis

- TOS = Final Crossing of Vzc – Initial Crossing of Vzc
- TOS = 35 µs – 15 µs = 20 µs < 25 µs = TOS_MAX

Time duration test passed

Amplitude and Time Duration Tests Passed => Overshoot specification is satisfied.



1.4 Power Sequencing (REQUIRED)

VR11.1 features a power sequence that is compatible with both VR11 and VR11.1 processors.

Desktop and UP server/workstation VR11.1 systems use a pull-up resistor tied to the V_{TT} supply as an enable signal. Once the PWM V_{CC} voltage is above its under voltage lockout (UVLO) threshold, out of configuration states such as reset, and a valid enable signal is received, the PWM is to initiate the start up sequence with TD1.

The PWM should ramp V_{CC} to the default 'Vboot' value and start a timer. It will remain at the Vboot voltage during Tc and then read in the VID lines and ramp to the programmed VID voltage. See Figure 1-11 timing diagram for details on the power-on sequence requirements.

1.4.1 VR_ENABLE

To ensure the that V_{TTA} and V_{TTD} are valid prior to processor V_{CC}, Vtt_PG (the V_{TTA}/V_{TTD} regulator power good output) should be used as an enable signal for VRD11.1. See Figure 1-11.

1.4.2 Vboot Voltage Level (REQUIRED)

Vboot is a default power-on V_{CC} value. Upon detection of a valid V_{TT} supply (VTTPWRGOOD asserted), the PWM controller is to regulate the VRD to this value until VID codes are read. The Vboot voltage is 1.1 V. During Vboot, the output should operate with a loadline as if the VID=1.1 V.

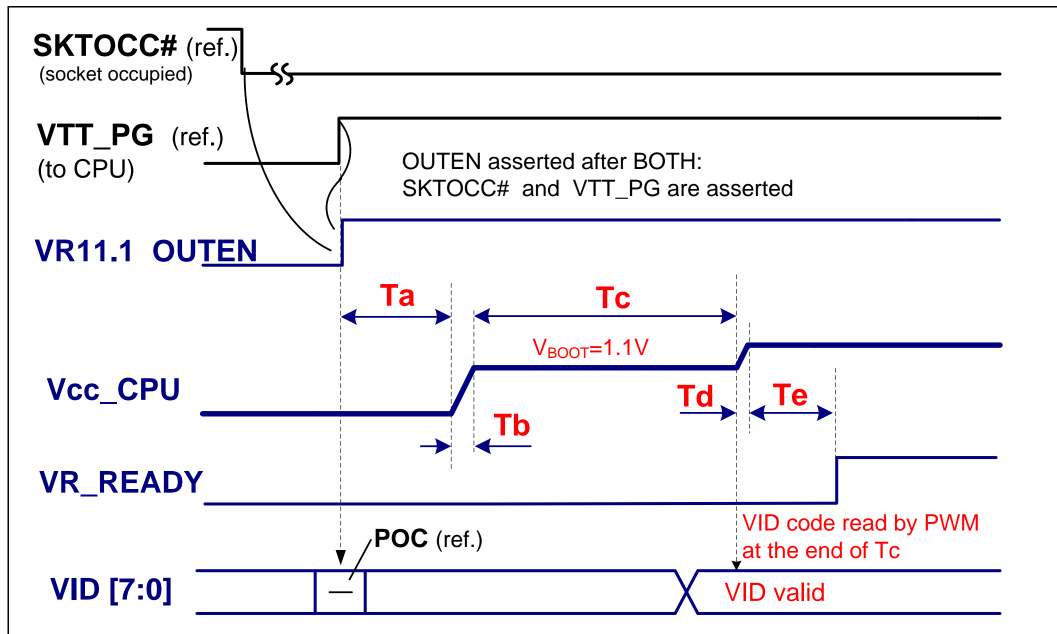
1.4.3 Under Voltage Lock Out (UVLO) (REQUIRED)

The PWM IC should detect its voltage rail and remain in the disabled state until a valid voltage level is available or reached. The voltage level is typically 3.0 V in a 3.3 V system, 4.0 V in a 5 V system or 7-8 V in a 12 V system. Ultimately the PWM vendor should set the level to meet his market segment requirements. However, the PWM and MOSFET driver components should coordinate start up such that both the PWM input voltage rail and power conversion input voltage rail (typically +12 V) of the buck converter are both up and valid prior to enabling the PWM function. The PWM and MOSFET driver component combinations need to be tolerant of any sequencing combination of 3.3 V, 5 V or 12 V input rails. If the PWM IC voltage rail, MOSFET driver voltage rail or power conversion rail fall below the UVLO thresholds, the PWM should shut down in an orderly manner and restart the start up sequence.

1.4.4 Soft Start (SS) (REQUIRED)

The PWM controller should have a soft start function to limit inrush current into the output capacitor bank and prevent false over current protection (OCP) trips. The soft start should have a ramp of 500 µs as an internally programmed default. A SS pin for user programmability of SS ramp to extend the ramp to 1–5 ms is required. Consult Td and Te parameters in Figure 1-11 for further details.

Figure 1-11. Start Up Sequence (Timing is not to scale, details in Table 1-7)



1.4.5 Power-off Timing Sequence (REQUIRED)

There can be a normal or an abnormal power-off, the typical cases are:

1. Normal power-off by de-asserting OUTEN (non-latching)
2. Abnormal power-off due to:
    - PWM _Vcc falling out of regulation, below its UVLO threshold
    - VID Off-code sent by CPU
    - OVP condition
    - OCP condition

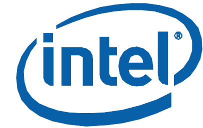


Figure 1-12 Power-off timing sequence (Timing is not to scale, details in Table 1-7)

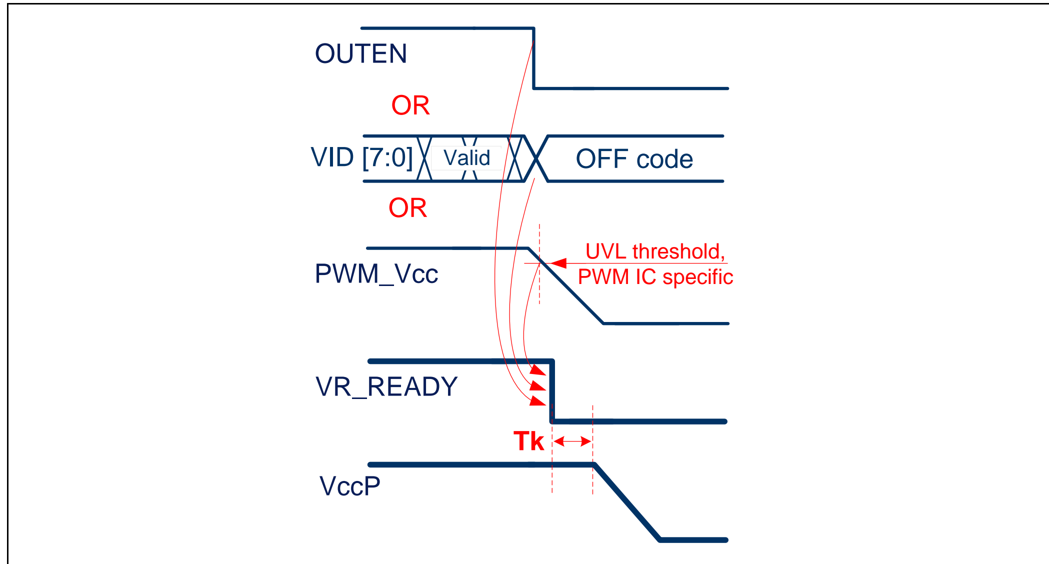
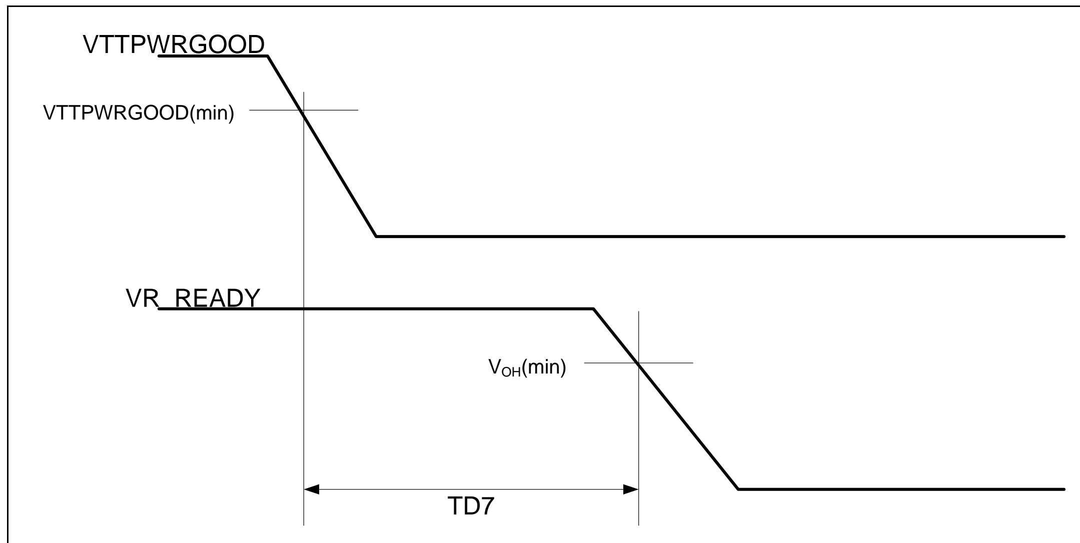


Figure 1-13. TD7 Reference Levels



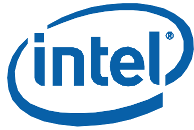
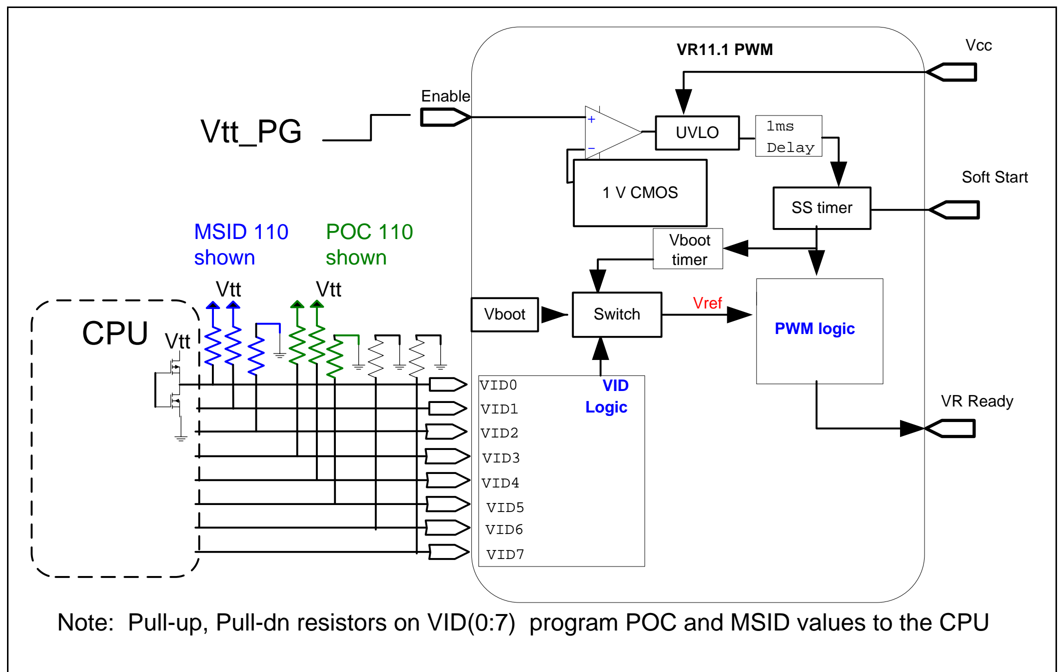


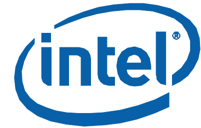
Table 1-7. Start Up Sequence Timing

Start up Delay Parameters			
Parameter	**Minimum**	**Typical, Default**	**Maximum**
Ta	0 ms	-	5 ms
Tb	50 µs	500 µs	5 ms
Tc	50 µs	-	3 ms
Td	0 µs	250 µs	3.5 ms
Te	50 µs	-	3 ms
Tk	0 ms	-	500 ms
TD7	0 ms	-	1 ms

Figure 1-14. Start Up Sequence Functional Block Diagram



NOTE: MSID and POC settings shown are for example only.



1.5 VRD Current Support (Required)

System boards supporting Intel processors must have voltage regulator designs compliant to electrical and thermal standards defined in the V_{CC} Regulator Design Parameter table in the section specific for the processor being supported. This includes full electrical support of Iccmax specifications and robust cooling solutions to support defined thermal design current (VR TDC) indefinitely within the envelope of system operating conditions. This includes regulator layout, processor fan selection, ambient temperature, chassis configuration, etc. Consult the V_{CC} Regulator Design Parameter table in the section specific for the processor being supported for processor V_{CC} and V_{TT} current limits.

Intel processor VR TDC is the sustained (DC equivalent) current that is to be used for voltage regulator thermal design with supporting Thermal Monitor circuitry (see Section 1.9.2). At VR TDC, components such as switching FETs and inductors reach maximum temperature, heating the motherboard layers and neighboring components to the pass/fail boundary of thermal limits. Thermal analysis must include current contributions of both the V_{CC} and V_{TT} regulators. In some instances the processor VRD will also power other motherboard components. Under this condition the VRD will supply current above the VR TDC limits; system designers must budget this additional current support in final VRD designs while remaining compliant to electrical and thermal specifications.

To avoid heat related failures, desktop computer systems should be validated for thermal compliance under the envelope of system operating conditions.

1.5.1 Phase Count Requirement

The PWM controller will be used in DC-DC converters that support processors from 30 A to 145 A TDC. It is expected that the PWM chip manufacturer will determine the optimal number of phases for a low cost design and allow for flexible implementations to meet various market segment requirements.

1.6 Control Inputs to VRD

1.6.1 Voltage Identification (VID [7:0]) (REQUIRED)

The VRD must accept an 8-bit code transmitted by the processor to establish the reference V_{CC} operating voltage.

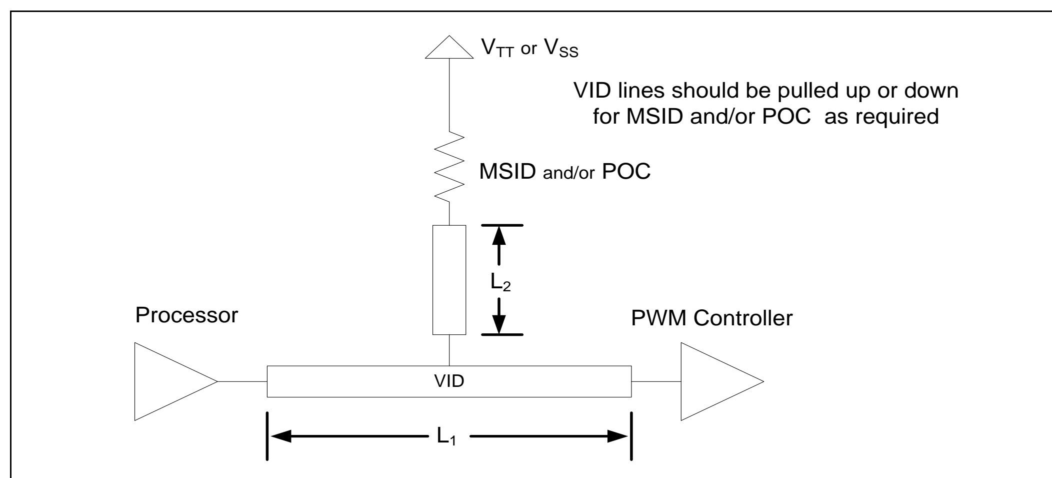
When an 'OFF' VID code appears at the input to the PWM controller, the DC-DC is to turn off the V_{CC} output within 0.5 seconds and latch off until power is cycled.

While operating in the D-VID mode, Intel processors can transmit VID codes across the eight bit bus with a data transmission rate of up to 1.25 µs. To properly design this bus against timing and signal integrity requirements (Table 1-8), the following information is provided. The VID buffer circuit is a push-pull CMOS circuit configuration. The worst-case settling time requirement for code transmission at each load is 200 nanoseconds, including line-to-line skew. VRD controller VID inputs should contain circuitry to detect a change and prevent false tripping or latching of VID codes during this 200-nanosecond window.

Intel recommends use of the D-VID bus topology described in Figure 1-15 and Table 1-8. Under these conditions, traces can be routed with micro strip, strip line, or a combination with a maximum of four layer transitions. The main trace length can vary between ½ inch and 15 inches with a maximum recommended line to line skew of 1 inch. Pull-up/down resistors are only necessary for MSID and/or POC requirements.

Some designs may require additional VID bus loads. In this case, care should be taken to design the topology to avoid excessive undershoot and overshoot at each load. Failure to comply with these limits may lead to component damage or cause premature failure. The responsible engineer must identify minimum and maximum limits of each component and design a topology that ensures voltages stay within these limits at all times.

Figure 1-15. D-VID Bus Topology



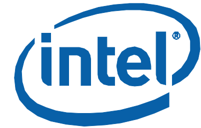


Table 1-8. Interface Signal Parameters

Design Parameter	Minimum	Typical	Maximum
VID Bus Voltage	—	V_{TT} [1]	—
Voltage Limits At Processor VID Lands	- 0.100 V	—	V_{TT} [2]
V_{IH}	0.8 V	—	—
V_{IL}	—	—	0.3 V
L_1, VID trace length	0.5 inch	—	15 inches
L_2, V_{TT} Stub Length	0 inch	—	1 inch
VID trace length skew	—	1.0 inch	—
VID trace width	5 mils	—	—
VID trace separation	5 mils	—	—
MSID and/or POC Resistors (R_{TT}) [4]	950 Ω	1 kΩ	1050 Ω
Processor CMOS driver leakage current	20 μA	—	200 μA

NOTES:

1. V_{TT} specifications are listed in the processor specific sections of this document
2. Consult the processor datasheet for signal overshoot limits
3. VRD11.1 PWM leakage should be 10 μA maximum.
4. Not Applicable to LGA775 designs

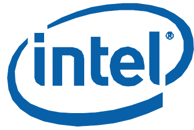
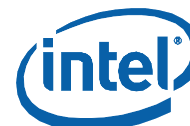


Table 1-9. VR11.1 VID Table (Same as VR11.0 VID Table)

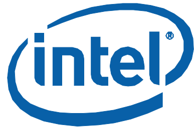
VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
0	0	0	0	0	0	0	0	OFF
0	0	0	0	0	0	0	1	OFF
0	0	0	0	0	0	1	0	1.60000
0	0	0	0	0	0	1	1	1.59375
0	0	0	0	0	1	0	0	1.58750
0	0	0	0	0	1	0	1	1.58125
0	0	0	0	0	1	1	0	1.57500
0	0	0	0	0	1	1	1	1.56875
0	0	0	0	1	0	0	0	1.56250
0	0	0	0	1	0	0	1	1.55625
0	0	0	0	1	0	1	0	1.55000
0	0	0	0	1	0	1	1	1.54375
0	0	0	0	1	1	0	0	1.53750
0	0	0	0	1	1	0	1	1.53125
0	0	0	0	1	1	1	0	1.52500
0	0	0	0	1	1	1	1	1.51875
0	0	0	1	0	0	0	0	1.51250
0	0	0	1	0	0	0	1	1.50625
0	0	0	1	0	0	1	0	1.50000
0	0	0	1	0	0	1	1	1.49375
0	0	0	1	0	1	0	0	1.48750
0	0	0	1	0	1	0	1	1.48125
0	0	0	1	0	1	1	0	1.47500
0	0	0	1	0	1	1	1	1.46875
0	0	0	1	1	0	0	0	1.46250
0	0	0	1	1	0	0	1	1.45625
0	0	0	1	1	0	1	0	1.45000
0	0	0	1	1	0	1	1	1.44375
0	0	0	1	1	1	0	0	1.43750
0	0	0	1	1	1	0	1	1.43125
0	0	0	1	1	1	1	0	1.42500
0	0	0	1	1	1	1	1	1.41875
0	0	1	0	0	0	0	0	1.41250

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
0	1	0	1	1	0	1	1	1.04375
0	1	0	1	1	1	0	0	1.03750
0	1	0	1	1	1	0	1	1.03125
0	1	0	1	1	1	1	0	1.02500
0	1	0	1	1	1	1	1	1.01875
0	1	1	0	0	0	0	0	1.01250
0	1	1	0	0	0	0	1	1.00625
0	1	1	0	0	0	1	0	1.00000
0	1	1	0	0	0	1	1	0.99375
0	1	1	0	0	1	0	0	0.98750
0	1	1	0	0	1	0	1	0.98125
0	1	1	0	0	1	1	0	0.97500
0	1	1	0	0	1	1	1	0.96875
0	1	1	0	1	0	0	0	0.96250
0	1	1	0	1	0	0	1	0.95625
0	1	1	0	1	0	1	0	0.95000
0	1	1	0	1	0	1	1	0.94375
0	1	1	0	1	1	0	0	0.93750
0	1	1	0	1	1	0	1	0.93125
0	1	1	0	1	1	1	0	0.92500
0	1	1	0	1	1	1	1	0.91875
0	1	1	1	0	0	0	0	0.91250
0	1	1	1	0	0	0	1	0.90625
0	1	1	1	0	0	1	0	0.90000
0	1	1	1	0	0	1	1	0.89375
0	1	1	1	0	1	0	0	0.88750
0	1	1	1	0	1	0	1	0.88125
0	1	1	1	0	1	1	0	0.87500
0	1	1	1	0	1	1	1	0.86875
0	1	1	1	1	0	0	0	0.86250
0	1	1	1	1	0	0	1	0.85625
0	1	1	1	1	0	1	0	0.85000
0	1	1	1	1	0	1	1	0.84375



VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
0	0	1	0	0	0	0	1	1.40625
0	0	1	0	0	0	1	0	1.40000
0	0	1	0	0	0	1	1	1.39375
0	0	1	0	0	1	0	0	1.38750
0	0	1	0	0	1	0	1	1.38125
0	0	1	0	0	1	1	0	1.37500
0	0	1	0	0	1	1	1	1.36875
0	0	1	0	1	0	0	0	1.36250
0	0	1	0	1	0	0	1	1.35625
0	0	1	0	1	0	1	0	1.35000
0	0	1	0	1	0	1	1	1.34375
0	0	1	0	1	1	0	0	1.33750
0	0	1	0	1	1	0	1	1.33125
0	0	1	0	1	1	1	0	1.32500
0	0	1	0	1	1	1	1	1.31875
0	0	1	1	0	0	0	0	1.31250
0	0	1	1	0	0	0	1	1.30625
0	0	1	1	0	0	1	0	1.30000
0	0	1	1	0	0	1	1	1.29375
0	0	1	1	0	1	0	0	1.28750
0	0	1	1	0	1	0	1	1.28125
0	0	1	1	0	1	1	0	1.27500
0	0	1	1	0	1	1	1	1.26875
0	0	1	1	1	0	0	0	1.26250
0	0	1	1	1	0	0	1	1.25625
0	0	1	1	1	0	1	0	1.25000
0	0	1	1	1	0	1	1	1.24375
0	0	1	1	1	1	0	0	1.23750
0	0	1	1	1	1	0	1	1.23125
0	0	1	1	1	1	1	0	1.22500
0	0	1	1	1	1	1	1	1.21875
0	1	0	0	0	0	0	0	1.21250
0	1	0	0	0	0	0	1	1.20625
0	1	0	0	0	0	1	0	1.20000
0	1	0	0	0	0	1	1	1.19375

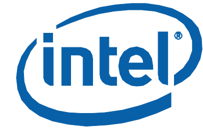
VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
0	1	1	1	1	1	0	0	0.83750
0	1	1	1	1	1	0	1	0.83125
0	1	1	1	1	1	1	0	0.82500
0	1	1	1	1	1	1	1	0.81875
1	0	0	0	0	0	0	0	0.81250
1	0	0	0	0	0	0	1	0.80625
1	0	0	0	0	0	1	0	0.80000
1	0	0	0	0	0	1	1	0.79375
1	0	0	0	0	1	0	0	0.78750
1	0	0	0	0	1	0	1	0.78125
1	0	0	0	0	1	1	0	0.77500
1	0	0	0	0	1	1	1	0.76875
1	0	0	0	1	0	0	0	0.76250
1	0	0	0	1	0	0	1	0.75625
1	0	0	0	1	0	1	0	0.75000
1	0	0	0	1	0	1	1	0.74375
1	0	0	0	1	1	0	0	0.73750
1	0	0	0	1	1	0	1	0.73125
1	0	0	0	1	1	1	0	0.72500
1	0	0	0	1	1	1	1	0.71875
1	0	0	1	0	0	0	0	0.71250
1	0	0	1	0	0	0	1	0.70625
1	0	0	1	0	0	1	0	0.70000
1	0	0	1	0	0	1	1	0.69375
1	0	0	1	0	1	0	0	0.68750
1	0	0	1	0	1	0	1	0.68125
1	0	0	1	0	1	1	0	0.67500
1	0	0	1	0	1	1	1	0.66875
1	0	0	1	1	0	0	0	0.66250
1	0	0	1	1	0	0	1	0.65625
1	0	0	1	1	0	1	0	0.65000
1	0	0	1	1	0	1	1	0.64375
1	0	0	1	1	1	0	0	0.63750
1	0	0	1	1	1	0	1	0.63125
1	0	0	1	1	1	1	0	0.62500



VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
0	1	0	0	0	1	0	0	1.18750	1	0	0	1	1	1	1	1	0.61875
0	1	0	0	0	1	0	1	1.18125	1	0	1	0	0	0	0	0	0.61250
0	1	0	0	0	1	1	0	1.17500	1	0	1	0	0	0	0	1	0.60625
0	1	0	0	0	1	1	1	1.16875	1	0	1	0	0	0	1	0	0.60000
0	1	0	0	1	0	0	0	1.16250	1	0	1	0	0	0	1	1	0.59375
0	1	0	0	1	0	0	1	1.15625	1	0	1	0	0	1	0	0	0.58750
0	1	0	0	1	0	1	0	1.15000	1	0	1	0	0	1	0	1	0.58125
0	1	0	0	1	0	1	1	1.14375	1	0	1	0	0	1	1	0	0.57500
0	1	0	0	1	1	0	0	1.13750	1	0	1	0	0	1	1	1	0.56875
0	1	0	0	1	1	0	1	1.13125	1	0	1	0	1	0	0	0	0.56250
0	1	0	0	1	1	1	0	1.12500	1	0	1	0	1	0	0	1	0.55625
0	1	0	0	1	1	1	1	1.11875	1	0	1	0	1	0	1	0	0.55000
0	1	0	1	0	0	0	0	1.11250	1	0	1	0	1	0	1	1	0.54375
0	1	0	1	0	0	0	1	1.10625	1	0	1	0	1	1	0	0	0.53750
0	1	0	1	0	0	1	0	1.10000	1	0	1	0	1	1	0	1	0.53125
0	1	0	1	0	0	1	1	1.09375	1	0	1	0	1	1	1	0	0.52500
0	1	0	1	0	1	0	0	1.08750	1	0	1	0	1	1	1	1	0.51875
0	1	0	1	0	1	0	1	1.08125	1	0	1	1	0	0	0	0	0.51250
0	1	0	1	0	1	1	0	1.07500	1	0	1	1	0	0	0	1	0.50625
0	1	0	1	0	1	1	1	1.06875	1	0	1	1	0	0	1	0	0.50000
0	1	0	1	1	0	0	0	1.06250	1	1	1	1	1	1	1	0	OFF
0	1	0	1	1	0	0	1	1.05625	1	1	1	1	1	1	1	1	OFF
0	1	0	1	1	0	1	0	1.05000									

1.6.2 Differential Remote Sense Input (REQUIRED)

The PWM controller must include differential sense inputs (remote sense, remote sense return) to compensate for an output voltage offset of ≤ 100 mV in the power distribution path and in the return path loop. The remote sense lines should draw no more than 1.0 mA to minimize offset errors. The remote sense input needs to have sufficient CMRR to not pass and amplify high frequency processor noise to the VR output. Refer to the processor specific sections of this document for measurement locations.



1.6.3 Power State Indicator (PSI#) (Required)

The processor will provide an output signal to the VR controller to indicate when the processor is in a low power state. The VR PWM controller can use this signal to change its operating state (phase shedding) to maximize efficiency at light loads or optimize the efficiency curve for system idle power reduction. The PSI# signal will be a 1 V CMOS compliant signal. See the Table 1-8.

PSI# will be asserted when the processor is in a power state such that the current draw is within the range of a single phase current rating – typically < 20 A. The PSI# signal will de-assert 3.3 μs prior to moving to a normal power state. Refer to the appropriate processor datasheet for specific details on the current threshold for PSI# assertion. If an increasing voltage DVID event occurs while PSI# is asserted, the PWM should change to normal power mode.

PSI# is high for normal power mode and is asserted low for low power mode.

Note that PSI# operation is different for LGA775 platforms. Please refer to that section for more information on unique PSI# operation.

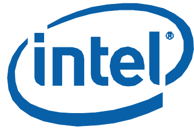
1.7 Input Voltage and Current

1.7.1 Input Voltages (EXPECTED)

VRD output voltage is supplied via DC-to-DC power conversion. To ensure proper operation, the input supplies to these regulators must satisfy the following conditions.

1.7.1.1 Desktop Input Voltages

The main power source for the V_{CC} VRD is 12 V ±15% and 3.3 V ±5% for the V_{TT} supply. These voltages are supplied by an AC-DC power supply through a dedicated 12 V cable to the motherboard VRD input. For input voltages outside the normal operating range, the VRD should either operate properly or shut down. Intel recommends a DC-DC regulator input filter with a minimum 1000 μF to ensure proper loading of the 12 V power source.



1.7.1.2 Efficiency (OPTIONAL)

The following tables show the expected VR efficiency for each of the VR configurations. The input voltage of efficiency testing should be 11 VDC. This input voltage will represent the worst case input voltage to the VRD under a high load condition.

Voltage regulator efficiency is measured from the 12 V voltage regulator input to the loadline reference node. See the processor specific sections for more details on the loadline reference nodes.

Table 1-10. 1366_VR Efficiency Guidelines

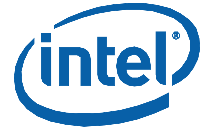
	VR Efficiency per loading level		
Configuration	**2–5 A**	**6–20 A**	**VR_TDC**
1366_VR_CONFIG_08B	> 70%	> 80%	> 75%

Table 1-11. LGA1156_VR Efficiency Guidelines

	VR Efficiency per loading level		
Configuration	**2–5 A**	**6–20 A**	**VR_TDC**
1156_VR_CONFIG_09A/B	> 70%	> 80%	> 75%

Table 1-12. LGA775_VR Efficiency Guidelines

	VR Efficiency per loading level		
Configuration	**Idle (20% of I_{CC} (max))**	**VR_TDC**	**I_{CC} (max)**
775_VR_CONFIG_04A	—	75%	—
775_VR_CONFIG_04B	—	75%	—
775_VR_CONFIG_05A	—	75%	—
775_VR_CONFIG_05B	—	75%	75% (80% preferred)
775_VR_CONFIG_06	75%	—	—



1.8 Output Protection

This section describes features built into the DC-DC regulator to prevent damage to itself, the processor, validation tools, or other system components.

1.8.1 Over-Voltage Protection (OVP) (PROPOSED)

OVP is proposed to protect the processor from high voltage damage that may lead to failure, or a reduced processor life span. The OVP circuit is to monitor V_{CC} for an over-voltage condition at the defined regulation lands. This voltage must never exceed maximum VID+200 mV (that is, 1.6 V + 200 mV) under any condition and operation above this level defines an OVP violation. In the event of an OVP violation, the V_{CC} VR low side MOSFETs should be driven on to protect the processor and the VR should de-assert VR_READY to shut down the core supply voltage. Power cycling is required to re-start the system.

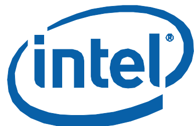
OVP at start-up should be fully functional with a trip level referenced to the boot VID of 1.1 V.

Operating at lower VID codes during Dynamic VID establishes low (invalid) OVP thresholds which must not be used to initiate a system shut down. For example, there is a time delay from transmission of a VID code to the VR reaction; this time lag may result in a 200 mV delta from the reference VID at a functional voltage that will not damage the processor. Because of these conditions, OVP functionality must be blanked during the Dynamic VID state.

1.8.2 Over-Current Protection (OCP) (PROPOSED)

The DC-DC should be capable of withstanding a continuous, abnormally low resistance on the output without damage or over-stress to the DC-DC. The OCP trip level should be programmable by the DC-DC designer, typically 130% of rated output current. If an OCP fault is detected, the VR should fold back or shut down, de-assert VR_READY and reset the start up sequence.

Output current under this condition must be limited to avoid component damage and violation of the VRD thermal specifications.



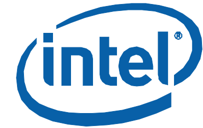
1.9 Output Indicators

1.9.1 VR_READY — V_{CC} Regulator Is 'ON' (REQUIRED)

VR_READY is an active high output that indicates the start up sequence is complete and the output voltage has moved to the programmed VID value. This signal will be used for start up sequencing for other voltage regulators, the clock, microprocessor reset, etc. This signal should not be de-asserted by low voltages that occur during D-VID operation. The signal should remain asserted during normal DC-DC operating conditions and only de-assert for fault or shutdown conditions. This signal is not a representation of the accuracy of the DC output to its VID value; it is simply a flag to indicate the VRD is functioning. See Figure 1-11 for timing and Table 1-13 for signal specifications.

Table 1-13. VR_Ready output signal Specifications

Signal Type		Open Collector/Drain Logic output from PWM IC, with external pull-up resistor and reference voltage.			
VR_Ready = HIGH		Active / Asserted			
VR_Ready = LOW		Not Active / De-Asserted			
Symbol	**Parameter**	**Min**	**Max**	**Units**	**Remarks**
V_{OH}	Output Voltage High	0.8	3.3	VDC	V_{TT} rail is expected; Open Coll. /Drain Trans. OFF, Imp. >100 kΩ depending on system implementation
V_{OL}	Output Voltage Low	0	0.3	VDC	With external pull-up resistor; Open Coll./Drain Trans. ON
I_{OL}	Output Low Sink Current	1.0	4.0	mA DC	Current limit set by external pull-up resistor
	Transition Edge Rate	—	150	ns	From 10-90% rise



1.9.2 Load Current Signal (Iout) (REQUIRED)

Iout load current measurement is required for power management features of the processor. This signal will be connected directly to the processor.

The VR11.1 PWM should have an analog output that varies linearly and represents the total output current from the voltage regulator. Voltage on this pin will be linearly proportional to the output current. Proportional gain will be platform specific and needs to be externally programmable. The dc-dc regulator on the platform will provide gain setting to processor using Power On Configuration (POC) lines (3 bit information to select one of 8 different gain options). The POC levels are multiplexed onto the VID lines with pull-up and pull-down resistors and read by the processor during the TD0 time (between V_{TT} being valid and Vtt_PG asserting). After Vtt_PG is asserted the VID CMOS drivers override the MSID, POC pull-up and pull-down resistors. See Table 1-8, "Interface Signals Parameters" for more information.

The information for total output current can come from the circuit blocks that generate the loadline droop. Iout is expected to be temperature compensated in the same manner as the loadline Vdroop. See the following tables for gain definitions.

Table 1-14. Iout Analog Output Requirements

Iout (mV)	VR Output Current (A)
0	0
900	I_{MAX}

NOTES:

1. I_{MAX} is the VR maximum current corresponding to the processor's POC gain setting not the OCP level.

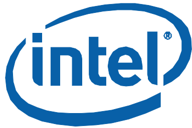
Table 1-15. Iout Gain and POC Settings

Processor I_{CC} (max)	I_{MAX} Iout gain: 900 mV = I_{MAX}	POC Gain Setting
Disabled	-	000
I_{CC} (max) ≤ 40 A	40 A	001
40 A < I_{CC} (max) ≤ 60 A	60 A	010
60 A < I_{CC} (max) ≤ 80 A	80 A	011
80 A < I_{CC} (max) ≤ 100 A	100 A	100
100 A < I_{CC} (max) ≤ 120 A	120 A	101
120 A < I_{CC} (max) ≤ 140 A	140 A	110
140 A < I_{CC} (max) ≤ 180 A	180 A	111

NOTES:

1. **Warning!** Under any operating or fault condition, voltage on Iout must not exceed 1.15 V to prevent damage to the processor input gate.

The processor receiver will be referenced to VSS_SENCE. To minimize offset errors between different reference potentials Iout from the PWM should be referenced to this



pin (VSS_SENCE). Regardless of implementation method, current draw on reference (VSS_SENCE) pin must not exceed a 1 mA for both Iout and remote sense bias currents.

Iout signal must be filtered with a filter time constant of >300 us to prevent ADC aliasing in the processor. This value should be well below the L/R time constant of the motherboard inductors.

The controller inaccuracy contribution should be minimized. Total solution accuracy will be defined by controller, inductor DCR accuracy (if solution implements inductor current sensing) and external passive components. The tightest accuracy is expected at full load. Linearity must be supported.

The Iout accuracy requirements are shown in Table 1-16.

Table 1-16. Iout Accuracy Requirements

Accuracy	Current
-0 / +20%	100% x I_{CC} (max)
-0 / +40%	50% x I_{CC} (max)
-0 / +60%	25% x I_{CC} (max)

It is highly recommended the IMON linearity and accuracy will be maximized. Less accurate IMON reporting will have negative performance impact on the processor. Total solution accuracy will be defined by the PWM controller, inductor DCR accuracy (if solution implements inductor current sensing) and the external passive components. The tightest accuracy is expected at full load. It will be left to the MB designer to specify the VR's IMON accuracy for the optimal design point. Vendors should provide the accuracy graphs to the MB designer to aid in component and vendor selection.

1.9.3 Thermal Monitoring

1.9.3.1 VR_HOT (EXPECTED)

Each customer is responsible for identifying maximum temperature specifications for all components in the voltage regulator design and ensuring that these specifications are not violated while continuously drawing specified VR TDC levels. In the event of a catastrophic thermal failure, the thermal monitoring circuit is to assert the VR_HOT signal to drive the processor PROCHOT# inputs immediately prior to exceeding maximum temperature ratings to prevent heat damage. Assertion of these signals will lower processor power consumption and reduce current draw through the voltage regulator, resulting in lower component temperatures. Assertion of PROCHOT# degrades system performance and must never occur when drawing less than specified thermal design current. The tolerance on VR_HOT should be ±4% or approximately ±4 degrees Celsius with 10 degree Celsius hysteresis.

VR_HOT is an active high output. See PWM IC vendor's data sheets for signal interface specifications (open drain or push-pull). VR_HOT cannot be tied directly to PROCHOT#; the signals must be inverted and buffered. See Table 1-17 for PROCHOT# signal requirements.

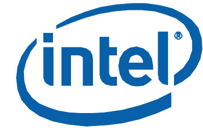


Figure 1-16. PROCHOT# Load External to Processor

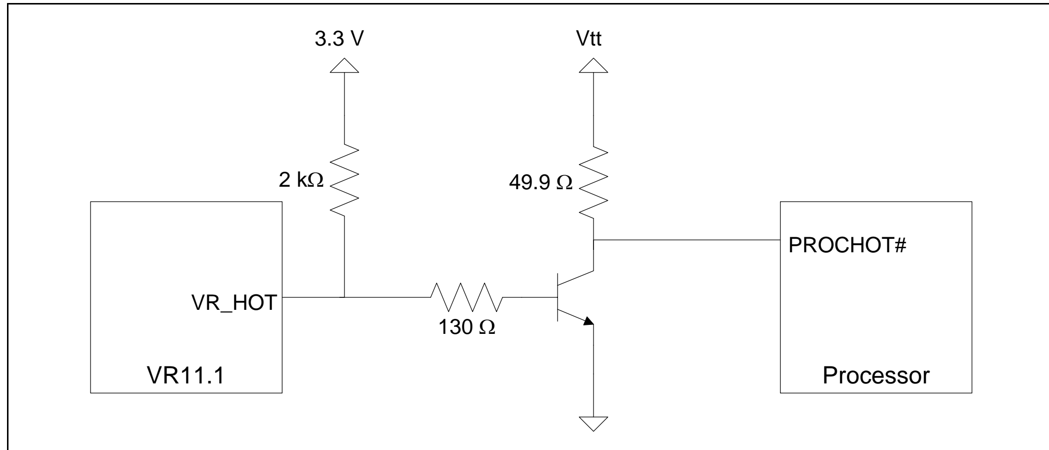


Table 1-17. Thermal Monitor Specifications

Parameter	Minimum	Typical	Maximum
V_{TT}	—	V_{TT} [1]	—
Q1 'on' resistance	—	—	11 Ω
PROCHOT# leakage current	—	—	200 µA
PROCHOT# transition time	1.10 ns	100 ns	—
PROCHOT# VOL (Maximum low voltage threshold)	—	—	0.4 V
Minimum time to toggle in and out of D-VID	0.5 ms	—	—

NOTE:

1. Consult the appropriate processor datasheet for the V_{TT} specifications.

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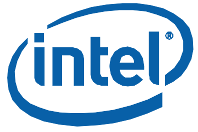
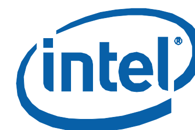




2 LGA1366 Information

2.1 Introduction

This chapter focuses on information unique to platforms designed with the LGA 1366.

2.1.1 Applications

Previously in the *Voltage Regulator-Down (VRD) 11.0 Processor Power Delivery Design Guidelines* the motherboard regulation loadline was defined at the socket. Specifically the loadline was referenced to the VCC_MB_REGULATION and VSS_MB_REGULATION lands on the LGA775 socket. This is still the case when VRD11.1 is used for platforms with the LGA775 socket. However, platforms using the LGA1366 socket will use a different loadline definition and reference point. The loadline for LGA1366 socket platforms is referenced to the VCC_SENSE and the VSS_SENSE lands. The implication of this is that the slope of the loadline at the VCC_SENSE/VSS_SENSE point is not the same as the socket loadline. The loadline at the VCC_SENSE/VSS_SENSE lands is 0.8 mΩ. This is equivalent to a socket loadline slope of 0.5 mΩ.

2.2 Processor V_{CC} Requirements

2.2.1 Loadline Definitions (REQUIRED)

To maintain processor reliability and performance, platform DC voltage regulation and transient-droop noise levels must always be contained within the Vccmin and Vccmax loadline boundaries (known as the loadline window). Loadline compliance must be ensured across component manufacturing tolerances, thermal variation, and age degradation. Loadline boundaries are defined by the following equations in conjunction with the V_{CC} regulator design parameter values defined in Table 2-2. In these equations, VID, R_{LL}, and TOB are known. Plotting V_{CC} while varying I_{CC} from 0 A to Iccmax establishes the Vccmax and Vccmin loadlines. Vccmax establishes the maximum DC loadline boundary. Vccmin establishes the minimum AC and DC voltage boundary. Short transient bursts above the Vccmax loadline are permitted; this condition is defined in Section 1.3.7.

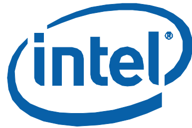


Table 2-1. Loadline Equations

Loadline	Equation
Equation 5: Vccmax Loadline	V_{CC} = VID – (R_{LL}* I_{CC})
Equation 6: Vcctyp Loadline	V_{CC} = VID – TOB - (R_{LL}* I_{CC})
Equation 7: Vccmin loadline	V_{CC} = VID – 2*TOB - (R_{LL}* I_{CC})

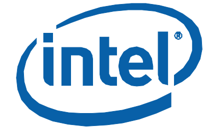
Loadline recommendations are established to provide guidance for satisfying processor loadline specifications, which are defined in processor datasheets. Loadline requirements must be satisfied at all times and may require adjustment in the loadline value. The processor loadlines are defined in the applicable processor datasheet.

Table 2-2. V_{CC} Regulator Design Parameters

VR Configuration	Iccmax	VR TDC	Dynamic I_{CC}	RLL	TOB	Maximum VID
1366_VR_CONFIG_08B	145 A	110 A	100 A	0.8 mΩ	± 19 mV	TBD V

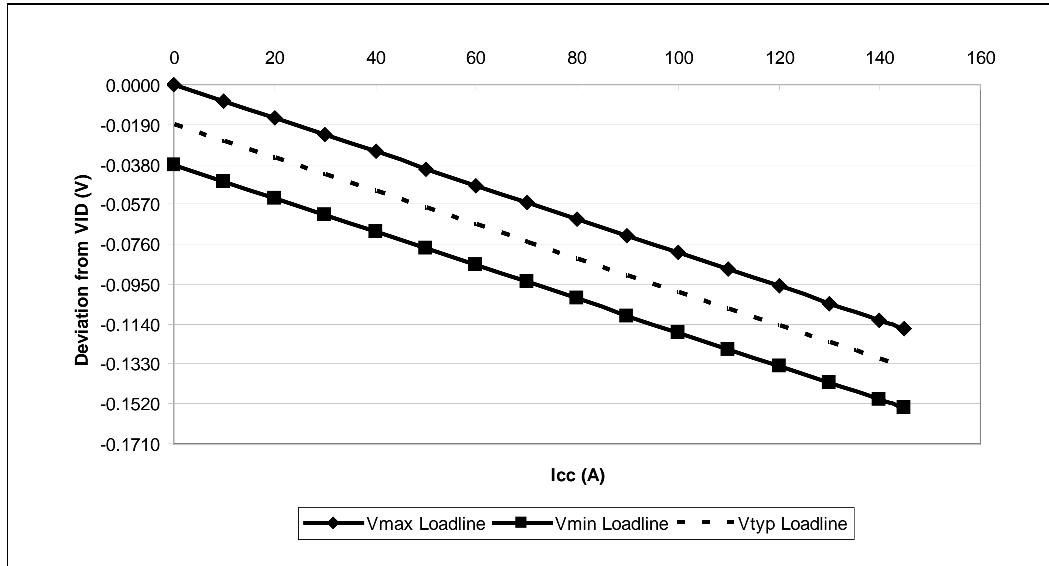
Table 2-2 provides a list of VRD11.1 LGA1366 voltage regulator design configurations. The configurations to be adopted by VRD hardware will depend on the specific processors the design is intended to support. It is common for a motherboard to support processors that require different VR configurations. In this case, the V_{CC} regulator design must meet the specifications of all processors supported by that board.

The following tables and figures show minimum and maximum voltage boundaries for each loadline design configuration defined in Table 2-2. V_{CCTYP} loadlines are provided for design reference; designs should calibrate the loadline to this case (centered in the loadline window, at the mean of the tolerance band). Different processors discussed in this design guide can be shipped with different VID values. The reader should not assume that processors with similar characteristics will have the same VID value. A single loadline chart and figure for each VRD design configuration can represent functionality for each possible VID value. Tables and figures presented as voltage deviation from VID provide the necessary information to identify voltage requirements at any reference VID. This avoids the redundancy of publishing tables and figures for each of the multiple cases.



2.2.1.1 Loadline Definition for 1366_VR_CONFIG_08B

Figure 2-1. Loadline Window for 1366_VR_CONFIG_08B

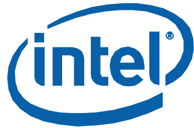


NOTES:
1. Presented as a deviation from VID
2. Loadline Slope = 0.8 mΩ, TOB = ±19 mV
3. Consult Table 2-2 for VR configuration parameter details

Table 2-3. Loadline Window for 1366_VR_CONFIG_08B

I_{CC}	Maximum (V)	Typical (V)	Minimum (V)
0 A	0.0000	-0.0190	-0.0380
10 A	-0.0080	-0.0270	-0.0460
20 A	-0.0160	-0.0350	-0.0540
30 A	-0.0240	-0.0430	-0.0620
40 A	-0.0320	-0.0510	-0.0700
50 A	-0.0400	-0.0590	-0.0780
60 A	-0.0480	-0.0670	-0.0860
70 A	-0.0560	-0.0750	-0.0940
80 A	-0.0640	-0.0830	-0.1020
90 A	-0.0720	-0.0910	-0.1100
100 A	-0.0800	-0.0990	-0.1180
110 A	-0.0880	-0.1070	-0.1260
120 A	-0.0960	-0.1150	-0.1340
130 A	-0.1040	-0.1230	-0.1420
140 A	-0.1120	-0.1310	-0.1500
145 A	-0.1160	-0.1350	-0.1540

NOTES:
1. Presented as a deviation from VID
2. Loadline Slope = 0.8 mΩ, TOB = ±19 mV
3. Consult Table 2-2 for VR configuration parameter details



VRD layout studies indicate that the phases are best located north of the processor with the controller to the northeast.

Table 2-4. Loadline Reference Lands for the LGA1366 Socket

Name	Land
VCC_SENSE	AR9
VSS_SENSE	AR8

To properly calibrate the loadline parameter, the VR designer must excite the processor socket with a current step that generates a voltage droop which must be checked against the loadline window requirements. Table 2-5 identifies the steady state and transient current values to use for this calibration.

Table 2-5. Intel® Processor Current Step Values for Transient Loadline Testing

VR Configuration	Starting Current	Ending Current	Dynamic Current Step	I_{CC} Rise Time	I_{CC} Fall Time
1366_VR_CONFIG_08B	45 A	145 A	100 A	200 ns	200 ns

2.2.1.2 Time Domain Validation

To ensure processor reliability and performance, platform transient-droop and overshoot noise levels must always be contained within the Vccmin and Vccmax loadline boundaries (known as the loadline window). The load generates a voltage droop, or overshoot, which must be checked against the loadline window requirements. The current step must have a fast enough slew rate to excite the impedance across the frequency range of the VR. In addition, the VR needs to be tested at different load frequencies and load steps to prevent any non-linear, resonant, or beating effects that could cause functional issues or loadline violations. Intel recommends sweeping the load frequency from DC to 1 MHz, using two different load steps.

Intel recommends testing using different VID levels for each of the supported VR configurations. In particular the highest and lowest VIDs should be checked. The VID ranges for each processor is available in the processor datasheet.

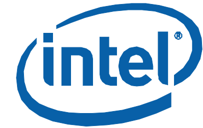
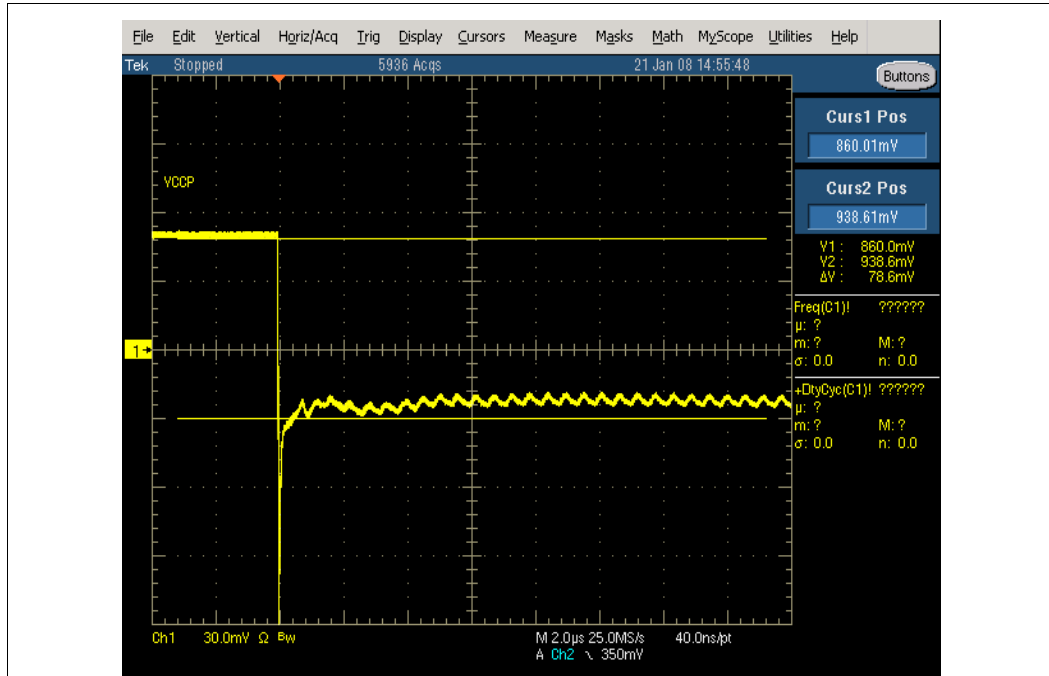
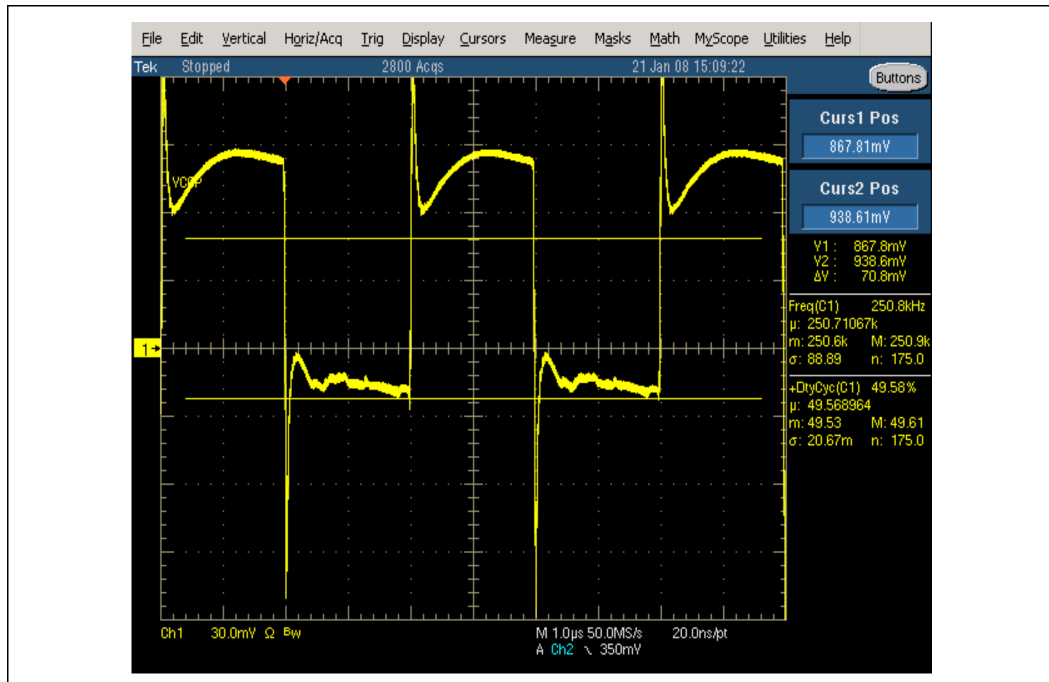


Figure 2-2. 200 Hz, 100 A Step Droop Waveform



NOTE: The cursor indicates the droop area of interest. A falling edge with a width less than 100 ns can be ignored.

Figure 2-3. 250 kHz, 100 A Step Waveform



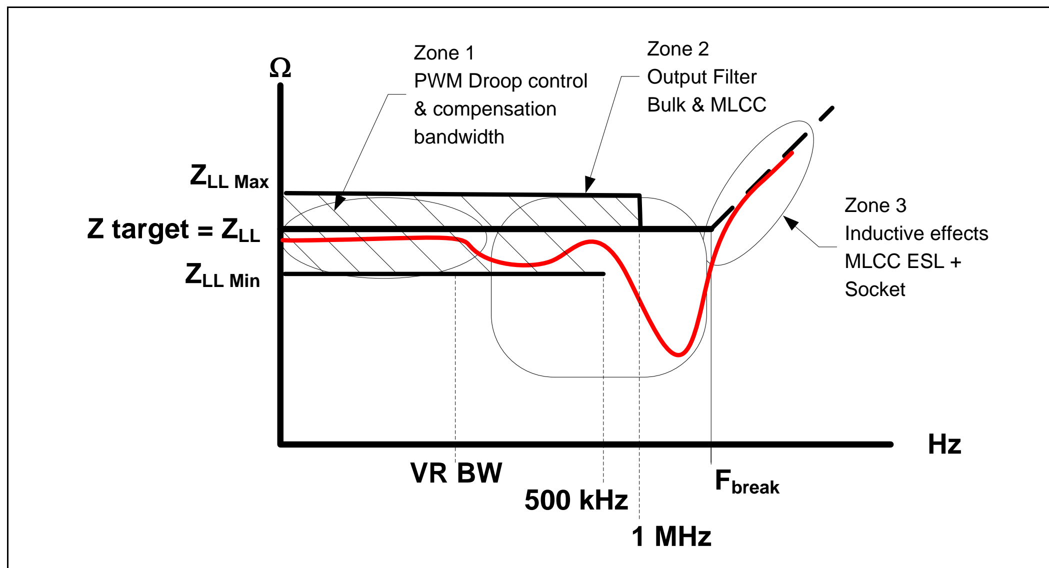
NOTE: The cursor indicates the droop area of interest. A falling edge with a width less than 100 ns can be ignored.

2.2.1.3 Platform Impedance Measurement and Analysis (Expected)

In addition to the tuning of the loadline with Vdroop testing and DC loadline testing, the decoupling capacitor selection needs to be analyzed to make sure the impedance of the decoupling is below the loadline target up to the frequency F_{break} as defined in Figure 2-4. This analysis can be done with impedance testing or through power delivery simulation if the designer can extract the parasitic resistance and inductance of the power planes on the motherboard and they have good models for the decoupling capacitors.

Measured power delivery impedance should be with in the tolerance band shown in Figure 2-4. For loadline compliance, time domain validation is required and the VR tolerance band must be met at all times. Above 500 kHz, the minimum impedance tolerance is not defined and is determined by the MLCC capacitors required to get the ESL low enough to meet the loadline impedance target at the F_{break} frequency. At 1 MHz, the Zmax tolerance drops to the loadline target impedance. Any resonance points that are above the Zmax line need to be carefully evaluated with time domain method defined in Section 2.2.1.2 by applying transient loads at that frequency and looking for Vmin violations. Maintaining the impedance profile up to F_{break} is important to ensure the package level decoupling properly matches the motherboard impedance. After F_{break}, the impedance measurement is permitted to rise at a inductive slope. The motherboard VR designer does not need to design for frequencies over F_{break} as the processor package decoupling takes over in the region above F_{break}.

Figure 2-4. Power Distribution Impedance versus Frequency



NOTES:

1. See Table 2-6. Impedance Measurement Parameters definitions
2. Zone 1 is defined by the VR closed loop compensation bandwidth (VR BW) of the voltage regulator. Typically 30–40 kHz for a 300 kHz voltage regulator design.
3. Zones 2 and 3 are defined by the output filter capacitors and interconnect parasitic resistance and inductance. The tolerance is relaxed over 500 kHz allowing the VR designer freedom to select output filter capacitors. The goal is to keep Z(f) below Z_{LL} up to Fbreak and as flat as practical, by selection of bulk capacitor values and type and number of MLCC capacitors. The ideal impedance would be between Z_{LL} and Z_{LL} Min but this may not be achieved with standard decoupling capacitors.

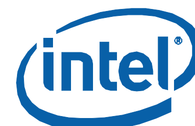


Table 2-6. Impedance Measurement Parameters

Parameter	Value	Notes
Z_{LL}	0.8 mΩ	LGA1366 Desktop LL target
$Z_{LL\ max}$	1.0 mΩ	Based on VR11.1 PWM tolerance band
$Z_{LL\ min}$	0.6 mΩ	Based on VR11.1 PWM tolerance band
F_{break}	2.0 MHz	—

2.3 V_{TT} Requirements (REQUIRED)

The V_{TT} regulator provides power to the non-core sections of the processor. The VTTPWRGOOD signal from this regulator begins power sequencing. Valid output voltage of the V_{TT} regulator must be ensured by the timing protocol defined in the Power Sequencing section.

2.3.1 Electrical Specifications

A VR11.0 based regulator is recommended for the V_{TT} supply with adequate decoupling capacitors to ensure the sum of AC bus noise and DC tolerance satisfy limits identified in Table 2-7. The processor V_{TT} supply must be maintained within these tolerance limits across full operational thermal limits, part-to-part component variation, age degradation, and regulator accuracy. Full bandwidth bus noise amplitude must be ensured across the land pairs defined in Table 2-9.

The V_{TT} supply must be unconditionally stable under all DC and transient conditions across the voltage and current ranges defined in Table 2-7. The V_{TT} supply must also operate in a no-load condition; that is, with no processor installed.

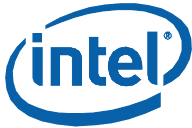
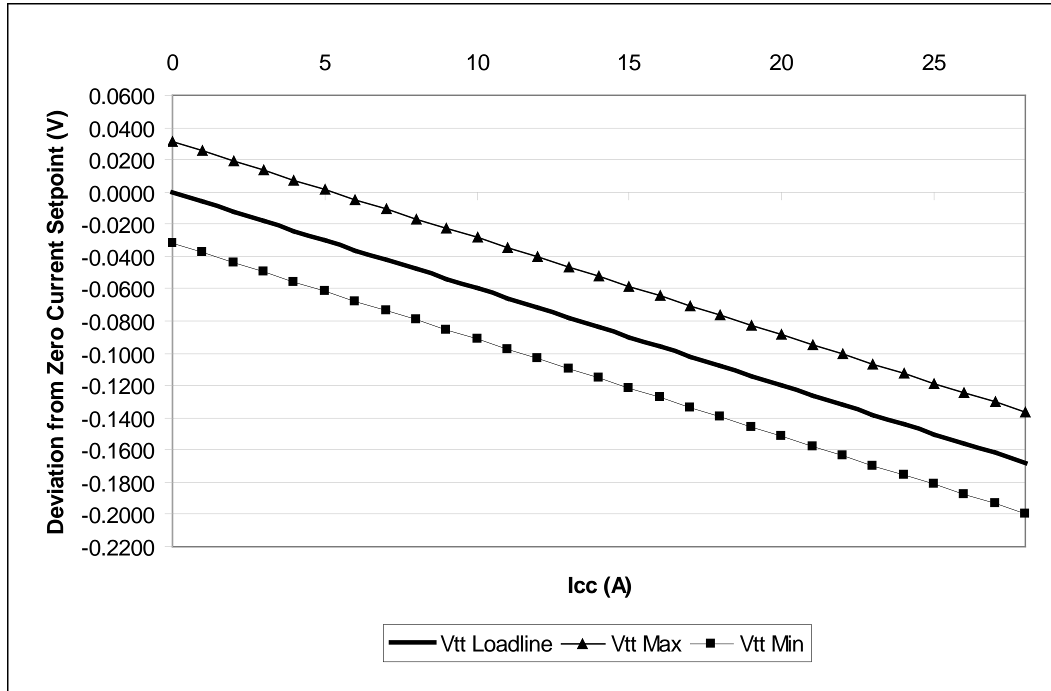


Figure 2-5. Window for V_{TT} Voltage on LGA1366 Platforms

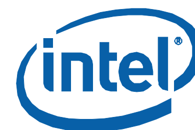


NOTES:

1. Presented as a deviation from V_{TT} zero current setpoint.

Table 2-7. Window for V_{TT} Voltage on LGA1366 Platforms

I_{CC} (A)	Maximum (V)	V_{TT} Loadline (V) 6.0 mΩ	Minimum (V)
0	0.0315	0.0000	-0.0315
1	0.0255	-0.0060	-0.0375
2	0.0195	-0.0120	-0.0435
3	0.0135	-0.0180	-0.0495
4	0.0075	-0.0240	-0.0555
5	0.0015	-0.0300	-0.0615
6	-0.0045	-0.0360	-0.0675
7	-0.0105	-0.0420	-0.0735
8	-0.0165	-0.0480	-0.0795
9	-0.0225	-0.0540	-0.0855
10	-0.0285	-0.0600	-0.0915
11	-0.0345	-0.0660	-0.0975
12	-0.0405	-0.0720	-0.1035
13	-0.0465	-0.0780	-0.1095
14	-0.0525	-0.0840	-0.1155
15	-0.0585	-0.0900	-0.1215
16	-0.0645	-0.0960	-0.1275



I_{CC} (A)	Maximum (V)	V_{TT} Loadline (V) 6.0 mΩ	Minimum (V)
17	-0.0705	-0.1020	-0.1335
18	-0.0765	-0.1080	-0.1395
19	-0.0825	-0.1140	-0.1455
20	-0.0885	-0.1200	-0.1515
21	-0.0945	-0.1260	-0.1575
22	-0.1005	-0.1320	-0.1635
23	-0.1065	-0.1380	-0.1695
24	-0.1125	-0.1440	-0.1755
25	-0.1185	-0.1500	-0.1815
26	-0.1245	-0.1560	-0.1875
27	-0.1305	-0.1620	-0.1935
28	-0.1365	-0.1680	-0.1995

NOTES:
1. Presented as a deviation from V_{TT} zero current setpoint.

Table 2-8 V_{TT} Parameters

I_{CC} Max	I_{CC} TDC	Istep	Istep Slew Rate	Ripple
28A	28 A	10 A	10A / us	15mV pk-pk

Table 2-9. V_{TT} Measurement Lands

Device	Supply	Land
Processor	VTTD_SENSE	AE36
Processor	VSS_SENSE_VTTD	AE37

Table 2-10. V_{TT} VID Lands

Processor Land	V_{TT} VID	VR11 VID Input
AV6	Vtt_VID4	VID4
AF7	Vtt_VID3	VID3
AV3	Vtt_VID2	VID2

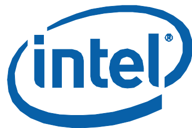


Table 2-11. V_{TT} VID Voltage

VR11 VID Input								DAC Voltage	V_{TT} Zero Current Setpoint (DAC+20 mV)
7	6	5	V_{TT}_VID4	V_{TT}_VID3	V_{TT}_VID2	1	0		
0	1	0	0	0	0	1	0	1.200 V	1.220 V
0	1	0	0	0	1	1	0	1.175 V	1.195 V
0	1	0	0	1	0	1	0	1.150 V	1.170 V
0	1	0	0	1	1	1	0	1.125 V	1.145 V
0	1	0	1	0	0	1	0	1.100 V	1.120 V
0	1	0	1	0	1	1	0	1.075 V	1.095 V
0	1	0	1	1	0	1	0	1.050 V	1.070 V
0	1	0	1	1	1	1	0	1.025 V	1.045 V

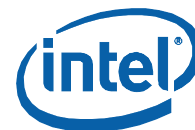
2.4 LGA 1366 Specific Signals

2.4.1 Power-on Configuration (POC) Signals on VID (REQUIRED)

All 8 VID lines will serve a second function: the Power On Configuration (POC) logic levels are multiplexed onto the VID lines with 1 kΩ pull-ups and pull-downs and they will be read by the processor during the time - as shown in the Power Sequencing section. The POC configuration programs the processor as to the platform VR capabilities. The VR does not read POC configuration resistors. After OUTEN is asserted the processor VID CMOS drivers override the POC pull-up, and pull-down resistors. See the Power Sequencing section for more information.

The POC bits (Multiplexed with 8 VID lines) are allocated is as follows:

- POC/(VID)[2:0] = MSID (Market Segment ID) bits, refer to the datasheet.
- POC/(VID)[5:3] = Current Sense Config bits, Iout gain setting, see Table 1-15.
- POC/(VID)[6] = RESERVED (pull-down resistors installed, unless stated otherwise in the datasheet).
- POC/(VID)[7] = VR11.1 Select signal, with pull-down resistor installed for VR11.1, refer to the datasheet.



2.5 MB Power Plane Layout (REQUIRED)

The motherboard layer stack-up must be designed to ensure robust, noise-free power delivery to the processor. Failure to minimize and balance power plane resistance may result in non-compliance to the loadline specification. A poorly planned stack-up or excessive holes in the power planes may increase system inductance and generate oscillation on the V_{CC} voltage rail at the processor. Both of these types of design errors can lead to processor failure and must be avoided by careful V_{CC} and V_{SS} plane layout and stack-up. The types of noise introduced by these errors may not be immediately observed on the processor power lands or during system-board voltage transient validation, so issues must be resolved by design, prior to layout, to avoid unexpected failures.

Following basic layout rules can help avoid excessive power plane noise. All motherboard layers in the area surrounding the processor socket should be used for V_{CC} power delivery; copper shapes that encompass the power delivery region of the processor land field are required. A careful motherboard design will help ensure a well-functioning system that minimizes the noise profile at the processor. The following subsections provide further guidance.

2.5.1 Minimize Power Path DC Resistance

Power path resistance can be minimized by ensuring that the copper layout area is balanced between V_{CC} and V_{SS} planes. A good six layer board design will have three V_{CC} layers and three V_{SS} layers. Because there is generally more V_{SS} copper in the motherboard stack-up, care should be taken to maximize the copper in V_{CC} floods. This includes care to minimize unnecessary plane splits and holes when locating through hole components, vias, and connection pads. Refer to Table 2-12 for more details on the reference board layer stackup.

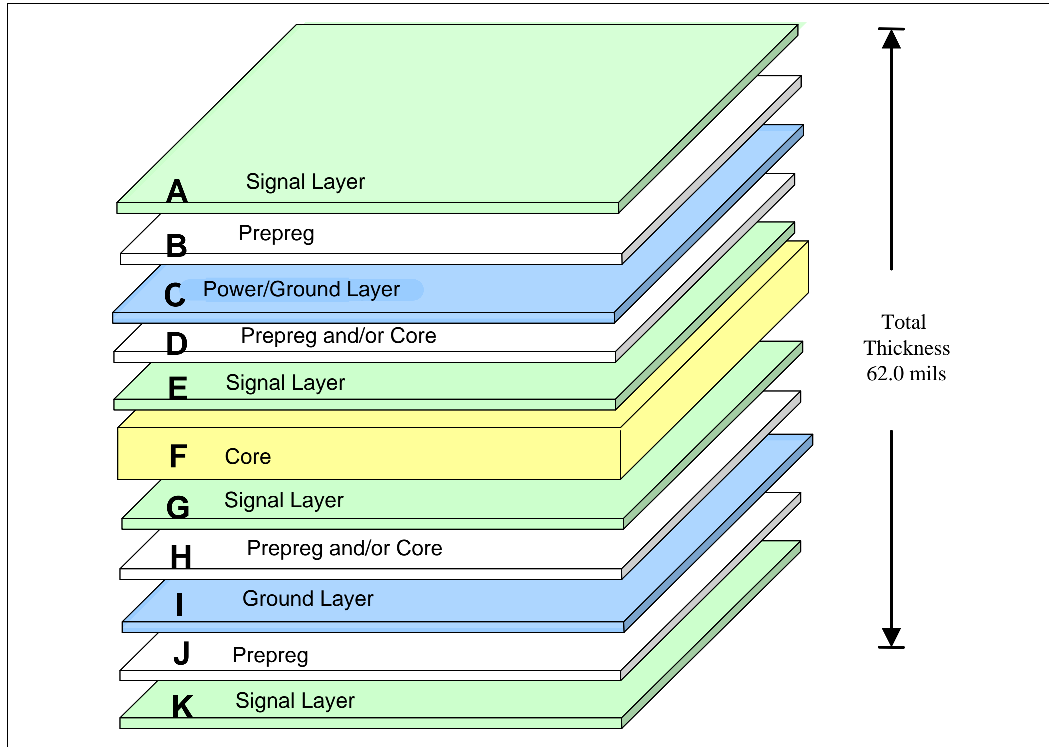
2.5.2 Minimize Power Delivery Inductance

At higher frequencies the ordering of the motherboard layers becomes critical as it is V_{CC}/ V_{SS} **plane pairs** which carry current and determine power plane inductance. The layer stack-up should maximize adjacent (layer-to-layer) planes at a minimized spacing to achieve the smallest possible inductance. Care must be taken to minimize unnecessary plane splits and holes when locating through-hole components, vias, and connection pads. Minimized inductance will ensure that the board does not develop low frequency noise which may cause the processor to fail (loadline violation).

2.5.3 Six-Layer Boards

A well-designed 6-layer board will feature generous V_{CC} shapes on the outer layers and large V_{SS} shapes on the inner layers. The V_{SS} -reference requirements for the front side bus are best accommodated with this layer ordering. The power plane area should be maximized and cut-out areas should be carefully placed to minimize parasitic resistance and inductance. Examples power plane layout of the Intel reference board are provided in Table 2-12 and Figure 2-6 through Figure 2-10.

Figure 2-6. Reference Board Layer Stack-up



NOTE: Drawing is not to scale

Table 2-12. Reference Board Layer Thickness (Prepreg 1080)

Layer	Minimum (mil)	Typical (mil)	Maximum (mil)
A	1.10	1.90	2.75
B	2.00	2.70	3.50
C	1.00	1.20	1.40
D	3.25	4.00	4.75
E	1.00	1.20	1.40
F	Adjusted to meet overall board thickness of 62 mils		
G	1.00	1.20	1.40
H	3.25	4.00	4.75
I	1.00	1.20	1.40
J	2.00	2.70	3.50
K	1.10	1.90	2.75

NOTES:

1. Consult Figure 2-6 for layer definition
2. Impedance Target: 50 Ω ± 15%; based on nominal 4 mil trace
3. Overall board thickness is 62 mils +8, -5 mils

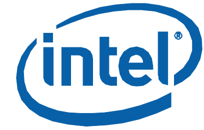
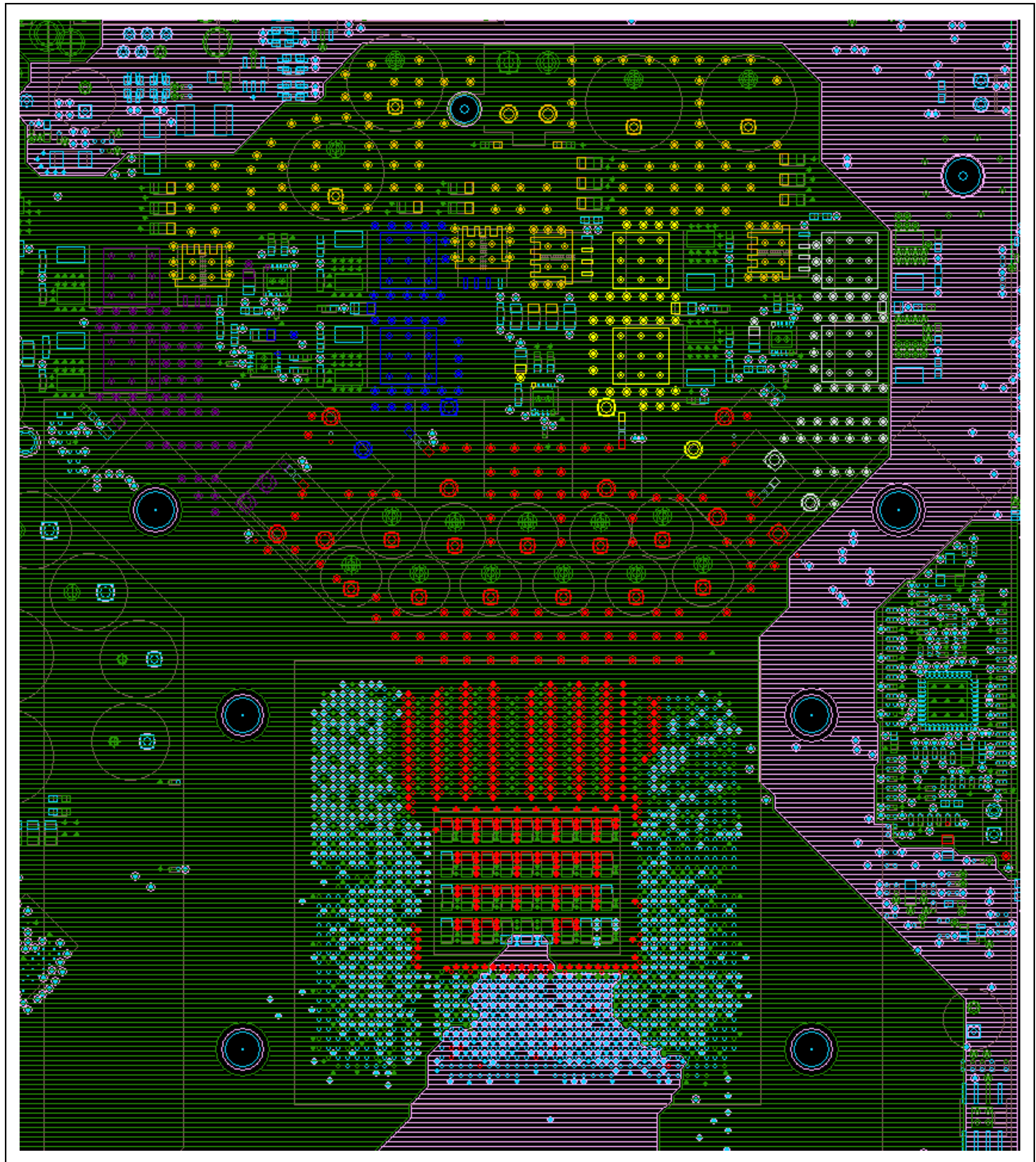


Figure 2-7. Layer 1 V_{CC} Shape for Intel® Reference Six-layer Motherboard

Figure 2-8. Layer 2 V_{SS} Routing for Intel® Reference Six-layer Motherboard



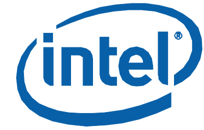
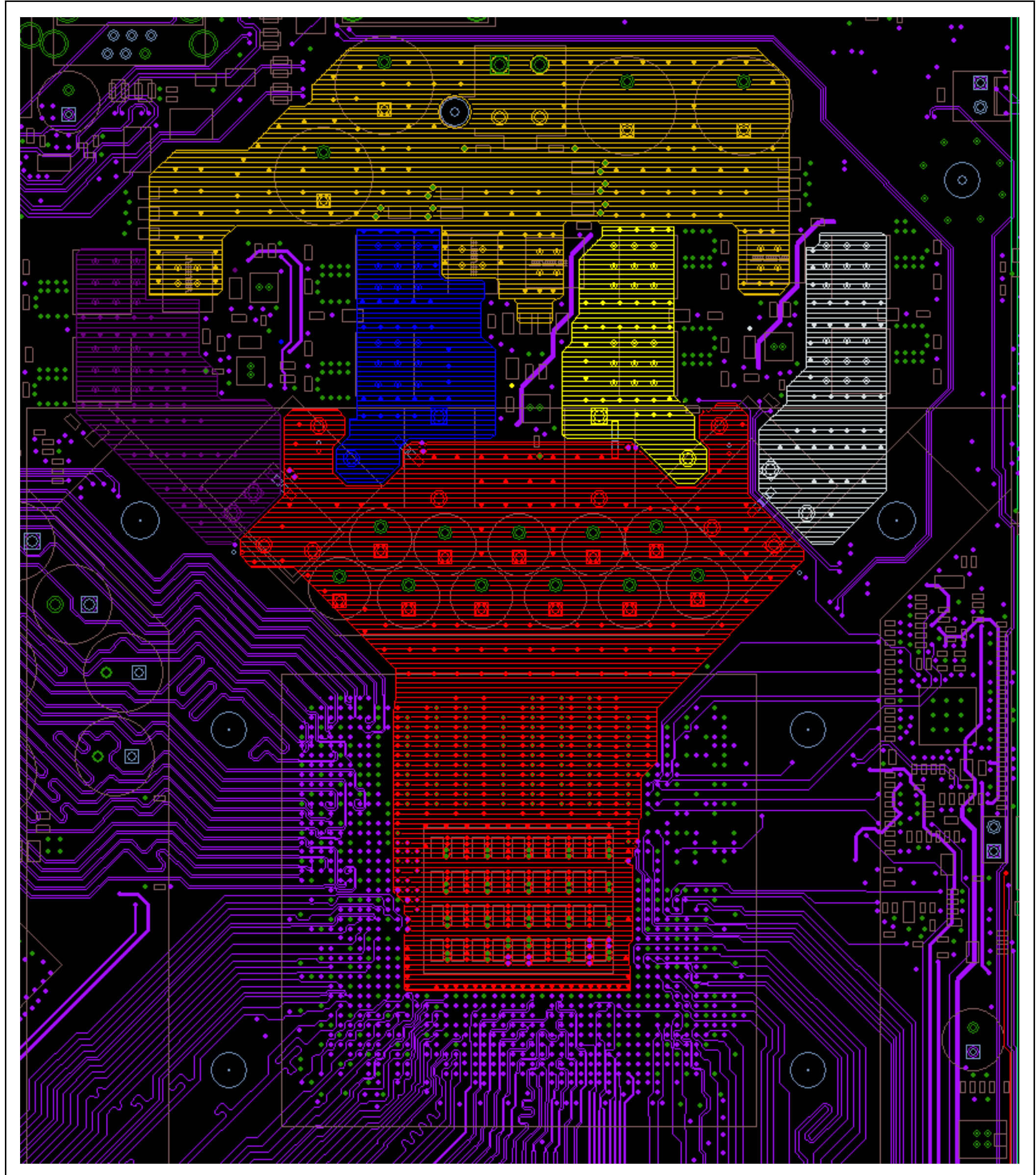


Figure 2-9. Layer 3 V_{CC} Routing for Intel® Reference Six-layer Motherboard

Figure 2-10. Layer 4 V_{CC} Shape for Intel® Reference Six-layer Motherboard



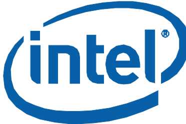
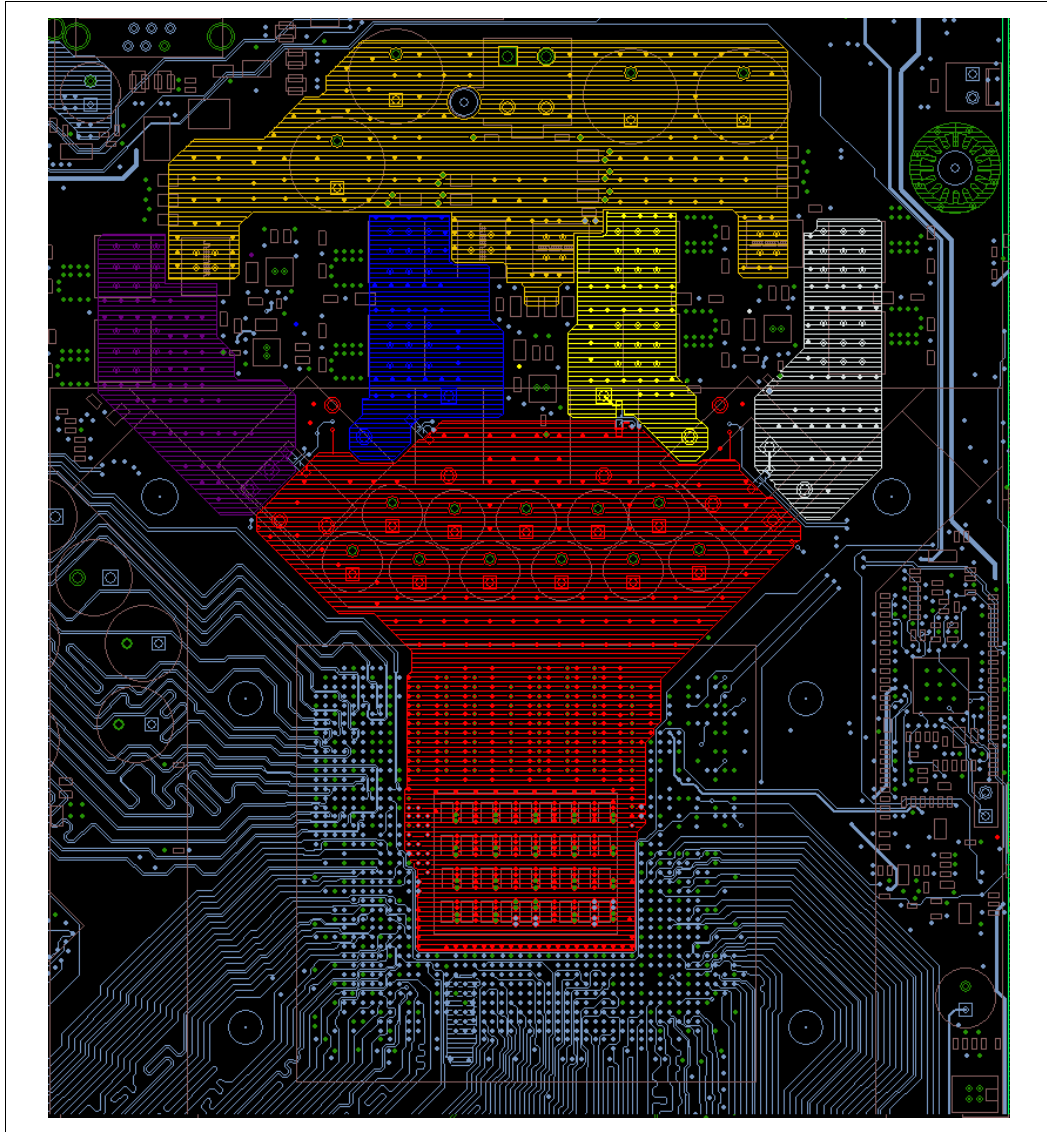


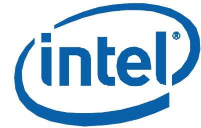
Figure 2-11. Layer 5 V_{SS} Shape for Intel® Reference Six-layer Motherboard

Figure 2-12. Layer 6 V_{CC} Shape for Intel® Reference Six-layer Motherboard



2.5.4 Resonance Suppression

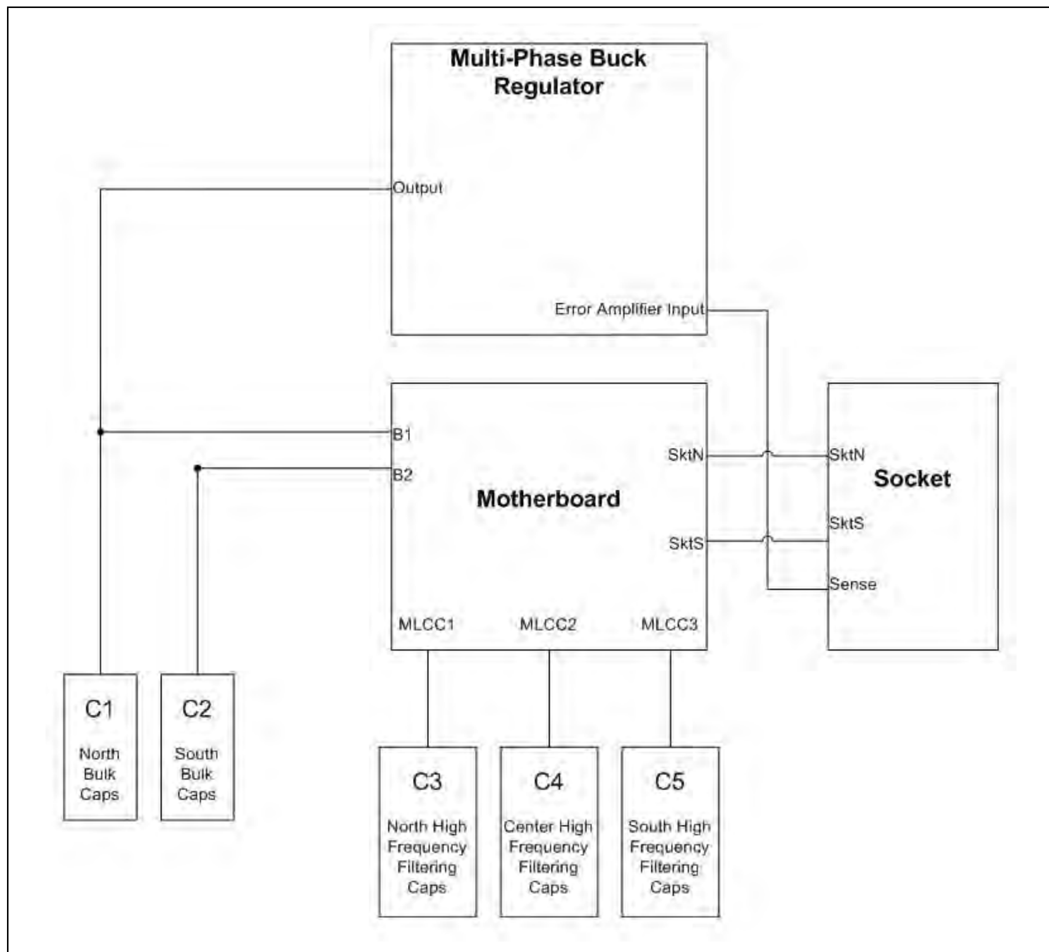
V_{CC} power delivery designs can be susceptible to resonance phenomena capable of creating droop amplitudes in violation of loadline specifications. This is due to the interleaved levels of inductively-separated decoupling capacitance. Furthermore, these resonances may not be detected through standard validation and require engineering analysis to identify and resolve. If not identified and corrected in the design process, these resonant phenomena may yield droop amplitudes in violation of loadline specifications by superimposing with standard VRD droop behavior. Frequency-dependent power delivery network impedance simulations and validation are strongly recommended to identify and resolve power delivery resonances before board are actually built. Careful modeling and validation can help to avoid voltage violations responsible for data corruption, system lock-up, or system 'blue-screening'.



2.6 Electrical Simulation (EXPECTED)

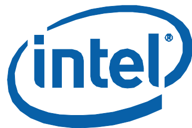
The following electrical models are enclosed to assist with VRD design analysis and component evaluation for loadline compliance. The block diagram shown in Figure 2-13 is a simplified representation of the V_{CC} power delivery network of the Intel six-layer reference board). The board model, detailed in Figure 2-16, characterizes the power plane layout of Figure 2-7 to Figure 2-10. The multiphase buck regulator and capacitor models should be obtained from each selected vendor. When fully integrated into electrical simulation software, this model can be used to evaluate PWM controller, capacitor, and inductor performance against the loadline and tolerance band requirements detailed in Section 1.3.2. To obtain accurate results, it is strongly recommended to create and use a custom model that represents the specific board design, PWM controller, and passive components that are under evaluation.

Figure 2-13. Simplified Reference Block Diagram



NOTE: Consult Figure 2-7 to Figure 2-12 for reference layout.

The motherboard model of Figure 2-16 represents the power delivery path of the Intel reference six-layer motherboard design. Input and output node locations are identified in Figure 2-17. Feedback to the PWM controller error amplifier should be tied to node



'Sense', the socket-motherboard interface. Node 'B1' is the location where the output inductors of the buck regulator ties to the motherboard power plane. 'North' bulk capacitors, C1, are also connected to node 'B1'. C1 represents the parallel combination of all capacitors and capacitor parasitics at this location. Node 'B2' is the location where the 'north' bulk capacitors, C1, connect to the 'south' bulk capacitors, C2. C2 represents the parallel combination of all capacitors and capacitor parasitics at this location. Nodes 'MLCC1', 'MLCC2', and 'MLCC3' represent the socket cavity and is connected to the mid-frequency filter, C3, C4 and C5. MLCC1, MLCC2 and MLCC3 represent the parallel combination of all capacitors and capacitor parasitics at the 'north', 'center' and 'south' of the socket cavity, respectively.

Typical capacitor models are identified in Figure 2-18. Each model represents the parallel combination of the local capacitor placement as identified in the previous paragraph. Recommended parallel values of each parameter are identified in Table 2-14. Consult Section 1.1 for further details regarding bulk and mid-frequency capacitor selection.

The LGA1366 socket is characterized by two impedance paths that connect to the motherboard at 'SktN' ('north' connection), and 'SktS' ('south' cavity connection). I_PWL is a piece-wise linear current step that is used to stimulate the voltage droop as seen at the motherboard-socket interface and is defined in Figure 2-21 and Table 2-16. This load step approximates the low frequency current spectrum that is necessary to evaluate bulk capacitor, mid-frequency capacitor and PWM controller performance. It does not provide high frequency content to excite package noise. The cavity capacitor solution, MLCC1, MLCC2 and MLCC3, are, are used as a reference for designing processor packaging material and should not be modified except to reduce ESR/ESL or increase total capacitance. <u>Failure to observe this recommendation may make the motherboard incompatible with some processor designs</u>.

The primary purpose of the simulation model is to identify options in supporting the loadline specification. Evaluation of the full power-path model will allow the designer to perform what-if analysis to determine the cost optimal capacitor and PWM controller configuration. This is especially useful in determining the capacitor configuration that can support loadline specifications across variation such as manufacturing tolerance, age degradation, and thermal drift. The designer is encouraged to evaluate different capacitor configurations and PWM controller designs. However, the designer should be aware that the feedback compensation network of most PWM controllers requires modification when the capacitor solution changes. Consult the PWM controller datasheet for further information.

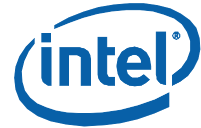


Figure 2-14. Example Voltage Droop Observed At Node 'Sense'

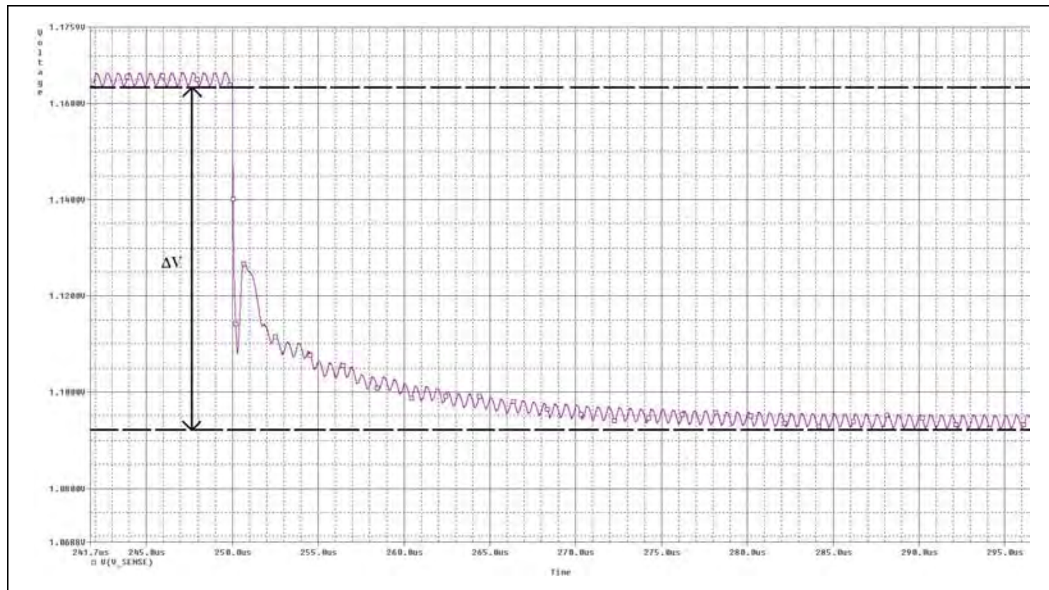
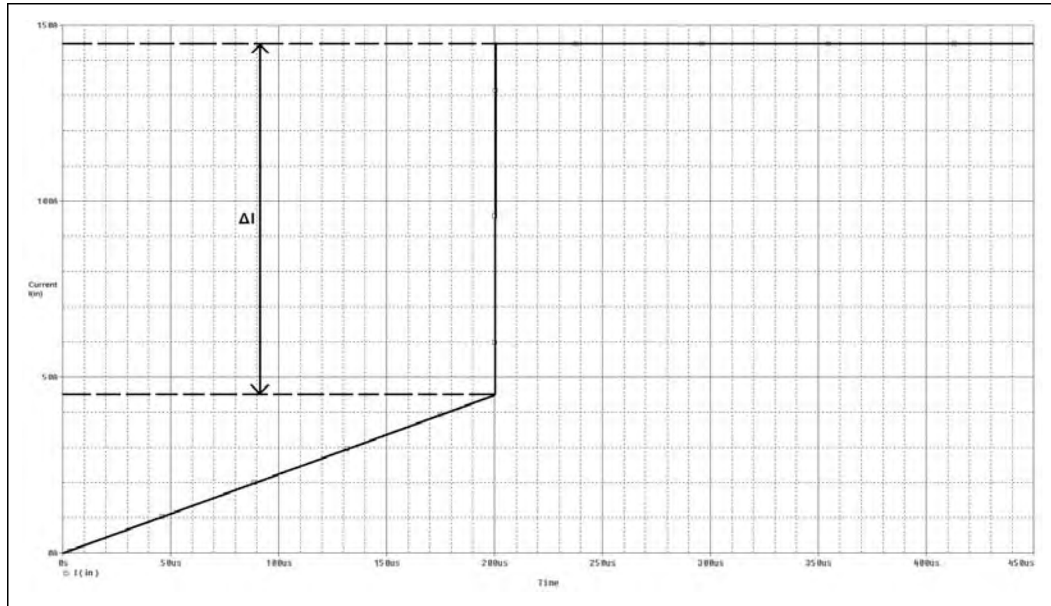


Figure 2-14 provides an example voltage droop waveform at node 'Sense', the socket-motherboard interface. The loadline value is defined as $\Delta V/\Delta I$ with ΔV measured at this node and the current step observed through I_PWL. The voltage amplitude is defined as the difference in the steady state voltage (prior to the transient) and the minimum voltage droop (consult Figure 2-14). Care must be taken to remove all ripple content in this measurement to avoid a pessimistic loadline calculation that will require additional capacitors (cost) to correct. Figure 2-15 provides an example current stimulus. The amplitude is measured as the difference in maximum current and steady state current prior to initiation of the current step. With ΔV and ΔI known, the loadline slope is simply calculated using Ohm's Law: $R_{LL} = \Delta V/\Delta I$.

Figure 2-15. Current Step Observed Through I_PWL



NOTE: To avoid excessive ringing in simulation, the system current should be slowly ramped from zero amps to the minimum recommended DC value prior to initiating the current step.

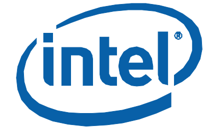
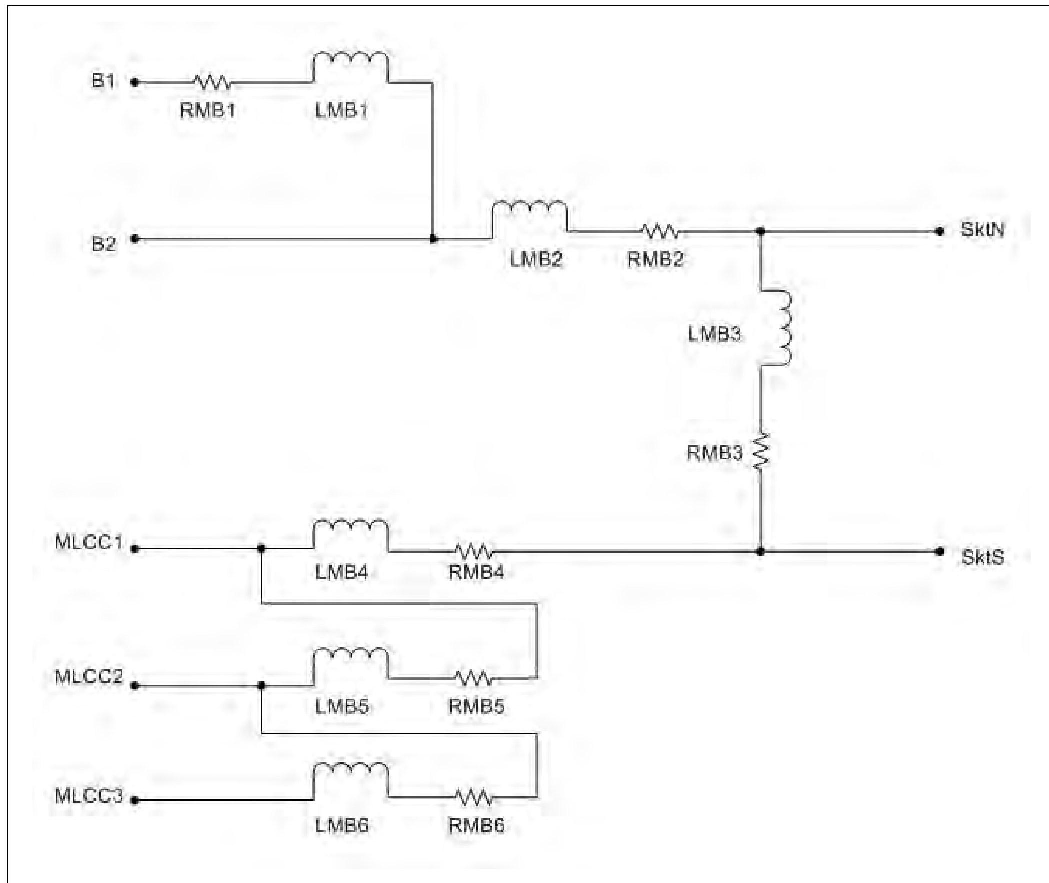


Figure 2-16. Schematic Diagram for the Six-Layer Intel® Reference Motherboard



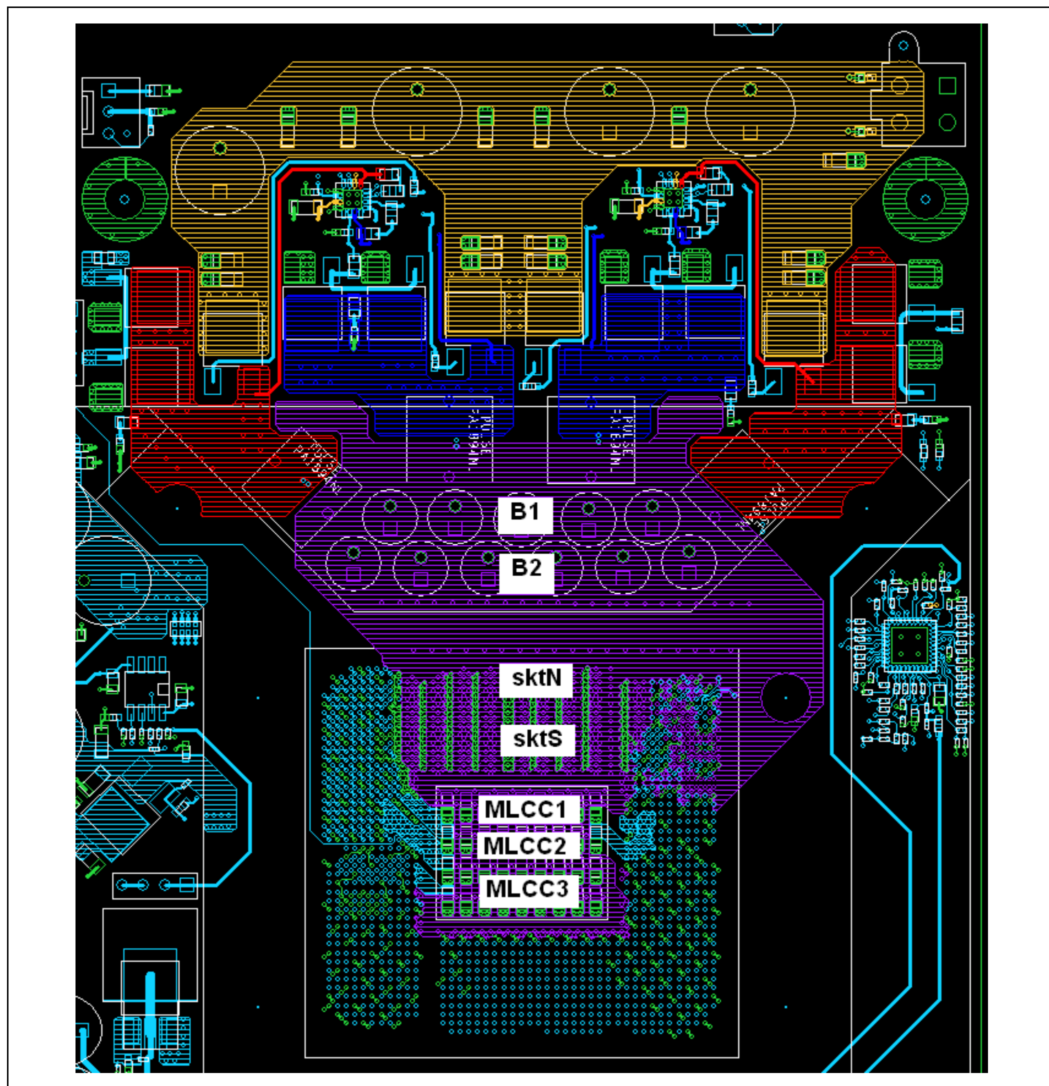
NOTE: Consult Figure 2-7 to Figure 2-10 for reference layout.

Table 2-13. Parameter Values for the Schematic of Figure 2-16

Parameter	Value	Comments
RMB1	0.12 mΩ	'North' power plane parasitic resistance from the buck regulator output inductor to the south power plane.
RMB2	0.36 mΩ	Power plane parasitic resistance from 'south' power plane from the south bulk capacitors to the 'north' LGA1366 socket connection.
RMB3	0.1 mΩ	Power plane parasitic resistance from the 'north' LGA1366 socket connection to the 'south' LGA1366 socket connection.
RMB4	0.21 mΩ	Power plane parasitic resistance from the 'south' LGA1366 socket connection to the 'north' of the LGA1366 socket cavity.
RMB5	0.12 mΩ	Power plane parasitic resistance from the 'north' of the LGA1366 socket cavity to the 'center' of the LGA1366 socket cavity.
RMB6	0.1 mΩ	Power plane parasitic resistance from the 'center' of the LGA1366 socket cavity to the 'south' of the LGA1366 socket cavity.
LMB1	15 pH	'North' power plane parasitic inductance from the buck regulator output inductor to the south power plane.

Parameter	Value	Comments
LMB2	46 pH	Power plane parasitic inductance from 'south' power plane from the south bulk capacitors to the 'north' LGA1366 socket connection.
LMB3	12 pH	Power plane parasitic inductance from the 'north' LGA1366 socket connection to the 'south' LGA1366 socket connection.
LMB4	42 pH	Power plane parasitic inductance from 'south' LGA1366 socket connection to the 'north' of the LGA1366 socket cavity.
LMB5	18 pH	Power plane parasitic inductance from the 'north' of the LGA1366 socket cavity to the 'center' of the LGA1366 socket cavity.
LMB6	10 pH	Power plane parasitic inductance from the 'center' of the LGA1366 socket cavity to the 'south' of the LGA1366 socket cavity.

Figure 2-17. Node Location for the Schematic of Figure 2-16



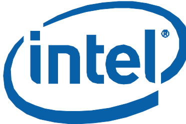


Figure 2-18. Schematic Representation of Bulk Decoupling Capacitors

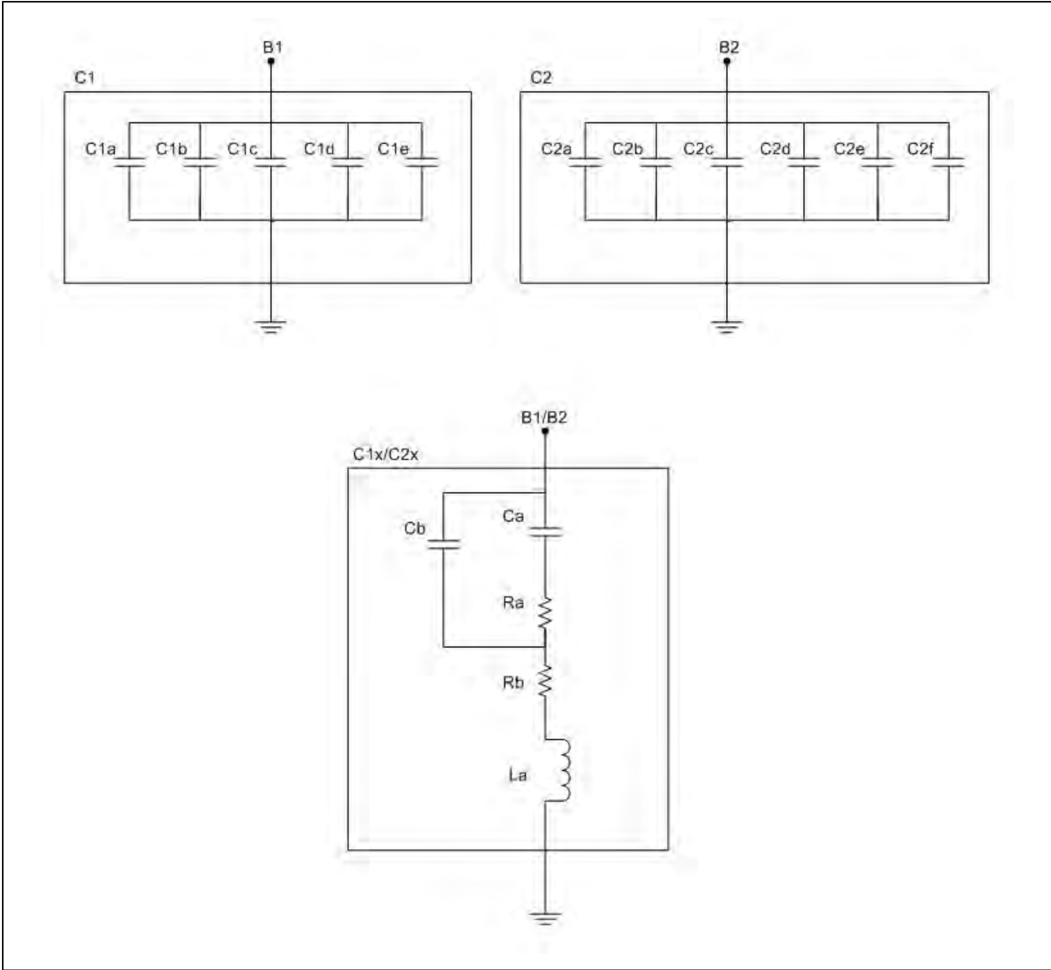
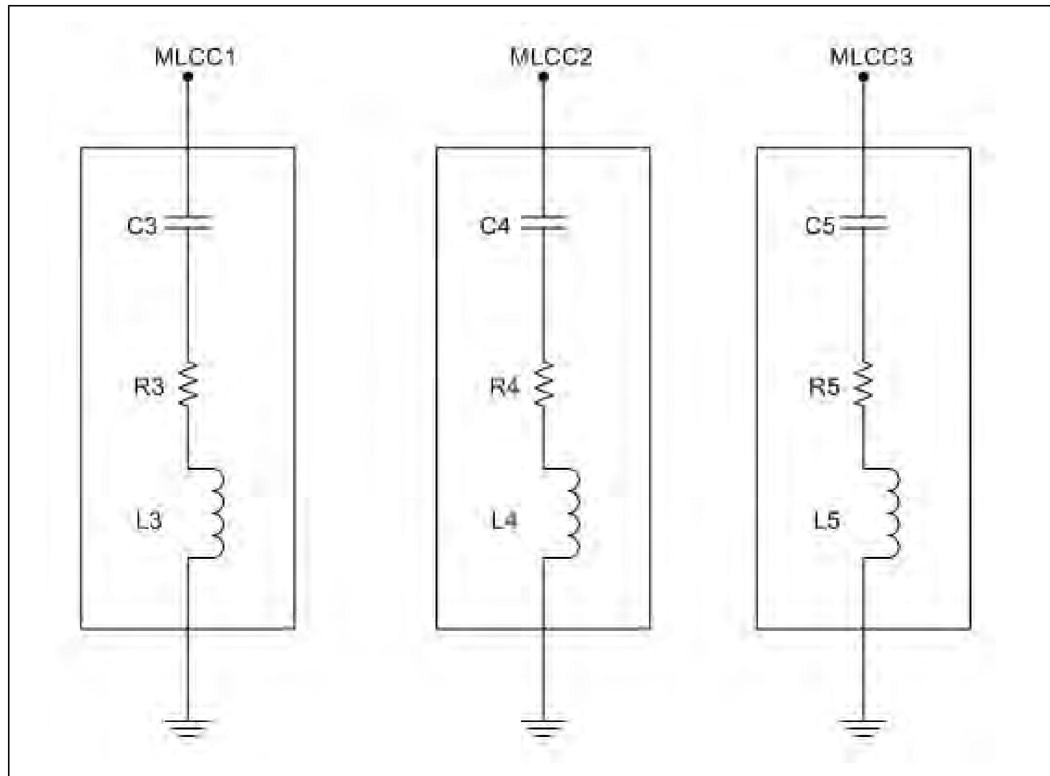


Figure 2-19. Schematic Representation of Mid-frequency Decoupling Capacitors



NOTES:
1. C1 represents the parallel model for ‘north’ location bulk decoupling.
2. C2 represents the parallel model for ‘south’ location bulk decoupling.
3. C3 represents the parallel model for mid-frequency decoupling located in the north of the socket cavity.
4. C4 represents the parallel model for mid-frequency decoupling located in the center of the socket cavity.
5. C5 represents the parallel model for mid-frequency decoupling located in the south of the socket cavity.

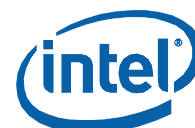


Table 2-14. Recommended Parameter Values for the Capacitors Models

Parameter	Value	Comments
Ca	120 μF[2]	Single bulk capacitor 5-element model.
Ra	80 mΩ	Single bulk capacitor 5-element model.
Cb	380 μF[2]	Single bulk capacitor 5-element model.
Rb	6 mΩ[2]	Single bulk capacitor 5-element model.
La	3 nH[1, 2]	Single bulk capacitor 5-element model.
C3	129 μF[2]	Parallel equivalent for ‘north cavity’ capacitors prior to age, thermal, and manufacturing degradation.
R3	556 μΩ[2]	Parallel equivalent for ‘north cavity’ capacitor maximum ESR.
L3	61.2 pH[1, 2]	Parallel equivalent for ‘north cavity’ capacitor maximum ESL.
C4	100 μF[2]	Parallel equivalent for ‘center cavity’ capacitors prior to age, thermal, and manufacturing degradation.
R4	714 μΩ[2]	Parallel equivalent for ‘center cavity’ capacitor maximum ESR.
L4	78.7 pH[1, 2]	Parallel equivalent for ‘center cavity’ capacitor maximum ESL.
C5	57 μF[2]	Parallel equivalent for ‘south cavity’ capacitors prior to age, thermal, and manufacturing degradation.
R5	1.25 mΩ[2]	Parallel equivalent for ‘south cavity’ capacitor maximum ESR.
L5	138 pH[1, 2]	Parallel equivalent for ‘south cavity’ capacitor maximum ESL.

NOTES:
1. Higher values of ESL may satisfy design requirements.
2. Contact capacitor vendors to identify values for the specific components used in your design

Figure 2-20. Schematic Representation of Socket Model

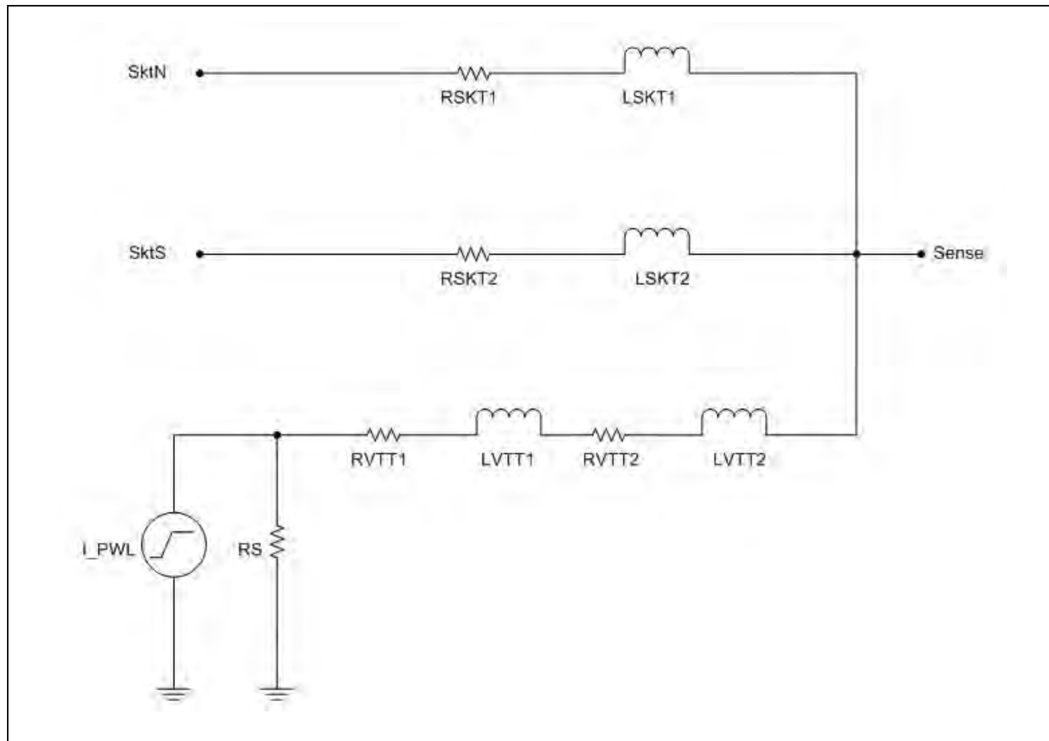


Table 2-15. Recommended Parameter Values for the Socket Model in Figure 2-20

Parameter	Value	Comments
RSKT1	0.4 mΩ	LGA1366 'north' segment resistance
RSKT2	0.4 mΩ	LGA1366 'south' segment resistance
RVTT1	0.42 mΩ	Resistance of VTT Tool load board
RVTT2	0.91 mΩ	Resistance of VTT Tool socket adapter (interposer)
RS	100 kΩ	VTT Tool current source resistance
LSKT1	50 pH	LGA1366 'north' segment inductance
LSKT2	40pH	LGA1366 'south' segment inductance
LVTT1	240 pH	Inductance of VTT Tool load board
LVTT2	42 pH	Inductance of VTT Tool socket adapter (interposer)

NOTES: These values are from the LGA 775 VTT Tool load board. The values will be updated with values from the LGA 1366 VTT Tool load board when they become available.

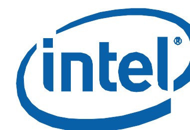


Figure 2-21. Current Load Step Profile for I_PWL

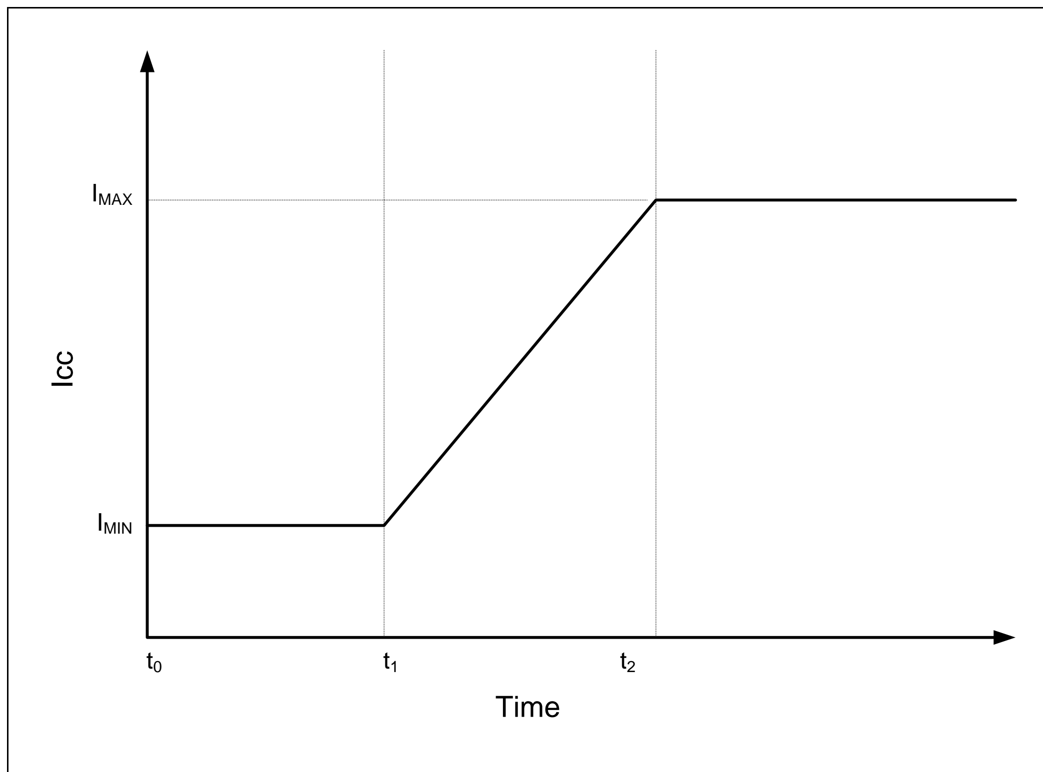
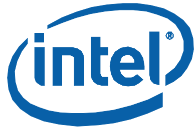


Table 2-16. I_PWL Current Parameters for Figure 2-21

Parameter	Value	Comments
t_0	0 s	Simulation 'time zero'
t_1	100 µs	Time to initiate the current step. This parameter must be chosen at a time that the V_{CC} rail is residing at steady state.
t_2	t_1 + 200 ns	Time of maximum current[1]
Istep	100 A	Current step for loadline testing[1]
Imin	45 A	Minimum current for simulation analysis[1]
Imax	145 A	Maximum current for simulation analysis[1]

NOTE:

1. See Table 2-5. Intel® Processor Current Step Values for Transient Loadline Testing



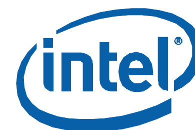
2.7 LGA1366 Voltage Regulator Configuration Parameters

2.7.1 1366_VR_CONFIG_08B

Table 2-17. 1366_VR_CONFIG_08B Specification Input Parameters

Definition	Variable Name	Value
Loadline Slope	LL_SLOPE	0.8 mΩ
Loadline Tolerance Band	TOB	19 mV
Maximum Overshoot Above VID	OS_AMP	50 mV
Maximum Overshoot Time Duration Above VID	OS_TIME	25 us
Peak To Peak Ripple Amplitude	RIPPLE	10 mV
Thermal Compensation Voltage Drift	THERMAL_DRIFT	2 mV
Iccmax	Iccmax	145 A
Dynamic Current Step	I_STEP	100 A
Maximum DC Test Current	I_DC_MAX	45 A
Minimum DC Test Current	I_DC_MIN	5 A
Voltage Regulator Thermal Design Current	VR_TDC	110 A
Current step rise time	I_RISE	200 ns
Current step fall time for overshoot	I_FALL	200 ns

§



3 LGA775 Information

3.1 Introduction

This chapter focuses on information unique to platforms designed with the LGA 775.

3.2 Processor V_{CC} Requirements

3.2.1 Socket Loadline Definitions (REQUIRED)

To maintain processor reliability and performance, platform DC voltage regulation and transient-droop noise levels must always be contained within the Vccmin and Vccmax socket loadline boundaries (known as the loadline window). Socket loadline compliance must be ensured across 3-σ component manufacturing tolerances, thermal variation, and age degradation. Socket loadline boundaries are defined by the following equations in conjunction with the V_{CC} regulator design parameter values defined in Table 3-2. In these equations, VID, R_{LL}, and TOB are known. Plotting V_{CC} while varying I_{CC} from 0 A to Iccmax establishes the Vccmax and Vccmin socket loadlines. Vccmax establishes the maximum DC socket loadline boundary. Vccmin establishes the minimum AC and DC voltage boundary. Short transient bursts above the Vccmax loadline are permitted; this condition is defined in Section 1.3.7.

Table 3-1. Socket Loadline Equations

Socket loadline	Equation
Equation 8: Vccmax Socket loadline	V_{CC} = VID – (R_{LL}* I_{CC})
Equation 9: Vcctyp Socket loadline	V_{CC} = VID – TOB - (R_{LL}* I_{CC})
Equation 10: Vccmin Socket loadline	V_{CC} = VID – 2*TOB - (R_{LL}* I_{CC})

Socket loadline recommendations are established to provide guidance for satisfying processor die loadline specifications, which are defined in processor datasheets. Die loadline requirements must be satisfied at all times and may require adjustment in the socket loadline value. The processor die loadlines are defined in the applicable processor datasheet.

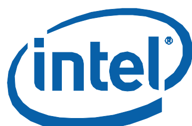


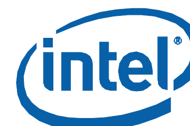
Table 3-2. V_{CC} Regulator Design Parameters

VR Configuration	Iccmax	VR TDC	Dynamic I_{CC}	RLL	TOB	Max VID
775_VR_CONFIG_04A	78 A	68 A	55 A	1.40 mΩ	±25 mV	1.4 V
775_VR_CONFIG_04B	119 A	101 A	95 A	1.00 mΩ	±19 mV	1.4 V
775_VR_CONFIG_05A	100 A	85 A	65 A	1.00 mΩ	±19 mV	1.4 V
775_VR_CONFIG_05B	125 A	115 A	95 A	1.00 mΩ	±19 mV	1.4 V
775_VR_CONFIG_06	75 A	60 A	50 A	1.00 mΩ	±19 mV	1.425 V

VRD transient socket loadline circuits should be designed to meet or exceed rated conditions defined in Table 3-2. For example, 775_VR_CONFIG_04A requires a socket loadline slope of 1.40 mΩ. A transient socket loadline slope of 1.0 mΩ will satisfy this requirement without adversely impacting system performance or processor lifespan. This condition may be necessary when supporting multiple processors with a single VRD design. However, the static loadline condition must be set to the recommended value unless explicitly stated otherwise in the processor datasheet. Operating at a low loadline resistance will result in higher processor operating temperature, which may result in damage or a reduced processor life span. Processor temperature rise from higher functional voltages may lead to operation at low power states which directly reduces processor performance. Operating at a higher loadline resistance will result in minimum voltage violations which may result in system lock-up, "blue screening", or data corruption.

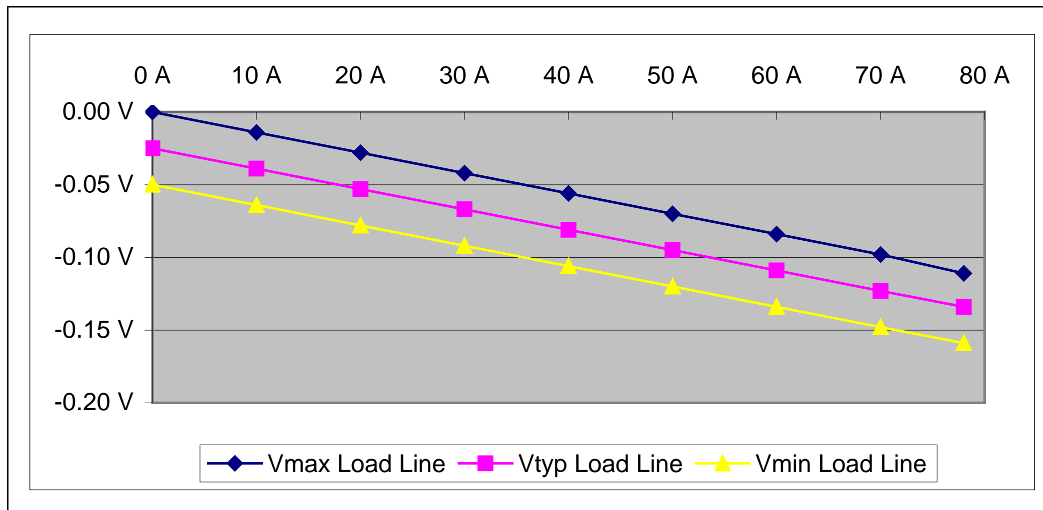
Table 3-2 provides a comprehensive list of VRD11 LGA775 voltage regulator design configurations. The configurations to be adopted by VRD hardware will depend on the specific processors the design is intended to support. It is common for a motherboard to support processors that require different VR configurations. In this case, the V_{CC} regulator design must meet the specifications of all processors supported by that board. For example, If a motherboard is targeted to support processors that require 775_VR_CONFIG_04A and 775_VR_CONFIG_04B, then the voltage regulator must have the ability to support 101 A of VR TDC, 119 A of electrical peak current, satisfy overshoot requirements of the Processor V_{CC} Overshoot Section with a dynamic load step of 95 A, satisfy a VRD tolerance band of ±19 mV.

The following tables and figures show minimum and maximum voltage boundaries for each socket loadline design configuration defined in Table 3-2. V_{CCTYP} socket loadlines are provided for design reference; designs should calibrate the socket loadline to this case (centered in the loadline window, at the mean of the tolerance band). Different processors discussed in this design guide can be shipped with different VID values. The reader should not assume that processors with similar characteristics will have the same VID value. Typical values will range from 1.1 V to 1.6 V in 6.25 mV increments. A single loadline chart and figure for each VRD design configuration can represent functionality for each possible VID value. Tables and figures presented as voltage deviation from VID provide the necessary information to identify voltage requirements at any reference VID. This avoids the redundancy of publishing tables and figures for each of the multiple cases.



3.2.1.1 Socket Loadline Definition for 775_VR_CONFIG_04A

Figure 3-1. Socket Loadline Window for 775_VR_CONFIG_04A



NOTES:

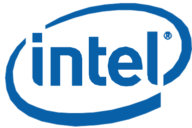
1. Presented as a deviation from VID
2. Socket loadline Slope = 1.4 mΩ, TOB = ±25 mV
3. Consult Table 3-2 for VR configuration parameter details

Table 3-3. Socket Loadline Window for 775_VR_CONFIG_04A

I_{CC}	Maximum	Typical	Minimum
0 A	0.000 V	-0.025 V	-0.050 V
10 A	-0.014 V	-0.039 V	-0.064 V
20 A	-0.028 V	-0.053 V	-0.078 V
30 A	-0.042 V	-0.067 V	-0.092 V
40 A	-0.056 V	-0.081 V	-0.106 V
50 A	-0.070 V	-0.095 V	-0.120 V
60 A	-0.084 V	-0.109 V	-0.134 V
70 A	-0.098 V	-0.123 V	-0.148 V
78 A	-0.111 V	-0.134 V	-0.159 V

NOTES:

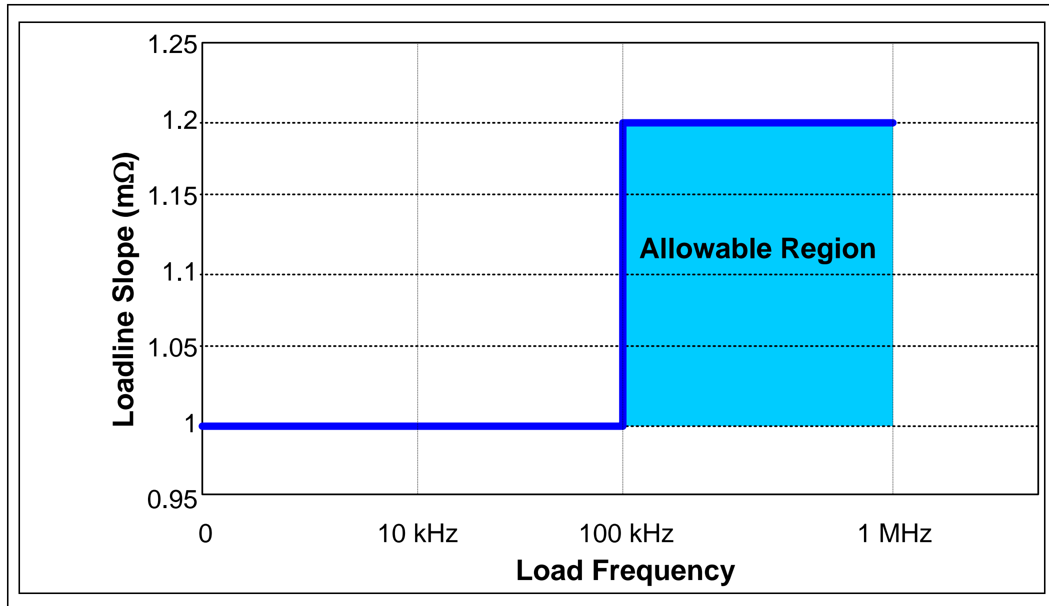
1. Presented as a deviation from VID
2. Socket loadline Slope = 1.4 mΩ, TOB = ±25 mV
3. Consult Table 3-2 for VR configuration parameter details



3.2.1.2 Socket Loadline Definition for 775_VR_CONFIG_04B, 05A, 05B, 06

The socket loadline for 775_VR_CONFIG_04B, 05A, 05B and 06 can be implemented in a piece-wise linear fashion. The socket loadline should have a 1 mΩ slope when the load frequency content is in the range of 0 to 100 kHz. When the load frequency is in the range of >100 kHz to 1 MHz, a loadline slope of up to 1.2 mΩ is allowed. See Figure 3-2.

Figure 3-2. Piece-wise Linear Socket Loadline



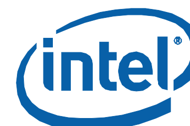
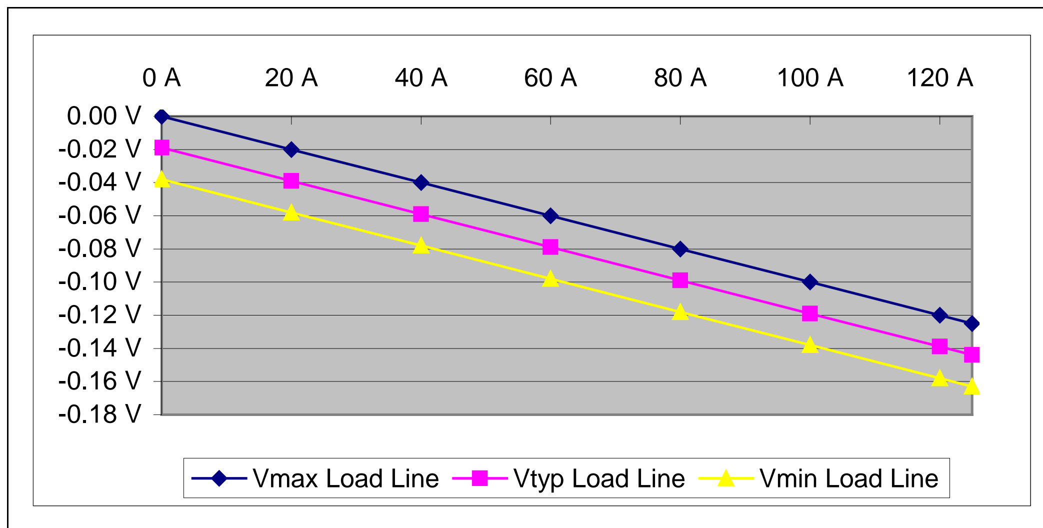


Figure 3-3. Socket Loadline Window for 775_VR_CONFIG_04B, 05A, 05B (0–100 kHz loadstep rate)



NOTES:

1. Presented as a deviation from VID
2. Socket loadline Slope = 1.0 mΩ, TOB = ±19 mV
3. Consult Table 3-2 for VR configuration parameter details

Table 3-4. Socket Loadline Window for 775_VR_CONFIG_04B, 05A, 05B (0–100 kHz loadstep rate)

I_{CC}	Maximum	Typical	Minimum
0 A	0.000 V	-0.019 V	-0.038 V
20 A	-0.020 V	-0.039 V	-0.058 V
40 A	-0.040 V	-0.059 V	-0.078 V
60 A	-0.060 V	-0.079 V	-0.098 V
80 A	-0.080 V	-0.099 V	-0.118 V
100 A	-0.100 V	-0.119 V	-0.138 V
120 A	-0.120 V	-0.139 V	-0.158 V
125 A	-0.125 V	-0.144 V	-0.163 V

NOTES:

1. Presented as a deviation from VID
2. Socket loadline Slope = 1.0 mΩ, TOB = ±19 mV
3. Consult Table 3-2 for VR configuration parameter details

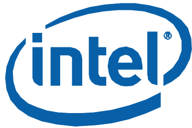
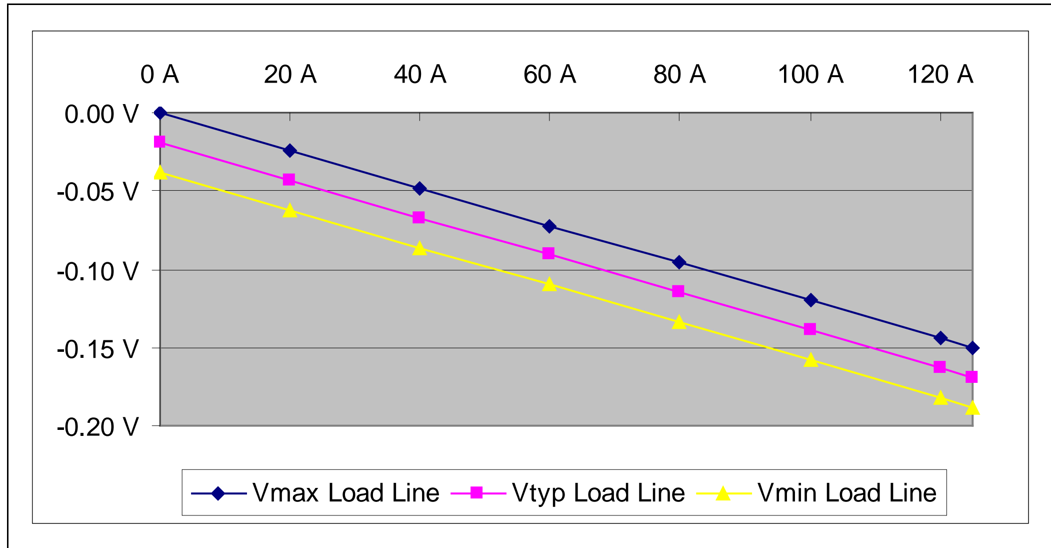


Figure 3-4. Socket Loadline Window for 775_VR_CONFIG_04B, 05A, 05B (>100 kHz–1 MHz loadstep Rate)



NOTES:

1. Presented as a deviation from VID
2. Socket loadline Slope = 1.2 mΩ, TOB = ±19 mV
3. Consult Table 3-2 for VR configuration parameter details

Table 3-5. Socket Loadline Window for 775_VR_CONFIG_04B, 05A, 05B (>100 kHz-1 MHz loadstep Rate)

I_{CC}	Maximum	Typical	Minimum
0 A	0.000 V	-0.019 V	-0.038 V
20 A	-0.024 V	-0.043 V	-0.062 V
40 A	-0.048 V	-0.067 V	-0.086 V
60 A	-0.072 V	-0.091 V	-0.110 V
80 A	-0.096 V	-0.115 V	-0.134 V
100 A	-0.120 V	-0.139 V	-0.158 V
120 A	-0.144 V	-0.163 V	-0.182 V
125 A	-0.150 V	-0.169 V	-0.188 V

NOTES:

1. Presented as a deviation from VID
2. Socket loadline Slope = 1.2 mΩ, TOB = ±19 mV
3. Consult Table 3-2 for VR configuration parameter details

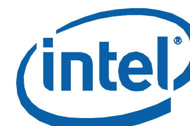
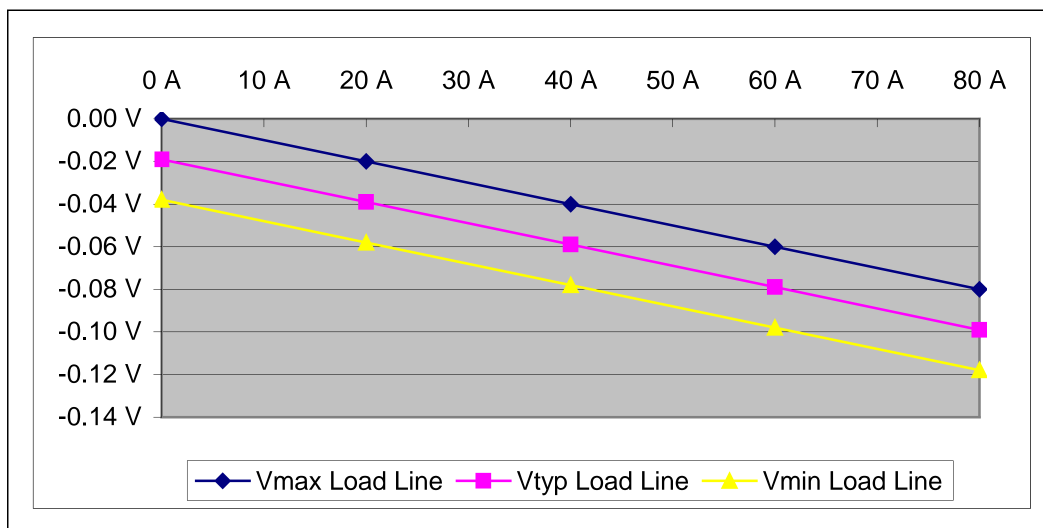


Figure 3-5. Socket Loadline Window for Design Configurations 775_VR_CONFIG_06 (0–100 kHz Loadstep Rate)



NOTES:

1. Presented as a deviation from VID
2. Socket loadline Slope = 1.0 mΩ, TOB = ±19 mV
3. Consult Table 3-2 for VR configuration parameter details

Table 3-6. Socket Loadline Window for 775_VR_CONFIG_06 (0–100 kHz Loadstep Rate)

I_{CC}	Maximum	Typical	Minimum
0 A	0.000 V	-0.019 V	-0.038 V
20 A	-0.020 V	-0.039 V	-0.058 V
40 A	-0.040 V	-0.059 V	-0.078 V
60 A	-0.060 V	-0.079 V	-0.098 V
80 A	-0.080 V	-0.099 V	-0.118 V

NOTES:

1. Presented as a deviation from VID
2. Socket loadline Slope = 1.0 mΩ, TOB = ±19 mV
3. Consult Table 3-2 for VR configuration parameter details

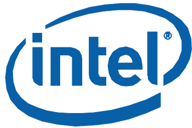
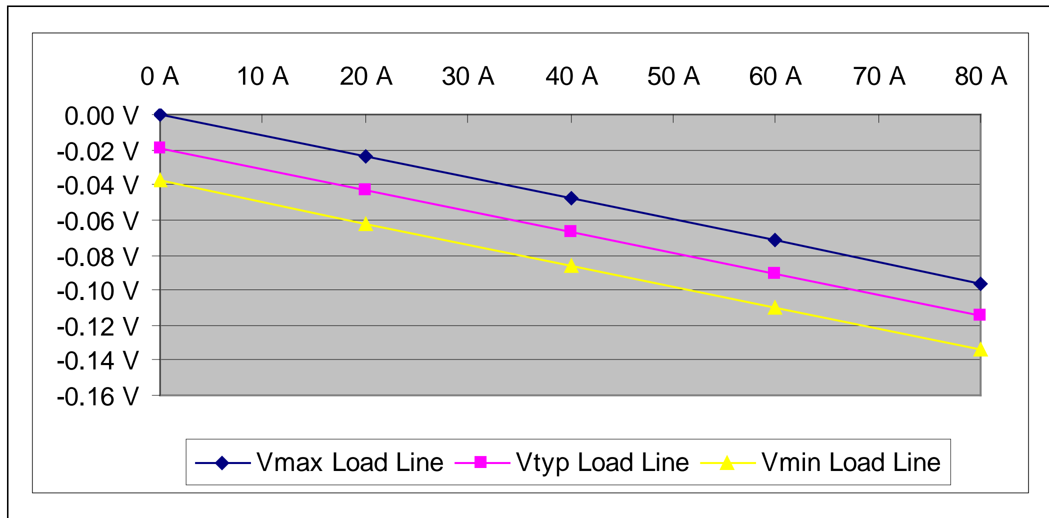


Figure 3-6. Socket Loadline Window for Design Configurations 775_VR_CONFIG_06 (>100 kHz-1 MHz Loadstep Rate)



NOTES:
1. Presented as a deviation from VID
2. Socket loadline Slope = 1.2 mΩ, TOB = ±19 mV
3. Consult Table 3-2 for VR configuration parameter details

Table 3-7. Socket Loadline Window for 775_VR_CONFIG_06 (>100 kHz–1 MHz Loadstep Rate)

I_{CC}	Maximum	Typical	Minimum
0 A	0.000 V	-0.019 V	-0.038 V
20 A	-0.024 V	-0.043 V	-0.062 V
40 A	-0.048 V	-0.067 V	-0.086 V
60 A	-0.072 V	-0.091 V	-0.110 V
80 A	-0.096 V	-0.115 V	-0.134 V

NOTES:
1. Presented as a deviation from VID
2. Socket loadline Slope = 1.2 mΩ, TOB = ±19 mV
3. Consult Table 3-2 for VR configuration parameter details

Reference nodes for socket loadline measurements and voltage regulation are located in the land field between the socket cavity and the voltage regulator region. See Figure 3-7 VRD Phase Orientation. References for north phase configurations are identified in Table 3-8. It is recommended to place motherboard test points at this location to enable loadline calibration.

VRD layout studies indicate that the highest phase count is best located north of the processor with the controller to the southeast.

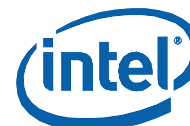
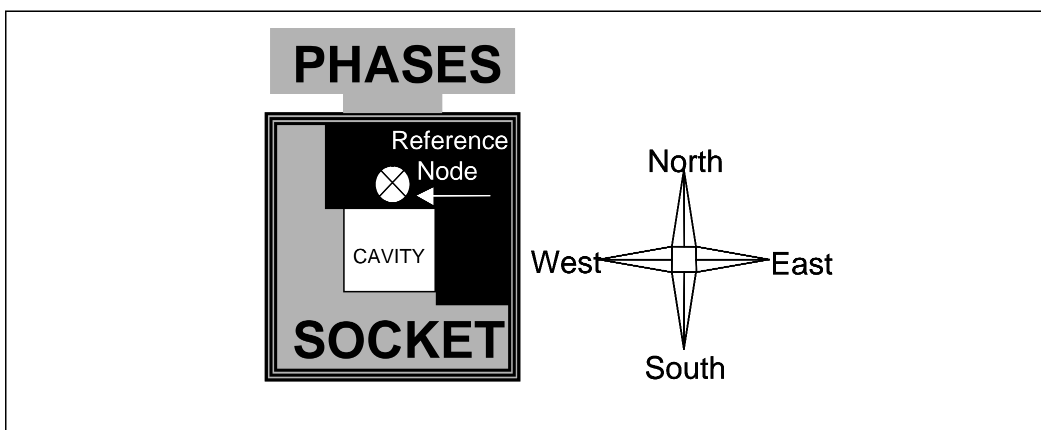


Table 3-8. Socket Loadline Reference Lands

Orientation	Land
VCC_MB_SENSE (North Vcc)	U27
VSS_MB_SENSE (North V_{SS})	V26
VCC_MB_REGULATION (SE Vcc Jumper)	AN5
VSS_MB_REGULATION (SE V_{SS} Jumper)	AN6
VCC_DIE_SENSE	AN3
VSS_DIE_SENSE	AN4

Figure 3-7. VRD Phase Orientation



To properly calibrate the socket loadline parameter, the VR designer must excite the processor socket with a current step that generates a voltage droop which must be checked against the loadline window requirements. Table 3-9 identifies the steady state and transient current values to use for this calibration.

Table 3-9. Intel® Processor Current Step Values for Transient Socket loadline Testing

VR Configuration	Starting Current	Ending Current	Dynamic Current Step	I_{CC} Rise Time
775_VR_CONFIG_04A	23 A	78 A	55 A	83 A/µs
775_VR_CONFIG_04B	24 A	119 A	95 A	83 A/µs
775_VR_CONFIG_05A1	20 A	85 A	65 A	50 ns
775_VR_CONFIG_05B1	30 A	125 A	95 A	50 ns
775_VR_CONFIG_061	25 A	75 A	50 A	50 ns

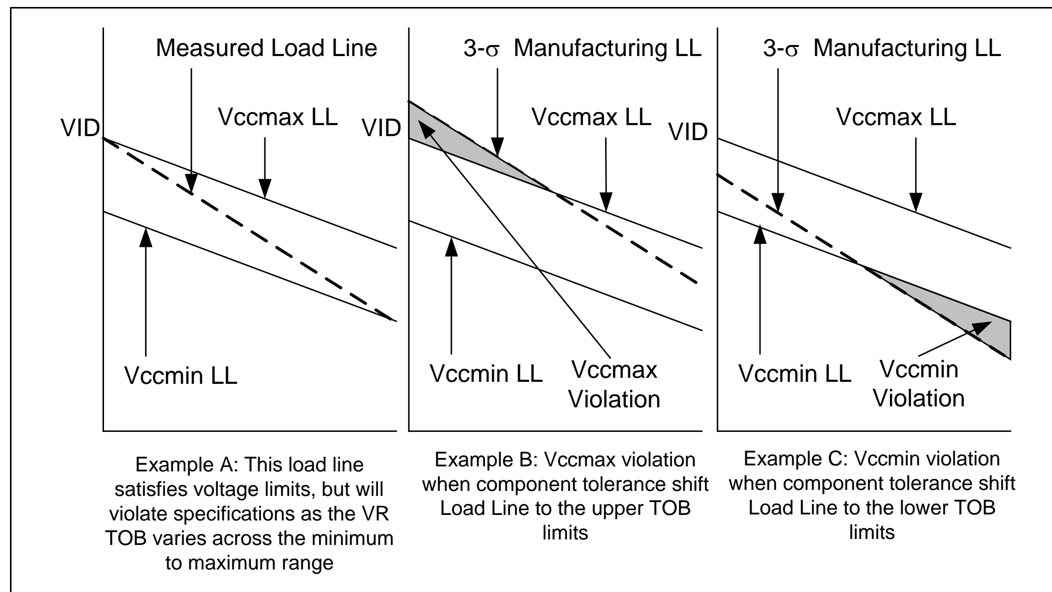
NOTES:

1. 775_VR_CONFIG_05A and 775_VR_CONFIG_05B configurations may be used with some board configurations

VRD designs must be socket loadline compliant across the full tolerance band window to avoid data corruption, system lock-up, and reduced performance. When validating a system's socket loadline, a single measurement is statistically insignificant and cannot represent the response variation seen across the entire high volume manufacturing population of VRD designs. A typical socket loadline may fit in the specification window; however designs residing elsewhere in the tolerance band distribution may violate the specifications. Figure 3-8 Example A shows a loadline that is contained in the specification window and, this single instance, complies with Vccmin and Vccmax specifications. The positioning of this socket loadline will shift up and down as the tolerance drifts from typical to the design limits. Figure 3-8 Example B shows that Vccmax limits will be violated as the component tolerances shift the loadline to the upper tolerance band limits. Figure 3-8 Example C shows that the Vccmin limits will be violated as the component tolerances shift the loadline to the lower tolerance band limits.

To satisfy specifications across high volume manufacturing variation, a typical socket loadline must be centered in the loadline window and have a slope equal to the value specified in Table 3-2. Figure 3-9 Example A shows a socket loadline that meets this condition. Under full 3-σ tolerance band variation, the loadline slope will intercept the Vccmax loadline (Figure 3-9 Example B) or Vccmin loadline (Figure 3-9 Example C) limits.

Figure 3-8. Examples of High Volume Manufacturing Loadline Violations



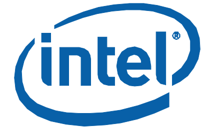
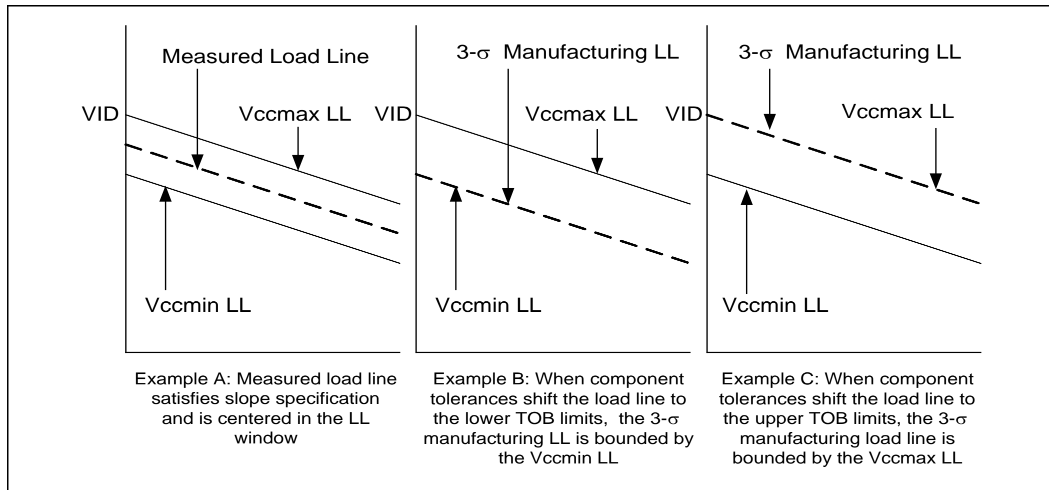


Figure 3-9. High Volume Manufacturing Compliant Loadline

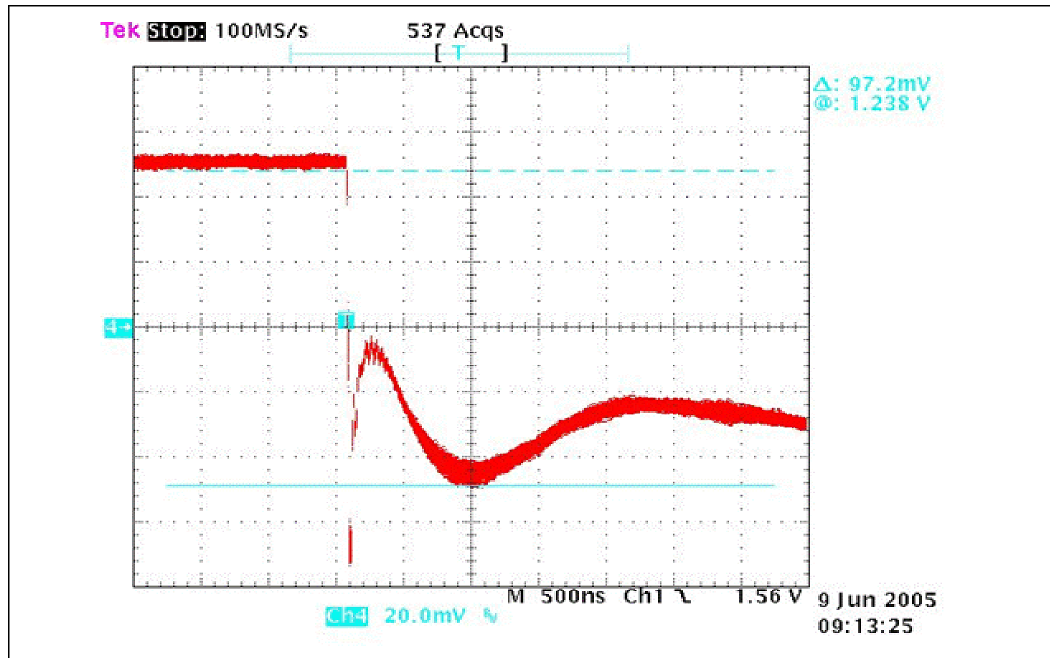


3.2.1.3 Time Domain Validation

To ensure processor reliability and performance, platform transient-droop and overshoot noise levels must always be contained within the Vccmin and Vccmax socket loadline boundaries (known as the loadline window). The load generates a voltage droop, or overshoot, which must be checked against the loadline window requirements. The current step must have a fast enough slew rate to excite the impedance across the frequency range of the VR. In addition, the VR needs to be tested at different load frequencies and load steps to prevent any non-linear, resonant, or beating effects that could cause functional issues or loadline violations. Intel recommends sweeping the load frequency from DC to 1 MHz, using two different load steps.

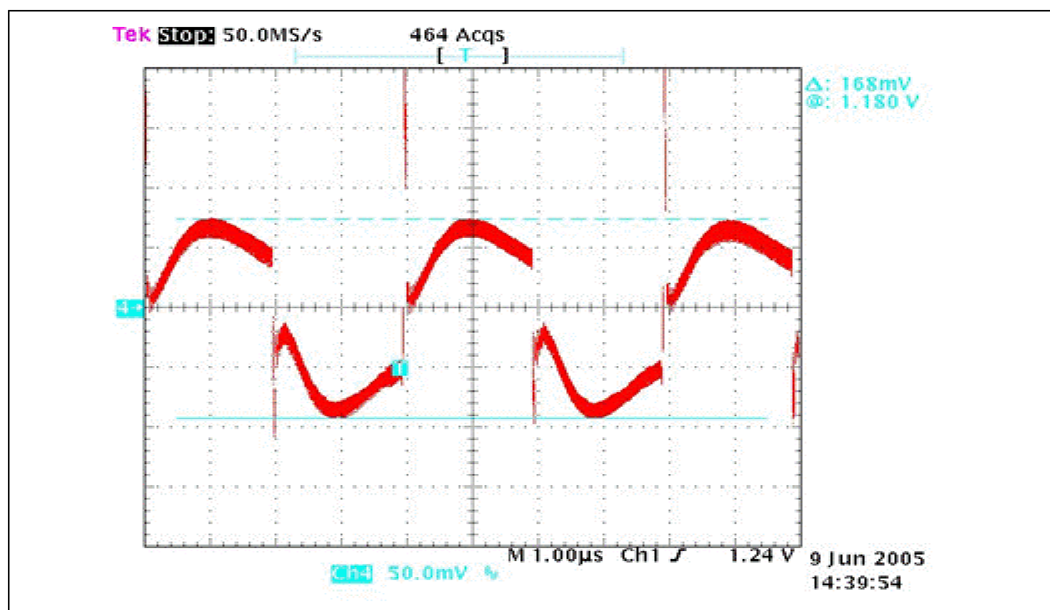
Intel recommends testing using different VID levels for each of the supported VR configurations. In particular the highest and lowest VIDs should be checked. The VID ranges for each processor is available in the processor datasheet.

Figure 3-10. 200 Hz, 100 A Step Droop Waveform

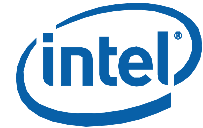


NOTE: The cursor indicates the droop area of interest. A falling edge with a width less than 100 ns can be ignored.

Figure 3-11. 250 kHz, 100 A Step Waveform



NOTE: The cursor indicates the droop area of interest. A falling edge with a width less than 100 ns can be ignored.

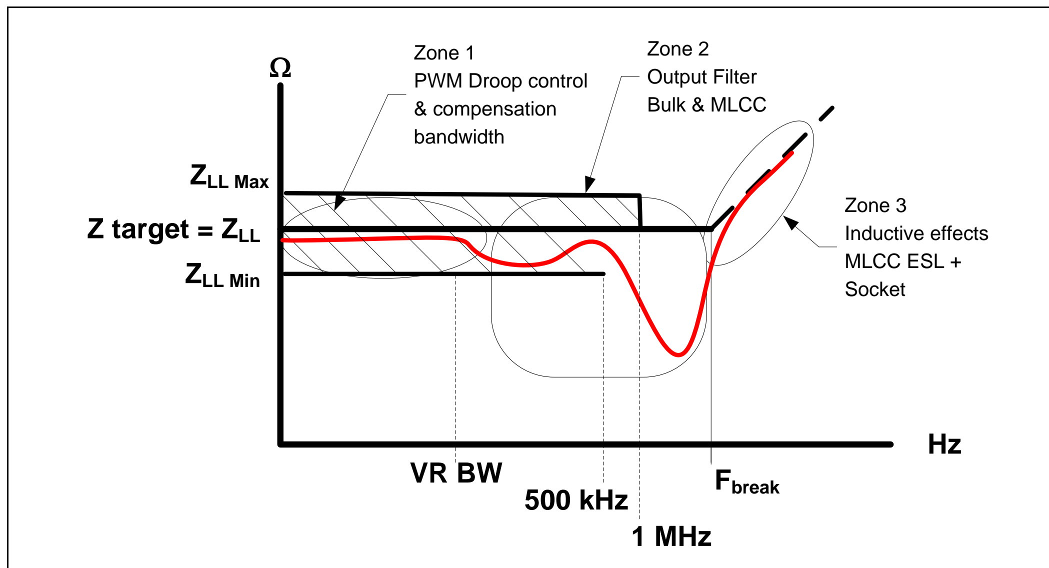


3.2.1.4 Platform Impedance Measurement and Analysis (Expected)

In addition to the tuning of the loadline with Vdroop testing and DC loadline testing, the decoupling capacitor selection needs to be analyzed to make sure the impedance of the decoupling is below the loadline target up to the frequency F_{break} as defined in Figure 2-4. This analysis can be done with impedance testing or through power delivery simulation if the designer can extract the parasitic resistance and inductance of the power planes on the motherboard and they have good models for the decoupling capacitors.

Measured power delivery impedance should be with in the tolerance band shown in Figure 3-12. For Loadline compliance, time domain validation is required and the VR tolerance band must be met at all times. Above 500 kHz, the minimum impedance tolerance is not defined and is determined by the MLCC capacitors required to get the ESL low enough to meet the loadline impedance target at the F_{break} frequency. At 1 MHz, the Zmax tolerance drops to the loadline target impedance. Any resonance points that are above the Zmax line need to be carefully evaluated with time domain method defined in Section 3.2.1.3 by applying transient loads at that frequency and looking for Vmin violations. Maintaining the impedance profile up to F_{break} is important to ensure the package level decoupling properly matches the motherboard impedance. After F_{break}, the impedance measurement is permitted to rise at a inductive slope. The motherboard VR designer does not need to design for frequencies over F_{break} as the processor package decoupling takes over in the region above F_{break}.

Figure 3-12. Power Distribution Impedance versus Frequency



NOTES:

1. See Table 3-10. Impedance Measurement Parameters definitions
2. Zone 1 is defined by the VR closed loop compensation bandwidth (VR BW) of the voltage regulator. Typically 30–40 kHz for a 300 kHz voltage regulator design.
3. Zones 2 and 3 are defined by the output filter capacitors and interconnect parasitic resistance and inductance. The tolerance is relaxed over 500 kHz allowing the VR designer freedom to select output filter capacitors. The goal is to keep Z(f) below Z_{LL} up to Fbreak and as flat as practical, by selection of bulk capacitor values and type and number of MLCC capacitors. The ideal impedance would be between Z_{LL} and Z_{LL} Min but this may not be achieved with standard decoupling capacitors.

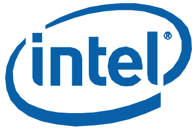
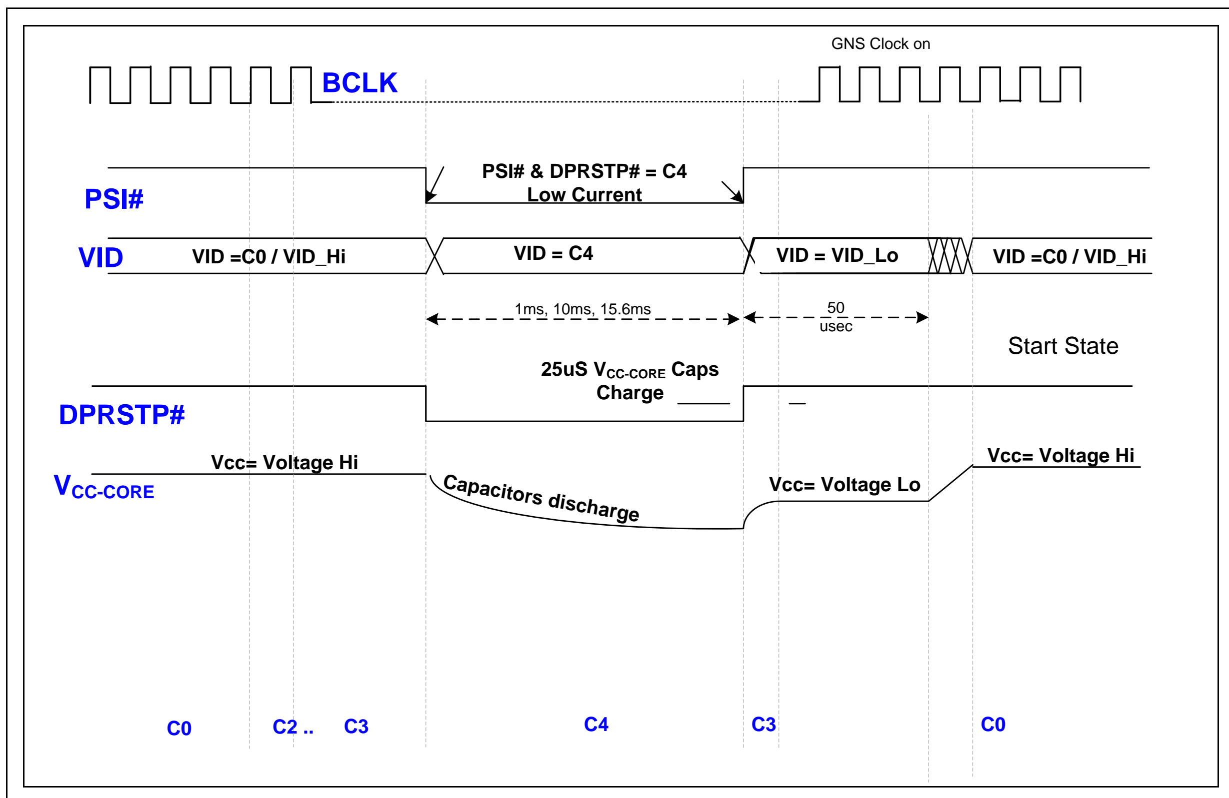


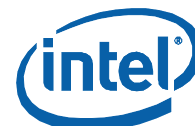
Table 3-10. Impedance Measurement Parameters

Parameter	Value	Notes:
Z_{LL}	1 mΩ	LGA775 Desktop LL target
$Z_{LL\ max}$	1.2 mΩ	Based on VR11 PWM tolerance band
$Z_{LL\ min}$	0.8 mΩ	Based on VR11 PWM tolerance band
F_{break}	2.0 MHz	-

3.3 PSI# Operation

PSI# from an LGA775 platform with a Intel® Core™2 Duo processor or Intel® Core™2 Quad processor will be asserted when the processor enters the C4 state. Additionally, a large step DVID jump as much as 250 mV will occur at the same time. The VR will recover from this event within the timeframe specified for large DVID jumps, which is within 10 us per 100 mV. The timing diagram below shows a 250 mV step.





3.4 V_{TT} Requirements (REQUIRED)

The V_{TT} regulator provides power to the processor VID circuitry, the chipset - processor front side bus, and miscellaneous buffer signals. This rail voltage must converge to the amplitude defined in Table 3-11 to begin power sequencing. The VR11 PWM controller will sense the amplitude of the V_{TT} rail and initiate power sequencing upon crossing a defined threshold voltage. The V_{TT} regulator controller does not include an enable signal; valid output voltage of Table 3-11 must be ensured by the timing protocol defined in the Start-up Sequence diagram.

3.4.1 Electrical Specifications

A linear regulator is recommended for the V_{TT} supply with adequate decoupling capacitors to ensure the sum of AC bus noise and DC tolerance satisfy limits identified in Table 3-11. The processor and chipset V_{TT} supply must be maintained within these tolerance limits across full operational thermal limits, part-to-part component variation, age degradation, and regulator accuracy. Full bandwidth bus noise amplitude must be ensured across all Vcc/ V_{SS} land pairs defined in Table 3-12.

The V_{TT} supply must be unconditionally stable under all DC and transient conditions across the voltage and current ranges defined in Table 3-11. The V_{TT} supply must also operate in a no-load condition (that is, with no processor installed).

Vtt_SEL is an output from the processor that indicates to the V_{TT} regulator the appropriate output voltage. The Vtt_SEL output is either an open circuit (Vtt_SEL = 1) or directly tied to the processor V_{SS} (Vtt_SEL = 0).

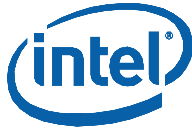
Table 3-11. V_{TT} Specifications

Processor	V_{TT} Min	V_{TT} Typ	V_{TT} Max	Itt Min	Itt Typ	Itt Max
775_VR_CONFIG_04A 775_VR_CONFIG_04B 775_VR_CONFIG_05A 775_VR_CONFIG_05B 775_VR_CONFIG_06 Vtt_SEL = 1	1.140 V	1.200 V[1]	1.260 V	0.15 A	3.4 A	5.25 A[2]
Future LGA775 configurations Vtt_SEL = 0	1.045 V	1.100 V[1]	1.155 V	0.15 A	3.4 A	5.25 A[2]

NOTES:
1. Combined DC and Transient voltage tolerance is 5%, with a maximum 2% DC tolerance.
2. Itt can be up to 7.5 A at power-up. This is applicable when V_{CC} is low and V_{TT} is high.

Table 3-12. V_{TT} Measurement Lands

Device	Supply	Land
Processor	V_{TT}	D25
Processor	V_{SS}	E25



3.5 MB Power Plane Layout (REQUIRED)

The motherboard layer stack-up must be designed to ensure robust, noise-free power delivery to the processor. Failure to minimize and balance power plane resistance may result in non-compliance to the die loadline specification. A poorly planned stack-up or excessive holes in the power planes may increase system inductance and generate oscillation on the V_{CC} voltage rail at the processor. Both of these types of design errors can lead to processor failure and must be avoided by careful V_{CC} and V_{SS} plane layout and stack-up. The types of noise introduced by these errors may not be immediately observed on the processor power lands or during system-board voltage transient validation, so issues must be resolved by design, prior to layout, to avoid unexpected failures.

Following basic layout rules can help avoid excessive power plane noise. All motherboard layers in the area surrounding the processor socket should be used for V_{CC} power delivery; copper shapes that encompass the power delivery region of the processor land field are required. A careful motherboard design will help ensure a well-functioning system that minimizes the noise profile at the processor die. The following subsections provide further guidance.

3.5.1 Minimize Power Path DC Resistance

Power path resistance can be minimized by ensuring that the copper layout area is balanced between V_{CC} and V_{SS} planes. A good four-layer board design will have two V_{CC} layers and two V_{SS} layers. Because there is generally more V_{SS} copper in the motherboard stack-up, care should be taken to maximize the copper in V_{CC} floods. This includes care to minimize unnecessary plane splits and holes when locating through hole components, vias, and connection pads. Refer to Table 3-13 for more details on the reference board layer stackup.

3.5.2 Minimize Power Delivery Inductance

At higher frequencies the ordering of the motherboard layers becomes critical as it is V_{CC}/ V_{SS} **plane pairs** which carry current and determine power plane inductance. The layer stack-up should maximize adjacent (layer-to-layer) planes at a minimized spacing to achieve the smallest possible inductance. Care must be taken to minimize unnecessary plane splits and holes when locating through-hole components, vias, and connection pads. Minimized inductance will ensure that the board does not develop low frequency noise which may cause the processor to fail (loadline violation).

3.5.3 Four-Layer Boards

A well-designed 4-layer board will feature generous V_{CC} shapes on the outer layers and large V_{SS} shapes on the inner layers. The V_{SS} -reference requirements for the front side bus are best accommodated with this layer ordering. The power plane area should be maximized and cut-out areas should be carefully placed to minimize parasitic resistance and inductance. Examples power plane layout of the Intel reference board are provided in Table 3-13 and Figure 3-13 through Figure 3-17.

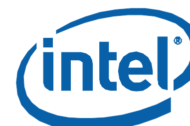
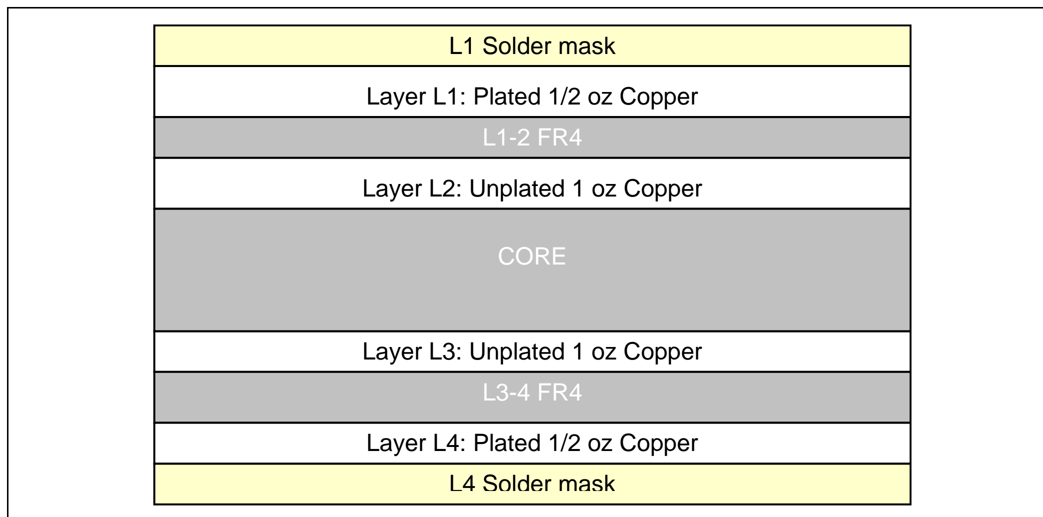


Figure 3-13. Reference Board Layer Stack-up



NOTE: Drawing is not to scale

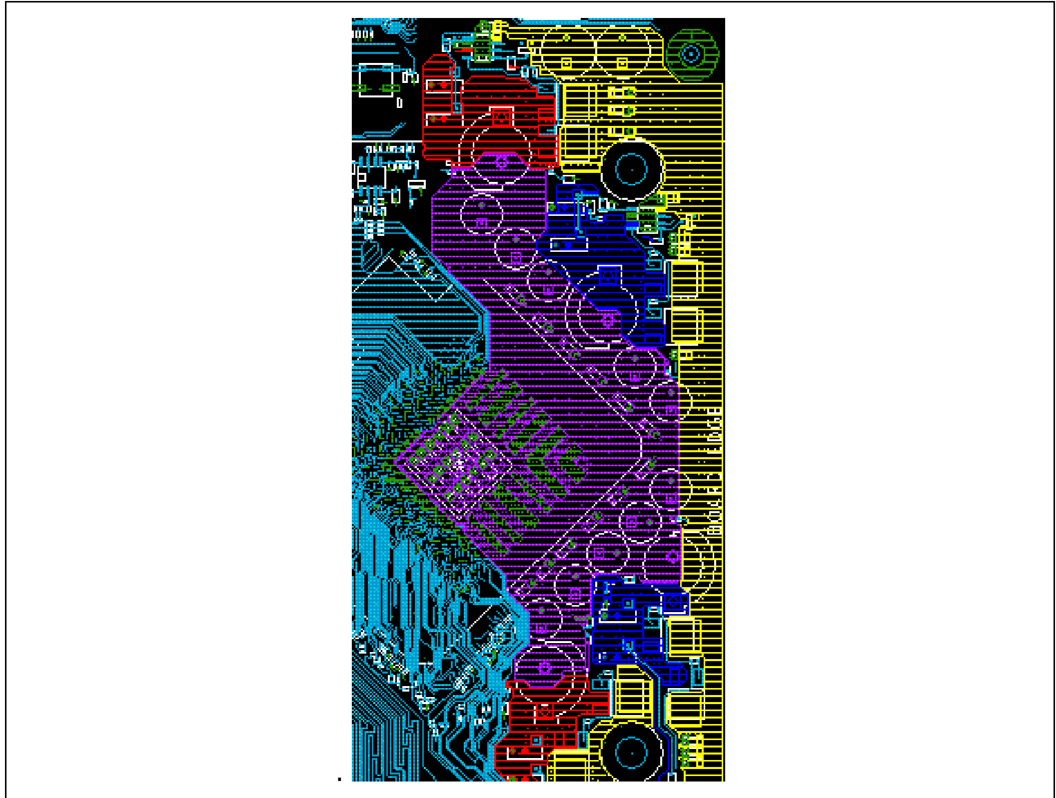
Table 3-13. Reference Board Layer Thickness (Prepreg 1080)

Layer	Minimum	Typical	Maximum
L1 Solder mask	0.2 mils	0.7 mils	1.2 mils
L1	1.1 mils	1.9 mils	2.7 mils
L1-2 FR4	2.0 mils	2.7 mils	3.5 mils
L2	1.0 mils	1.2 mils	1.4 mils
Core	45 mils	50 mils	55 mils
L3	1.0 mils	1.2 mils	1.4 mils
L3-4 FR4	2.0 mils	2.7 mils	3.5 mils
L4	1.1 mils	1.9 mils	2.7 mils
L4 Solder mask	0.2 mils	0.7 mils	1.2mils

NOTES:

1. Consult Figure 2-6 for layer definition
2. Impedance Target: 50 Ω ± 15%; based on nominal 4 mil trace
3. Overall board thickness is 62 mils +8, -5 mils

Figure 3-14. Layer 1 V_{CC} Shape for Intel® Reference Four-layer Motherboard



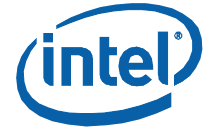


Figure 3-15. Layer 2 V_{SS} Routing for Intel® Reference Four-layer Motherboard

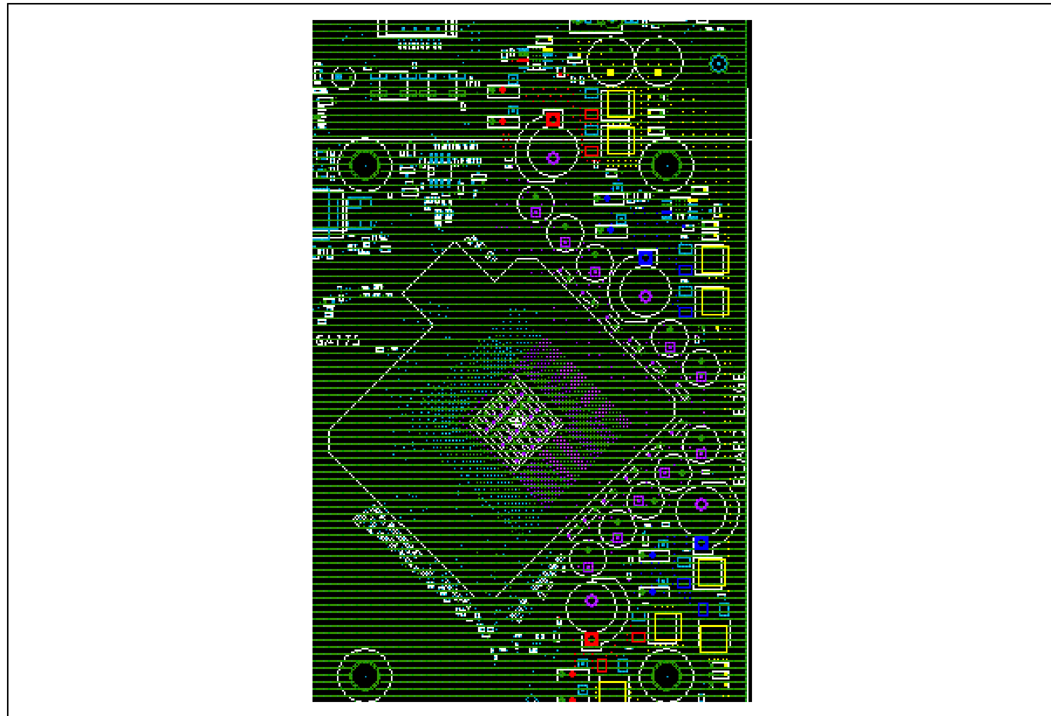


Figure 3-16. Layer 3 V_{SS} Routing for Intel® Reference Four-layer Motherboard

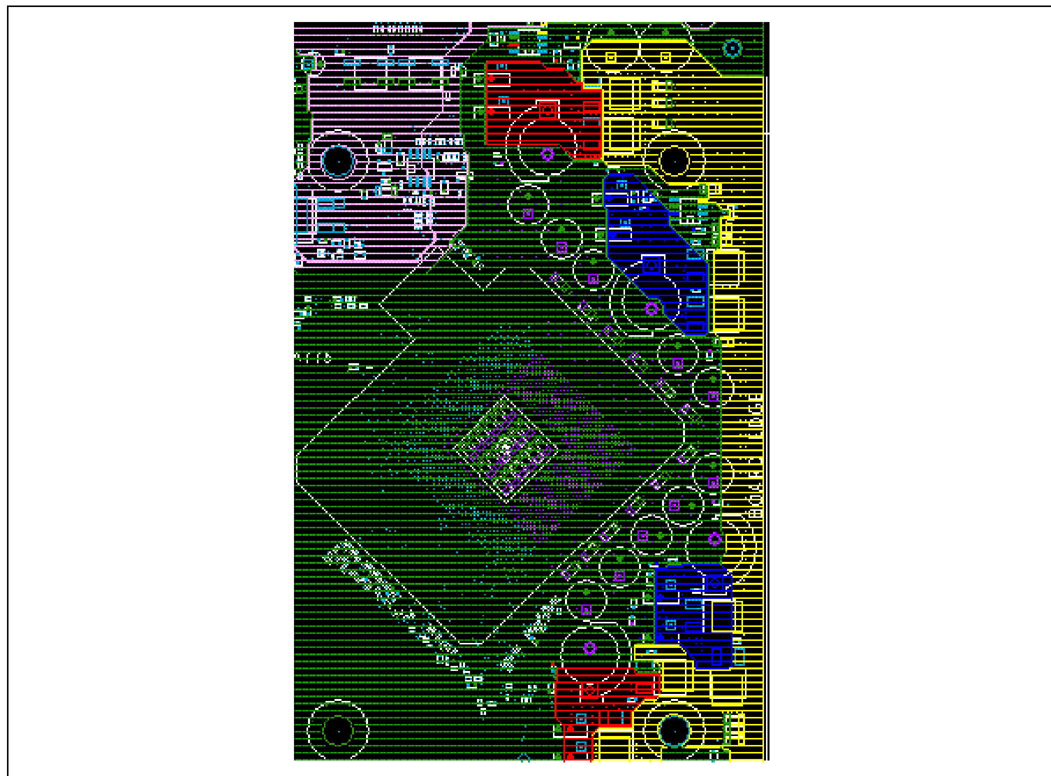
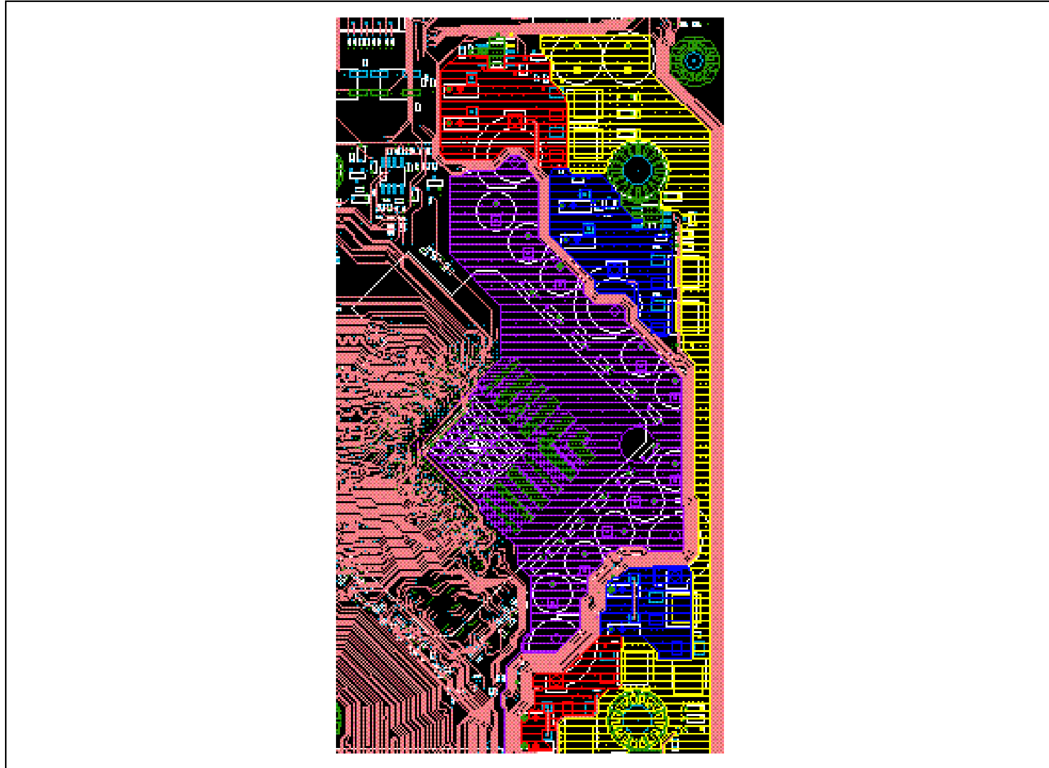


Figure 3-17. Layer 4 V_{CC} Shape for Intel® Reference Four-layer Motherboard

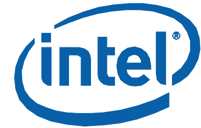


3.5.4 Six-Layer Boards

Six layer boards provide layout engineers with greater design flexibility compared to the four-layer standard. Adjacent plane pairs of the same potential are not useful at higher frequencies, so the best approach is to maximize adjacent, closely spaced V_{CC}/ V_{SS} plane pairs. The plane pair separated by the PCB core material is of lesser importance since it is generally an order of magnitude larger in spacing than other plane pairs in the stack-up. Because the V_{SS} planes are typically full floods of copper, an example of a well-designed 6-layer stack-up will have 4 V_{CC} layers and 2 layers for V_{SS}. The DC resistive requirements (Section 3.5.1) of the power delivery loop can still be met because the V_{SS} floods are larger than the V_{CC} floods, and the higher frequency needs are considered as there are 4 V_{CC}/ V_{SS} plane pairs to deliver current and reduce inductance.

3.5.5 Resonance Suppression

V_{CC} power delivery designs can be susceptible to resonance phenomena capable of creating droop amplitudes in violation of loadline specifications. This is due to the interleaved levels of inductively-separated decoupling capacitance. Furthermore, these resonances may not be detected through standard validation and require engineering analysis to identify and resolve. If not identified and corrected in the design process, these resonant phenomena may yield droop amplitudes in violation of loadline specifications by superimposing with standard VRD droop behavior. Frequency-dependent power delivery network impedance simulations and validation are strongly

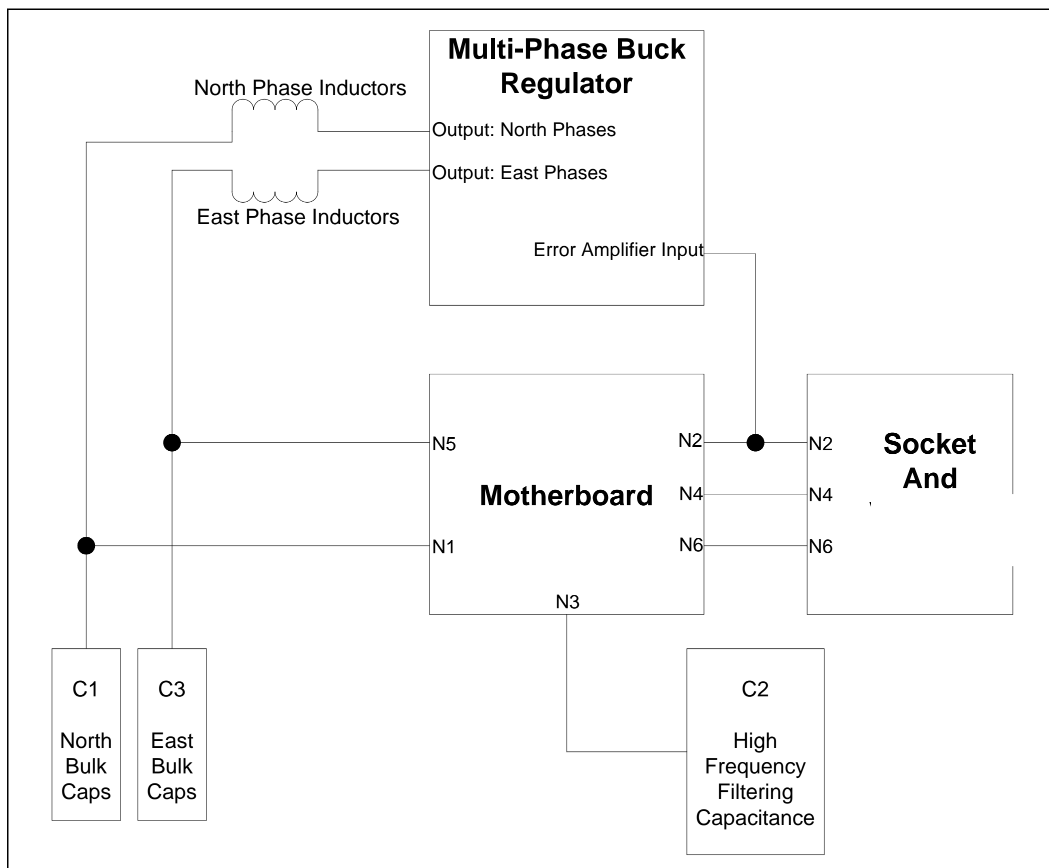


recommended to identify and resolve power delivery resonances before board are actually built. Careful modeling and validation can help to avoid voltage violations responsible for data corruption, system lock-up, or system 'blue-screening'.

3.6 Electrical Simulation (EXPECTED)

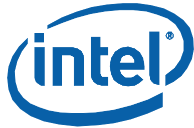
The following electrical models are enclosed to assist with VRD design analysis and component evaluation for loadline compliance. The block diagram shown in Figure 3-18 is a simplified representation of the V_{CC} power delivery network of the Intel four-layer reference board). The board model, detailed in Figure 3-21, characterizes the power plane layout of Figure 3-14 to Figure 3-17. The multiphase buck regulator and capacitor models should be obtained from each selected vendor. When fully integrated into electrical simulation software, this model can be used to evaluate PWM controller, capacitor, and inductor performance against the loadline and tolerance band requirements detailed in Section 3.2.1. To obtain accurate results, it is strongly recommended to create and use a custom model that represents the specific board design, PWM controller, and passive components that are under evaluation.

Figure 3-18. Simplified Reference Block Diagram



NOTE: Consult Figure 3-14 to Figure 3-17 for reference layout.

The motherboard model of Figure 3-21 represents the power delivery path of Intel's reference four-layer motherboard design. Input and output node locations are



identified in Figure 3-22. Feedback to the PWM controller error amplifier should be tied to node 'N2', the socket-motherboard interface. Node 'N1' is the location where the 'north' phase inductors of the buck regulator ties to the 'north' motherboard power plane. If the design incorporates more than one 'north' phase, the inductors of each should be tied to this node. 'North' bulk capacitors, C1, are also connected to node 'N1'. C1 represents the parallel combination of all capacitors and capacitor parasitics at this location. Node 'N5' is the location where the output inductors of the 'east' side phases tie to the 'east' motherboard power plane. If the design incorporates more than one 'east' phase, the inductors of each should be tied to this node. 'East' bulk capacitors, C3, are also connected to 'N5'. C3 represents the parallel combination of all capacitors and capacitor parasitics at this location. Node 'N3' represents the socket cavity and is connected to the mid-frequency filter, C2. C2 represents the parallel combination of all capacitors and capacitor parasitics at this location.

Typical capacitor models are identified in Figure 3-23. Each model represents the parallel combination of the local capacitor placement as identified in the previous paragraph. Recommended parallel values of each parameter are identified in Table 3-15.

The LGA775 socket is characterized by three impedance paths that connect to the motherboard at 'N2' ('north' connection), 'N4' ('south' cavity connection), and 'N6' ('east' connection). I_PWL is a piece-wise linear current step that is used to stimulate the voltage droop as seen at the motherboard-socket interface and is defined in Figure 2-21 and Table 2-16. This load step approximates the low frequency current spectrum that is necessary to evaluate bulk capacitor, mid-frequency capacitor and PWM controller performance. It does not provide high frequency content to excite package noise. The cavity capacitor solution, C2, is used as a reference for designing processor packaging material and should not be modified except to reduce ESR/ESL or increase total capacitance. Failure to observe this recommendation may make the motherboard incompatible with some processor designs.

The primary purpose of the simulation model is to identify options in supporting the socket loadline specification. Evaluation of the full power-path model will allow the designer to perform what-if analysis to determine the cost optimal capacitor and PWM controller configuration. This is especially useful in determining the capacitor configuration that can support loadline specifications across variation such as manufacturing tolerance, age degradation, and thermal drift. The designer is encouraged to evaluate different capacitor configurations and PWM controller designs. However, the designer should be aware that the feedback compensation network of most PWM controllers requires modification when the capacitor solution changes. Consult the PWM controller datasheet for further information.

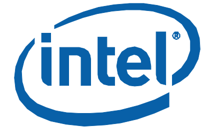


Figure 3-19. Example Voltage Droop Observed At Node 'N2'

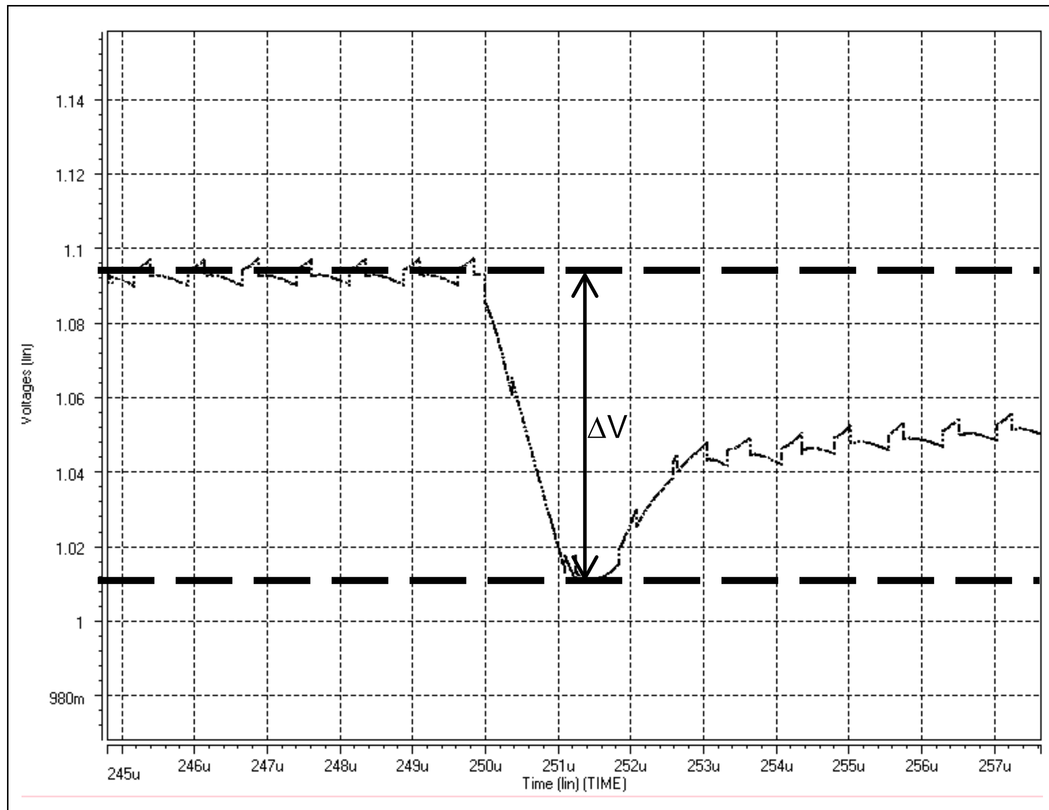
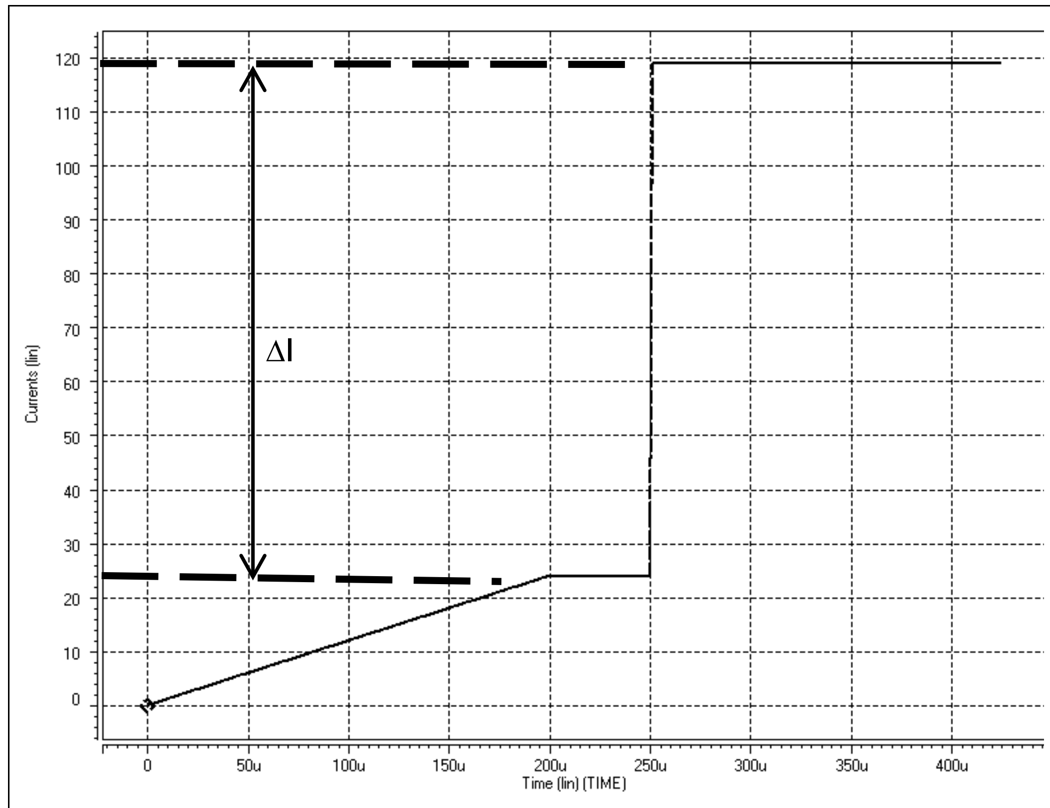


Figure 2-14 provides an example voltage droop waveform at node 'N2', the socket-motherboard interface. The loadline value is defined as $\Delta V/\Delta I$ with ΔV measured at this node and the current step observed through I_PWL. The voltage amplitude is defined as the difference in the steady state voltage (prior to the transient) and the minimum voltage droop (consult Figure 2-14). Care must be taken to remove all ripple content in this measurement to avoid a pessimistic loadline calculation that will require additional capacitors (cost) to correct. Figure 2-15 provides an example current stimulus. The amplitude is measured as the difference in maximum current and steady state current prior to initiation of the current step. With ΔV and ΔI known, the loadline slope is simply calculated using Ohm's Law: $R_{LL} = \Delta V/\Delta I$.

Figure 3-20. Current Step Observed Through I_PWL



NOTE: To avoid excessive ringing in simulation, the system current should be slowly ramped from zero amps to the minimum recommended DC value prior to initiating the current step.

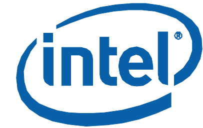
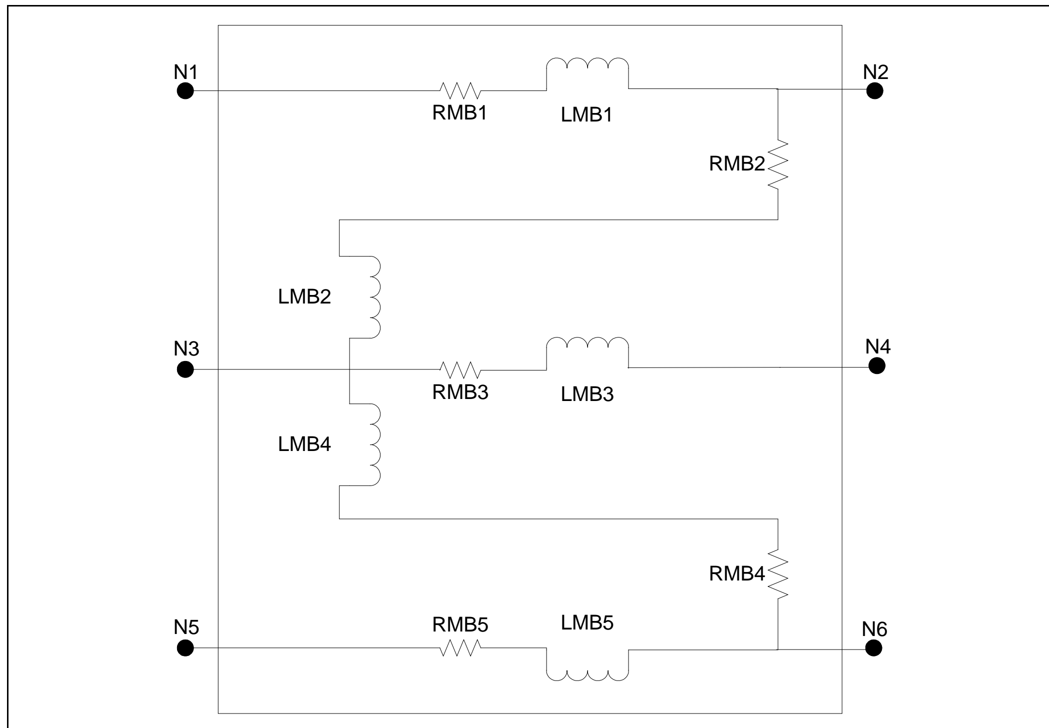


Figure 3-21. Schematic Diagram for the Four-layer Intel® Reference Motherboard

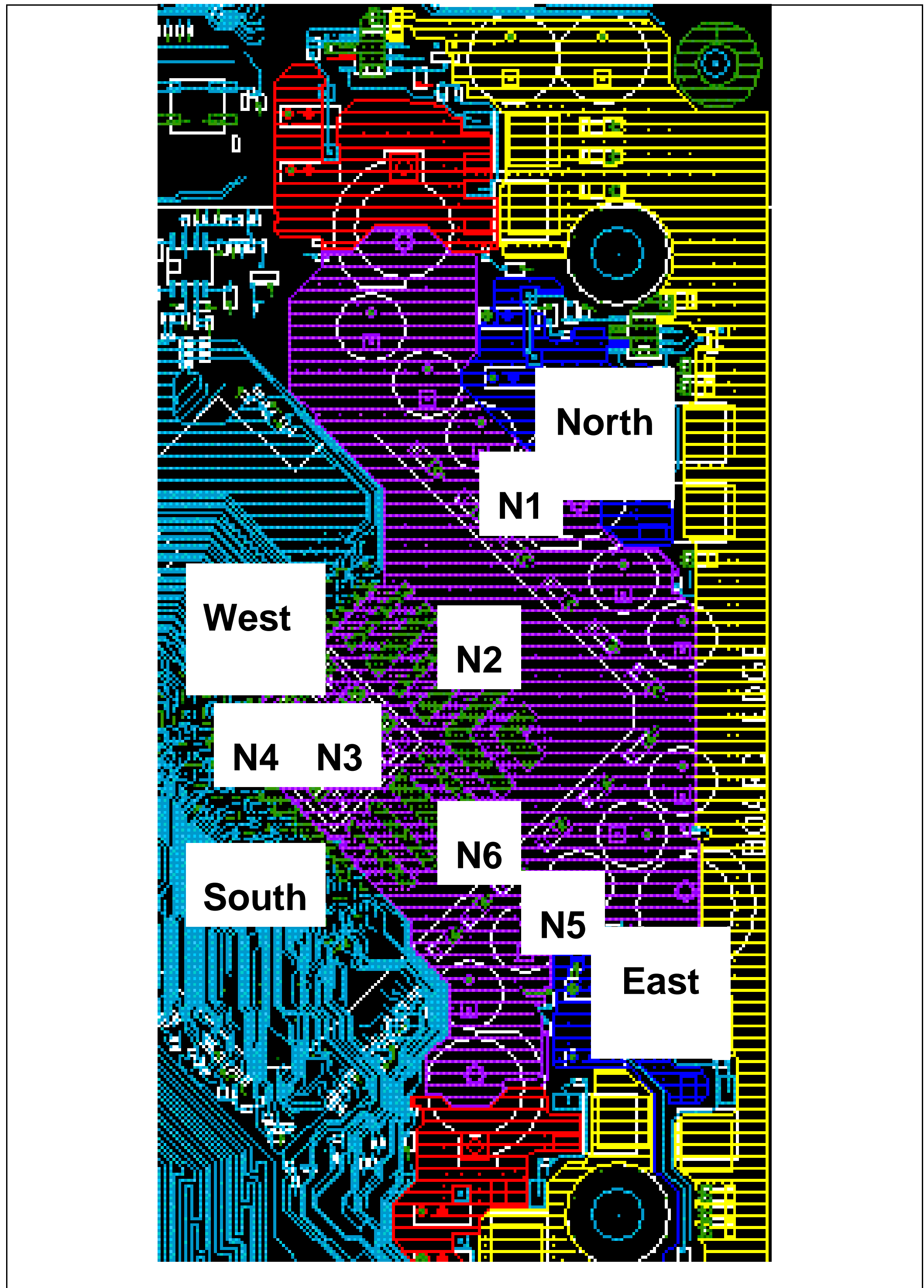


NOTE: Consult Figure 3-14 to Figure 3-17 for reference layout.

Table 3-14. Parameter Values for the Schematic of Figure 3-21

Parameter	Value	Comments
RMB1	0.64 mΩ	'North' power plane parasitic resistance from the buck regulator output inductor to the LGA775 socket connection.
RMB2	0.56 mΩ	Power plane parasitic resistance from 'north' LGA775 motherboard connection to the center of the LGA775 cavity.
RMB3	0.59 mΩ	Power plane parasitic resistance from the center of the LGA775 cavity to the 'south' LGA775 socket connection.
RMB4	0.59 mΩ	Power plane parasitic resistance from the center of the LGA775 cavity to the 'east' LGA775 socket connection.
RMB5	0.58 mΩ	'East' power plane parasitic resistance from the buck regulator output inductor to the LGA775 connection.
LMB1	120 pH	'North' power plane parasitic inductance from the buck regulator output inductor to the LGA775 socket connection
LMB2	166 pH	Power plane parasitic inductance from 'north' LGA775 motherboard connection to the center of the LGA775 cavity.
LMB3	166 pH	Power plane parasitic inductance from the center of the LGA775 cavity to the 'south' LGA775 socket connection.
LMB4	247 pH	Power plane parasitic inductance from 'east' LGA775 motherboard connection to the center of the LGA775 cavity.
LMB5	138 pH	'East' power plane parasitic inductance from the buck regulator output inductor to the LGA775 connection.

Figure 3-22. Node Location for the Schematic of Figure 3-21



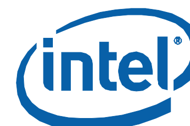
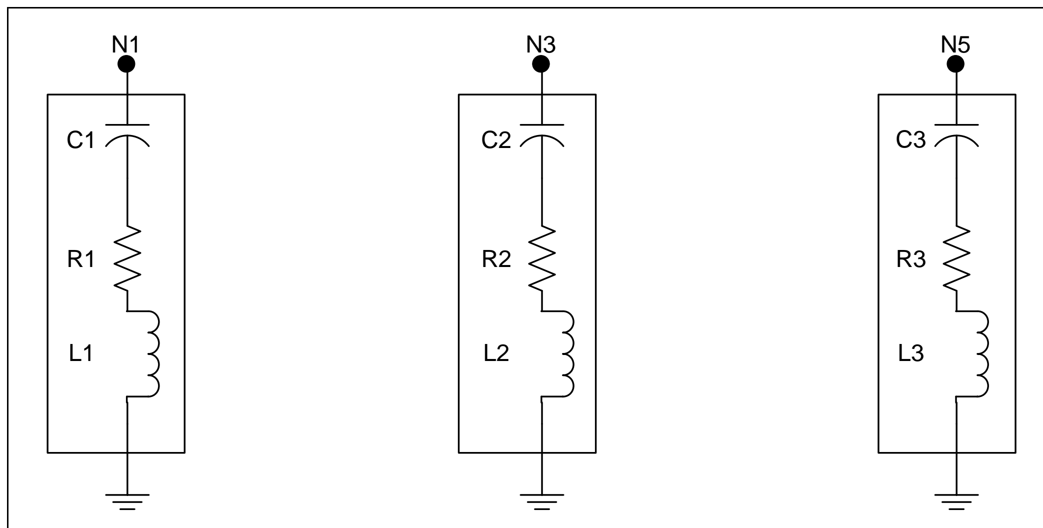


Figure 3-23. Schematic Representation of Decoupling Capacitors



NOTES:

1. C1 represents the parallel model for 'north' location bulk decoupling.
2. C2 represents the parallel model for mid-frequency decoupling located in the socket cavity.
3. C3 represents the parallel model for 'east' location bulk decoupling.

Table 3-15. Recommended Parameter Values for the Capacitors Models in Figure 3-23

Parameter	Value	Comments
C1	2800 μF[2]	Parallel equivalent for 'north' capacitors prior to age, thermal, and manufacturing degradation.
R1	1.2 mΩ	Parallel equivalent for 'north' capacitor maximum ESR.
L1	600 pH[1, 2]	Parallel equivalent for 'north' capacitor maximum ESL.
C2	328 μF[2]	Parallel equivalent for 'cavity' capacitors prior to age, thermal, and manufacturing degradation.
R2	16.7 μΩ[2]	Parallel equivalent for 'cavity' capacitor maximum ESR.
L2	29 pH[1, 2]	Parallel equivalent for 'cavity' capacitor maximum ESL.
C3	2800 μF[2]	Parallel equivalent for 'east' capacitors prior to DC bias, age, thermal, and manufacturing degradation.
R3	1.2 mΩ[2]	Parallel equivalent for 'east' capacitor maximum ESR.
L3	600 pH[1, 2]	Parallel equivalent for 'east' capacitor maximum ESL.

NOTES:

1. Higher values of ESL may satisfy design requirements.
2. Contact capacitor vendors to identify values for the specific components used in your design

Figure 3-24. Schematic Representation of Decoupling Capacitors

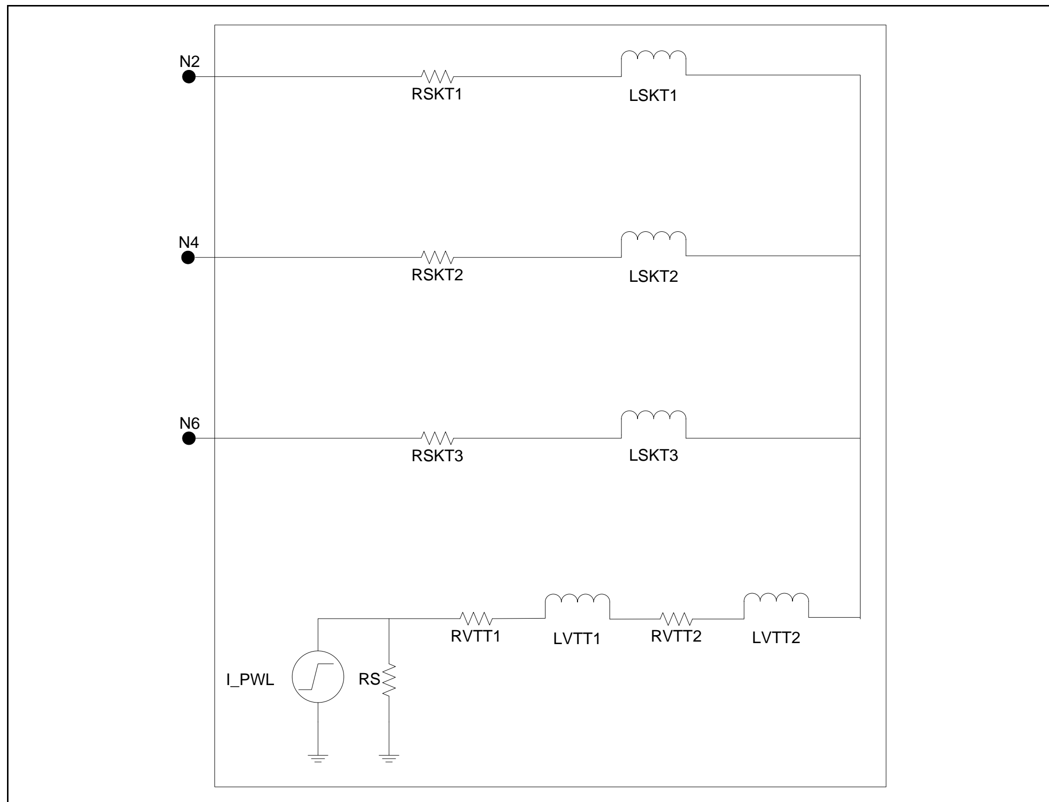


Table 3-16 Recommended Parameter Values for the Capacitor Models in Figure 3-23

Parameter	Value	Comments
RSKT1	0.38 mΩ	LGA775 ‘north’ segment resistance
RSKT2	1.13 mΩ	LGA775 ‘center’ segment resistance
RSKT3	0.29 mΩ	LGA775 ‘east’ segment resistance
RVTT1	0.42 mΩ	Resistance of VTT Tool load board
RVTT2	0.91 mΩ	Resistance of VTT Tool socket adapter (interposer)
RS	100 kΩ	VTT Tool current source resistance
LSKT1	40 pH	LGA775 ‘north’ segment inductance
LSKT2	120pH	LGA775 ‘center’ segment inductance
LSKT3	30 pH	LGA775 ‘east’ segment inductance
LVTT1	240 pH	Inductance of VTT Tool load board
LVTT2	42 pH	Inductance of VTT Tool socket adapter (interposer)

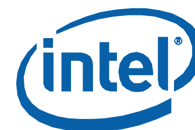


Figure 3-25. Current Load Step Profile for I_PWL

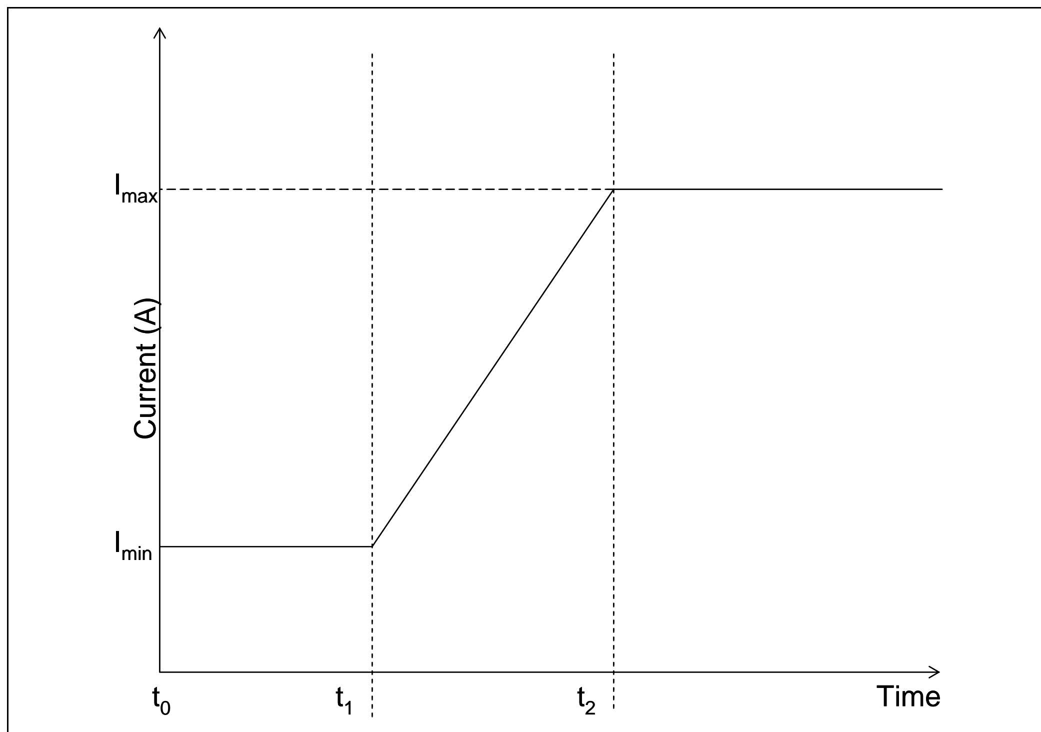
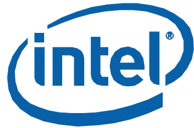


Table 3-17. I_PWL Current Parameters for Figure 3-25

Parameter	Value	Comments
t_0	0 s	Simulation 'time zero'
t_1	250 μs	Time to initiate the current step. This parameter must be chosen at a time that the V_{CC} rail is residing at steady state.
t_2	t_1 + 50 ns	Time of maximum current[1]
Istep	95 A	Current step for loadline testing[1]
Imin	30 A	Minimum current for simulation analysis[1]
Imax	125 A	Maximum current for simulation analysis[1]

NOTE:

1. See Table 3-9. Intel® Processor Current Step Values for Transient Socket loadline Testing



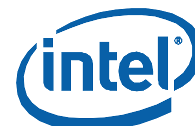
3.7 LGA775 Voltage Regulator Configuration Parameters

This section provides the parameter for loadline testing used to characterize the performance of the voltage regulator for the main board supporting LGA775 processor.

3.7.1 775_VR_CONFIG_04A

Table 3-18. 775_VR_CONFIG_04A Specification Input Parameters

Definition	Variable Name	Value
Socket Loadline Slope	SKT_LL	1.40 mΩ
Socket Loadline Tolerance Band	TOB	25 mV
Maximum Overshoot Above VID	OS_AMP	50 mV
Maximum Overshoot Time Duration Above VID	OS_TIME	25 us
Peak To Peak Ripple Amplitude	RIPPLE	10 mV
Thermal Compensation Voltage Drift	THERMAL_DRIFT	4 mV
Iccmax	Iccmax	78 A
Dynamic Current Step	I_STEP	55 A
Maximum DC Test Current	I_DC_MAX	23 A
Minimum DC Test Current	I_DC_MIN	5 A
Voltage Regulator Thermal Design Current	VR_TDC	68 A
Current step rise time	I_RISE	83 A/μs



3.7.2 775_VR_CONFIG_04B

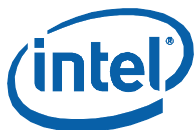
Table 3-19. 775_VR_CONFIG_04B Specification Input Parameters

Definition	Variable Name	Value
Socket Loadline Slope	SKT_LL	1.00 mΩ
Socket Loadline Tolerance Band	TOB	19 mV
Maximum Overshoot Above VID	OS_AMP	50 mV
Maximum Overshoot Time Duration Above VID	OS_TIME	25 us
Peak To Peak Ripple Amplitude	RIPPLE	10 mV
Thermal Compensation Voltage Drift	THERMAL_DRIFT	4 mV
Iccmax	Iccmax	119 A
Dynamic Current Step	I_STEP	95 A
Maximum DC Test Current	I_DC_MAX	24 A
Minimum DC Test Current	I_DC_MIN	5 A
Voltage Regulator Thermal Design Current	VR_TDC	101 A
Current step rise time	I_RISE	83 A/μs

3.7.3 775_VR_CONFIG_05A

Table 3-20. 775_VR_CONFIG_05A Specification Input Parameters

Definition	Variable Name	Value
Socket Loadline Slope	SKT_LL	1.0 mΩ
Socket Loadline Tolerance Band	TOB	19 mV
Maximum Overshoot Above VID	OS_AMP	50 mV
Maximum Overshoot Time Duration Above VID	OS_TIME	25 us
Peak To Peak Ripple Amplitude	RIPPLE	10 mV
Thermal Compensation Voltage Drift	THERMAL_DRIFT	4 mV
Iccmax	Iccmax	100 A
Dynamic Current Step	I_STEP	65 A
Maximum DC Test Current	I_DC_MAX	35 A
Minimum DC Test Current	I_DC_MIN	5 A
Voltage Regulator Thermal Design Current	VR_TDC	85 A
Current step rise time	I_RISE	50 ns



3.7.4 775_VR_CONFIG_05B

Table 3-21. 775_VR_CONFIG_05B Specification Input Parameters

Definition	Variable Name	Value
Socket Loadline Slope	SKT_LL	1.00 mΩ
Socket Loadline Tolerance Band	TOB	19 mV
Maximum Overshoot Above VID	OS_AMP	50 mV
Maximum Overshoot Time Duration Above VID	OS_TIME	25 us
Peak To Peak Ripple Amplitude	RIPPLE	10 mV
Thermal Compensation Voltage Drift	THERMAL_DRIFT	4 mV
Iccmax	Iccmax	125 A
Dynamic Current Step	I_STEP	95 A
Maximum DC Test Current	I_DC_MAX	30 A
Minimum DC Test Current	I_DC_MIN	5 A
Voltage Regulator Thermal Design Current	VR_TDC	115 A
Current step rise time	I_RISE	50 ns

3.7.5 775_VR_CONFIG_06

Table 3-22. 775_VR_CONFIG_06 Specification Input Parameters

Definition	Variable Name	Value
Socket Loadline Slope	SKT_LL	1.00 mΩ
Socket Loadline Tolerance Band	TOB	19 mV
Maximum Overshoot Above VID	OS_AMP	50 mV
Maximum Overshoot Time Duration Above VID	OS_TIME	25 us
Peak To Peak Ripple Amplitude	RIPPLE	10 mV
Thermal Compensation Voltage Drift	THERMAL_DRIFT	4 mV
Iccmax	Iccmax	75 A
Dynamic Current Step	I_STEP	50 A
Maximum DC Test Current	I_DC_MAX	25 A
Minimum DC Test Current	I_DC_MIN	5 A
Voltage Regulator Thermal Design Current	VR_TDC	60 A
Current step rise time	I_RISE	50 ns

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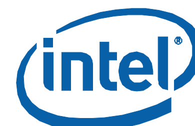


4 LGA1156 Information

4.1 Introduction

This chapter focuses on information unique to platforms designed with the LGA1156.

4.1.1 Applications

LGA1156 designs will use the V_{CC} and V_{SS} sense points to determine the loadline. The loadline at these points will be 1.4 mOhm.

4.2 Processor V_{CC} Requirements

4.2.1 Loadline Definitions (REQUIRED)

To maintain processor reliability and performance, platform DC voltage regulation and transient-droop noise levels must always be contained within the Vccmin and Vccmax loadline boundaries (known as the loadline window). Loadline compliance must be ensured across component manufacturing tolerances, thermal variation, and age degradation. Loadline boundaries are defined by the following equations in conjunction with the V_{CC} regulator design parameter values defined in Table 4-2. In these equations, VID, R_{LL}, and TOB are known. Plotting V_{CC} while varying I_{CC} from 0 A to Iccmax establishes the Vccmax and Vccmin loadlines. Vccmax establishes the maximum DC loadline boundary. Vccmin establishes the minimum AC and DC voltage boundary. Short transient bursts above the Vccmax loadline are permitted; this condition is defined in Section 1.3.7.

Table 4-1. Loadline Equations

Loadline	Equation
Equation 11: Vccmax Loadline	V_{CC} = VID – (R_{LL}* I_{CC})
Equation 12: Vcctyp Loadline	V_{CC} = VID – TOB - (R_{LL}* I_{CC})
Equation 13: Vccmin loadline	V_{CC} = VID – 2*TOB - (R_{LL}* I_{CC})

Loadline recommendations are established to provide guidance for satisfying processor loadline specifications, which are defined in processor datasheets. Loadline requirements must be satisfied at all times and may require adjustment in the loadline value. The processor loadlines are defined in the applicable processor datasheet.

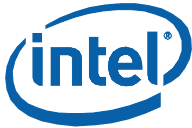


Table 4-2. V_{CC} Regulator Design Parameters

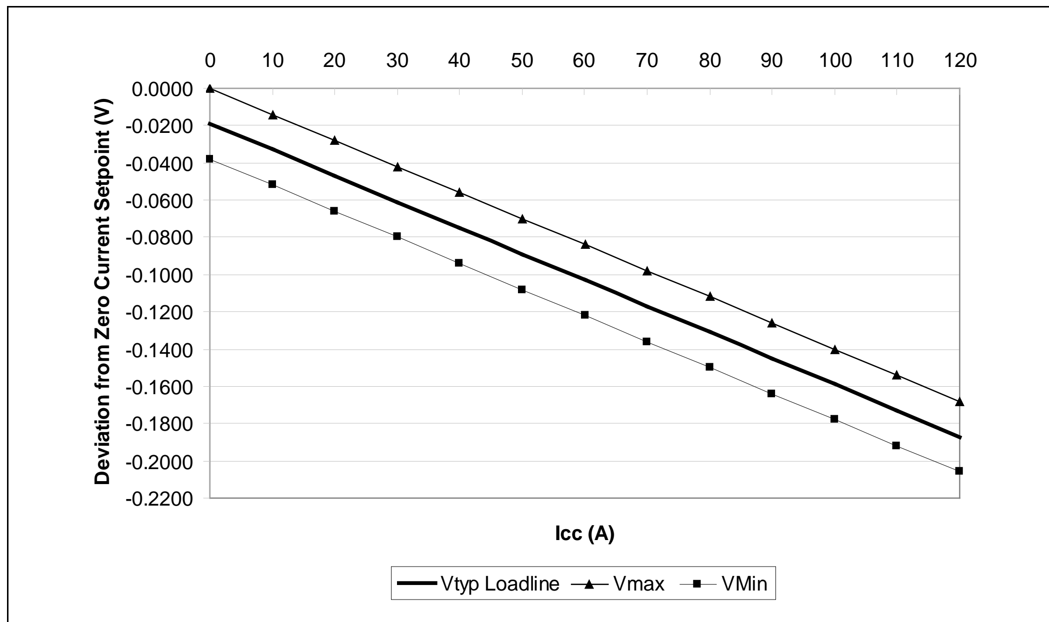
VR Configuration	Iccmax	VR TDC	Dynamic I_{CC}	RLL	TOB	Maximum VID
1156_VR_CONF_09A	75 A	60 A	50 A	1.4 mΩ	± 19 mV	TBD V
1156_VR_CONF_09B	110A	90 A	75 A	1.4 mΩ	± 19 mV	TBD V

Table 4-2 provides a list of VRD11.1 LGA1156 voltage regulator design configurations. The configurations to be adopted by VRD hardware will depend on the specific processors the design is intended to support. It is common for a motherboard to support processors that require different VR configurations. In this case, the V_{CC} regulator design must meet the specifications of all processors supported by that board.

The following tables and figures show minimum and maximum voltage boundaries for each loadline design configuration defined in Table 4-2. V_{CCTYP} loadlines are provided for design reference; designs should calibrate the loadline to this case (centered in the loadline window, at the mean of the tolerance band). Different processors discussed in this design guide can be shipped with different VID values. The reader should not assume that processors with similar characteristics will have the same VID value. A single loadline chart and figure for each VRD design configuration can represent functionality for each possible VID value. Tables and figures presented as voltage deviation from VID provide the necessary information to identify voltage requirements at any reference VID. This avoids the redundancy of publishing tables and figures for each of the multiple cases.

4.2.1.1 Loadline Definition for 1156_VR_CONFIG_09B

Figure 4-1. Loadline Window for 1156_VR_CONFIG_09B



NOTES:
1. Presented as a deviation from VID
2. Loadline Slope = 1.4 mΩ, TOB = ±19 mV
3. Consult Table 4-2 for VR configuration parameter details

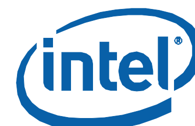


Table 4-3. Loadline Window for 1156_VR_CONFIG_09B

I_{CC}	Maximum (V)	Typical (V)	Minimum (V)
0 A	0.0000	-0.0190	-0.0380
10 A	-0.0140	-0.0330	-0.0520
20 A	-0.0280	-0.0470	-0.0660
30 A	-0.0420	-0.0610	-0.0800
40 A	-0.0560	-0.0750	-0.0940
50 A	-0.0700	-0.0890	-0.1080
60 A	-0.0840	-0.1030	-0.1220
70 A	-0.0980	-0.1170	-0.1360
80 A	-0.1120	-0.1310	-0.1500
90 A	-0.1260	-0.1450	-0.1640
100 A	-0.1400	-0.1590	-0.1780
110 A	-0.1540	-0.1730	-0.1920
120 A	-0.1680	-0.1870	-0.2060

NOTES:
1. Presented as a deviation from VID
2. Loadline Slope = 1.4 mΩ, TOB = ±19 mV
3. Consult Table 4-2 for VR configuration parameter details

VRD layout studies indicate that the phases are best located north of the processor with the controller to the northeast.

Table 4-4. Loadline Reference Lands for the LGA1156 Socket

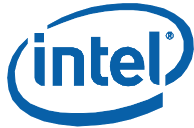
Name	Land
VCC_SENSE	T35
VSS_SENSE	T34

To properly calibrate the loadline parameter, the VR designer must excite the processor socket with a current step that generates a voltage droop, which must be checked against the loadline window requirements. Table 4-5 identifies the steady state and transient current values to use for this calibration.

Table 4-5. Intel® Processor Current Step Values for Transient Loadline Testing

VR Configuration	Starting Current	Ending Current	Dynamic Current Step	I_{CC} Rise Time	I_{CC} Fall Time
1156_VR_CONF_09A	25 A	75 A	50 A	100 ns[1]	100 ns[1]
1156_VR_CONF_09B	45 A	110A	75 A	100 ns[1]	100 ns[1]

NOTES:
1. I_{CC} Rise and Fall times are subject to change pending validation



4.2.1.2 Time Domain Validation

To ensure processor reliability and performance, platform transient-droop and overshoot noise levels must always be contained within the Vccmin and Vccmax loadline boundaries (known as the loadline window). The load generates a voltage droop, or overshoot, which must be checked against the loadline window requirements. The current step must have a fast enough slew rate to excite the impedance across the frequency range of the VR. In addition, the VR needs to be tested at different load frequencies and load steps to prevent any non-linear, resonant, or beating effects that could cause functional issues or loadline violations. Intel recommends sweeping the load frequency from DC to 1 MHz, using two different load steps.

Intel recommends testing using different VID levels for each of the supported VR configurations. In particular the highest and lowest VIDs should be checked. The VID ranges for each processor is available in the processor datasheet.

4.2.1.3 Platform Impedance Measurement and Analysis (Expected)

In addition to the tuning of the loadline with Vdroop testing and DC loadline testing, the decoupling capacitor selection needs to be analyzed to make sure the impedance of the decoupling is below the loadline target up to the frequency F_{break} as defined in Figure 4-2. This analysis can be done with impedance testing or through power delivery simulation if the designer can extract the parasitic resistance and inductance of the power planes on the motherboard and they have good models for the decoupling capacitors.

Measured power delivery impedance should be with in the tolerance band shown in Figure 4-2. For Loadline compliance, time domain validation is required and the VR tolerance band must be met at all times. Above 500 kHz, the minimum impedance tolerance is not defined and is determined by the MLCC capacitors required to get the ESL low enough to meet the loadline impedance target at the F_{break} frequency. At 1 MHz, the Zmax tolerance drops to the loadline target impedance. Any resonance points that are above the Zmax line need to be carefully evaluated with time domain method defined in Section 4.2.1.2 by applying transient loads at that frequency and looking for Vmin violations. Maintaining the impedance profile up to F_{break} is important to ensure the package level decoupling properly matches the motherboard impedance. After F_{break}, the impedance measurement is permitted to rise at a inductive slope. The motherboard VR designer does not need to design for frequencies over F_{break} as the processor package decoupling takes over in the region above F_{break}.

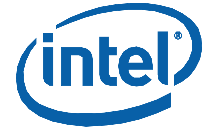
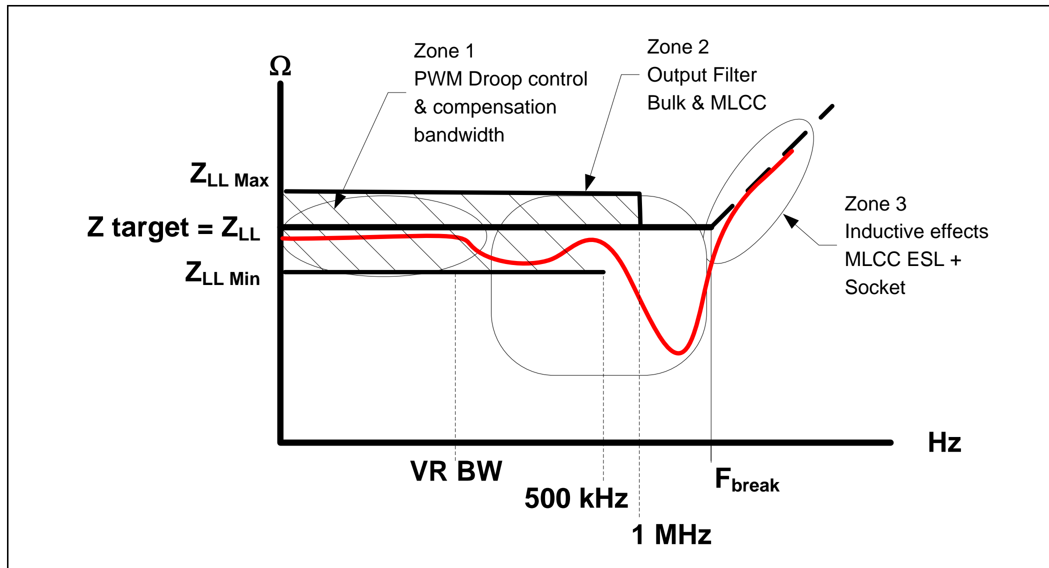


Figure 4-2. Power Distribution Impedance versus Frequency

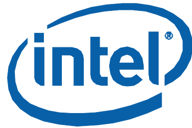


NOTES:

1. See Table 4-6. Impedance Measurement Parameters definitions
2. Zone 1 is defined by the VR closed loop compensation bandwidth (VR BW) of the voltage regulator. Typically 30-40 kHz for a 300 kHz voltage regulator design.
3. Zones 2 and 3 are defined by the output filter capacitors and interconnect parasitic resistance and inductance. The tolerance is relaxed over 500 kHz allowing the VR designer freedom to select output filter capacitors. The goal is to keep Z(f) below Z_{LL} up to Fbreak and as flat as practical, by selection of bulk capacitor values and type and number of MLCC capacitors. The ideal impedance would be between Z_{LL} and Z_{LL} Min but this may not be achieved with standard decoupling capacitors.

Table 4-6. Impedance Measurement Parameters

Parameter	Value	Notes
Z_{LL}	1.4 mΩ	LGA1156 Desktop LL target
$Z_{LL\ max}$	1.6 mΩ	Based on VR11.1 PWM tolerance band
$Z_{LL\ min}$	1.2 mΩ	Based on VR11.1 PWM tolerance band
F_{break}	2.0 MHz	-



4.3 LGA 1156 Specific Signals

4.3.1 Power-on Configuration (POC) Signals on VID (REQUIRED)

All 8 VID lines will serve a second function: the Power On Configuration (POC) logic levels are multiplexed onto the VID lines with 1 kΩ pull-ups and pull-downs and they will be read by the processor during the time — as shown in Section 1.4, Power Sequencing (REQUIRED). The POC configuration programs the processor as to the platform VR capabilities. The VR does not read POC configuration resistors. After OUTEN is asserted the processor VID CMOS drivers override the POC pull-up, and pull-down resistors. See the Power Sequencing section for more information.

The POC bits (multiplexed with 8 VID lines) are allocated is as follows:

- POC/(VID)[2:0] = MSID (Market Segment ID) bits, refer to the datasheet.
- POC/(VID)[5:3] = Current Sense Config bits, Iout gain setting.
- POC/(VID)[6] = RESERVED (pull-down resistors installed, unless stated otherwise in the datasheet).
- POC/(VID)[7] = VR11.1 Select signal, with pull-down resistor installed for VR11.1, refer to the datasheet.

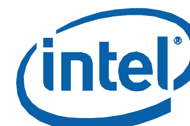
4.4 MB Power Plane Layout (REQUIRED)

The motherboard layer stack-up must be designed to ensure robust, noise-free power delivery to the processor. Failure to minimize and balance power plane resistance may result in non-compliance to the die loadline specification. A poorly planned stack-up or excessive holes in the power planes may increase system inductance and generate oscillation on the V_{CC} voltage rail at the processor. Both of these types of design errors can lead to processor failure and must be avoided by careful V_{CC} and V_{SS} plane layout and stack-up. The types of noise introduced by these errors may not be immediately observed on the processor power lands or during system-board voltage transient validation, so issues must be resolved by design, prior to layout, to avoid unexpected failures.

Following basic layout rules can help avoid excessive power plane noise. Copper shapes that encompass the power delivery region of the processor land field are required. A careful motherboard design will help ensure a well-functioning system that minimizes the noise profile at the processor die. The following subsections provide further guidance.

4.4.1 Minimize Power Path DC Resistance

Power path resistance can be minimized by ensuring that the copper layout area is balanced between V_{CC} and V_{SS} planes. A good four-layer board design will have two V_{CC} layers and two V_{SS} layers. Because there is generally more V_{SS} copper in the motherboard stack-up, care should be taken to maximize the copper in V_{CC} floods. This includes care to minimize unnecessary plane splits and holes when locating through hole components, vias, and connection pads. Refer to Table 4-7 for more details on the reference board layer stack up.



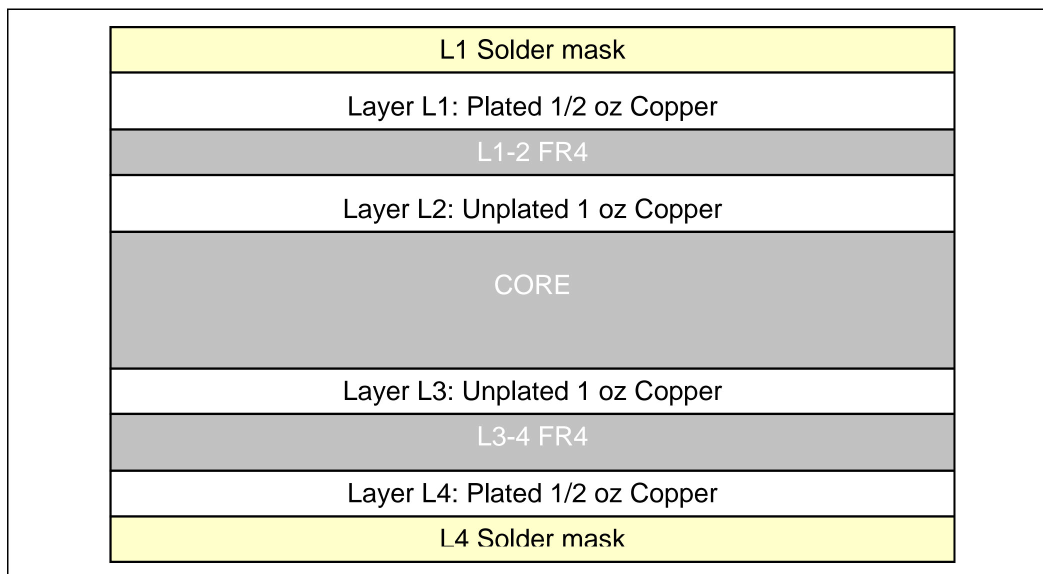
4.4.2 Minimize Power Delivery Inductance

At higher frequencies the ordering of the motherboard layers becomes critical as it is V_{CC}/ V_{SS} **plane pairs**, which carry current and determine power plane inductance. The layer stack-up should maximize adjacent (layer-to-layer) planes at a minimized spacing to achieve the smallest possible inductance. Care must be taken to minimize unnecessary plane splits and holes when locating through-hole components, vias, and connection pads. Minimized inductance will ensure that the board does not develop low frequency noise which may cause the processor to fail (loadline violation).

4.4.3 Four-Layer Boards

A well-designed four-layer board will feature generous V_{CC} shapes on the outer layers and large V_{SS} shapes on the inner layers. The V_{SS} -reference requirements for the front side bus are best accommodated with this layer ordering. The power plane area should be maximized and cut-out areas should be carefully placed to minimize parasitic resistance and inductance. Examples power plane layout of the Intel reference board are provided in Table 4-7 and Figure 4-3 through Figure 4-7.

Figure 4-3. Reference Board Layer Stack-up



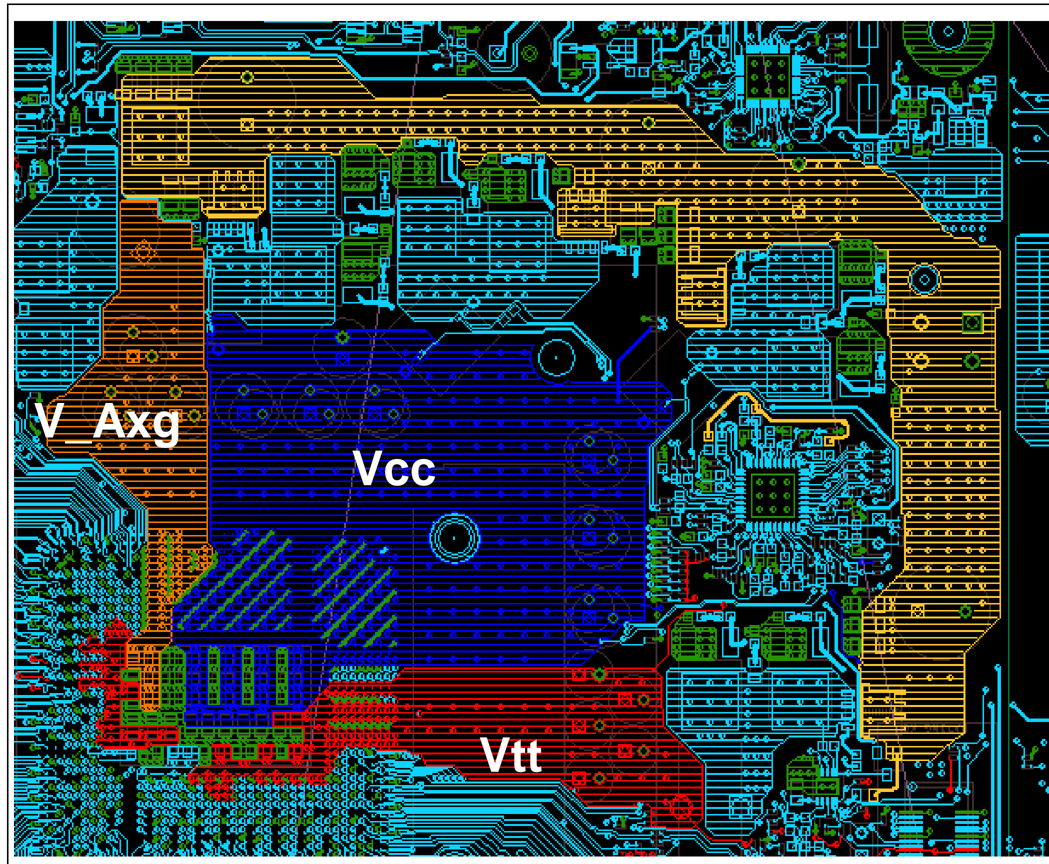
NOTE: Drawing is not to scale

Table 4-7. Reference Board Layer Thickness (Prepreg 1080)

Layer	Minimum	Typical	Maximum
L1 Solder mask	0.2 mils	0.7 mils	1.2 mils
L1	1.1 mils	1.9 mils	2.7 mils
L1-2 FR4	2.0 mils	2.7 mils	3.5 mils
L2	1.0 mils	1.2 mils	1.4 mils
Core	45 mils	50 mils	55 mils
L3	1.0 mils	1.2 mils	1.4 mils
L3-4 FR4	2.0 mils	2.7 mils	3.5 mils
L4	1.1 mils	1.9 mils	2.7 mils
L4 Solder mask	0.2 mils	0.7 mils	1.2 mils

NOTES:
1. Consult Figure 4-3 for layer definition.
2. Impedance Target: 50 Ω ± 15%; based on nominal 4 mil trace.
3. Overall board thickness is 62 mils +8, -5 mils.

Figure 4-4. Layer 1 V_{CC} Shape for Intel® Reference Four-layer Motherboard



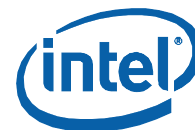


Figure 4-5. Layer 2 V_{SS} Routing for Intel® Reference Four-layer Motherboard

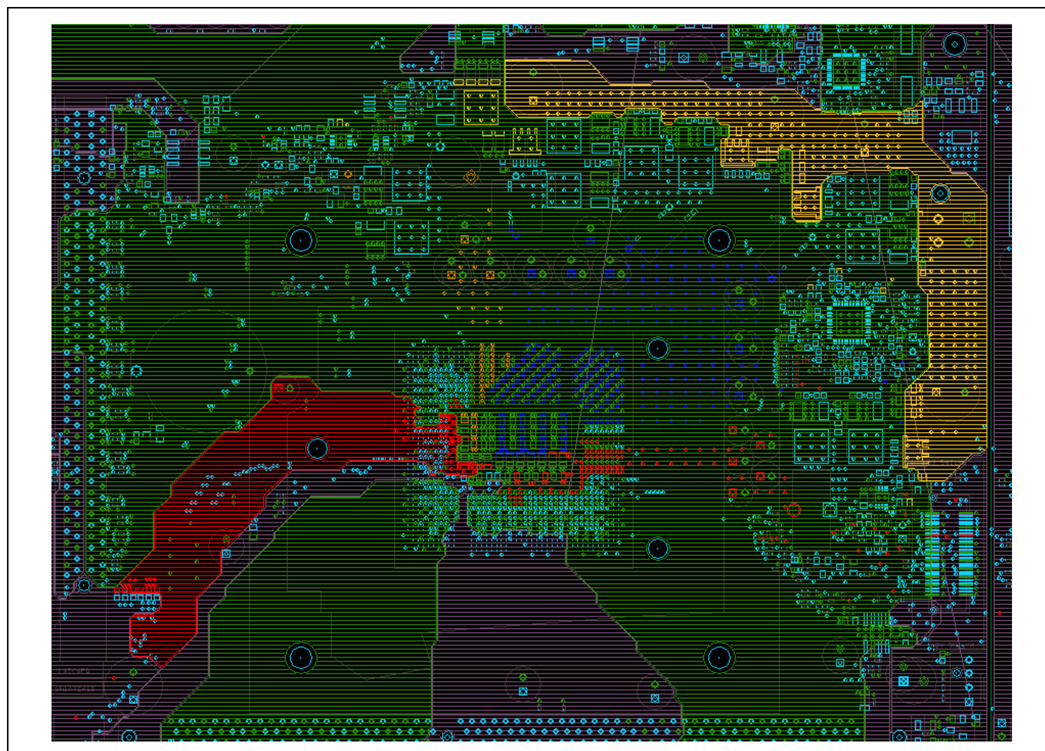


Figure 4-6. Layer 3 V_{SS} Routing for Intel® Reference Four-layer Motherboard

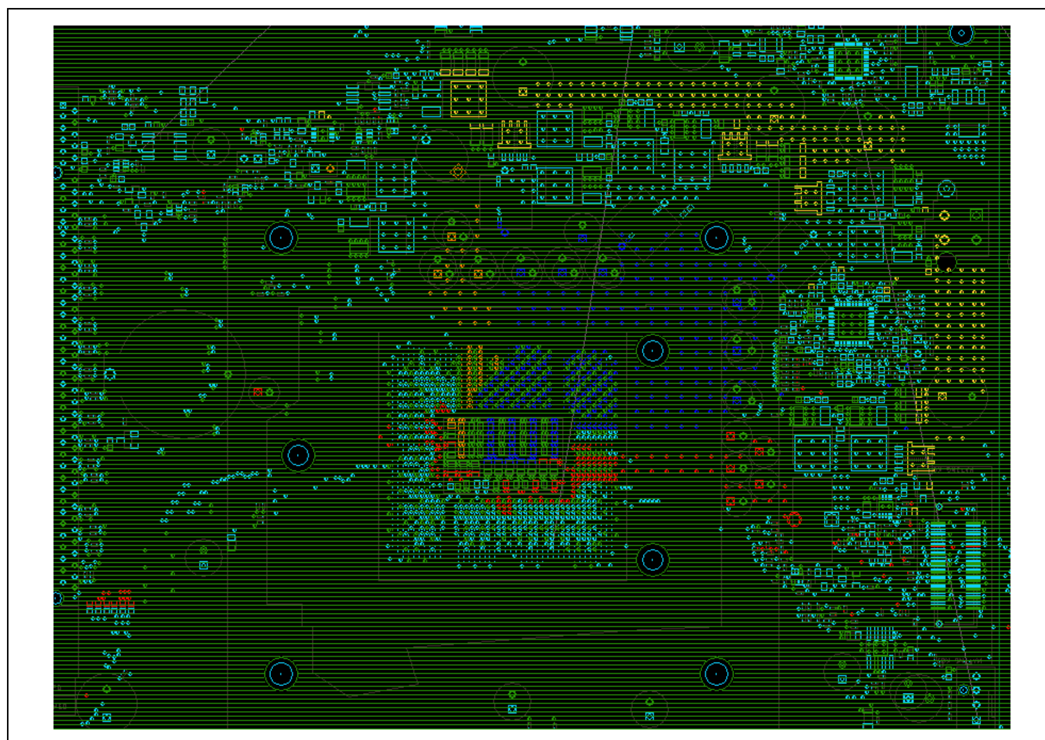
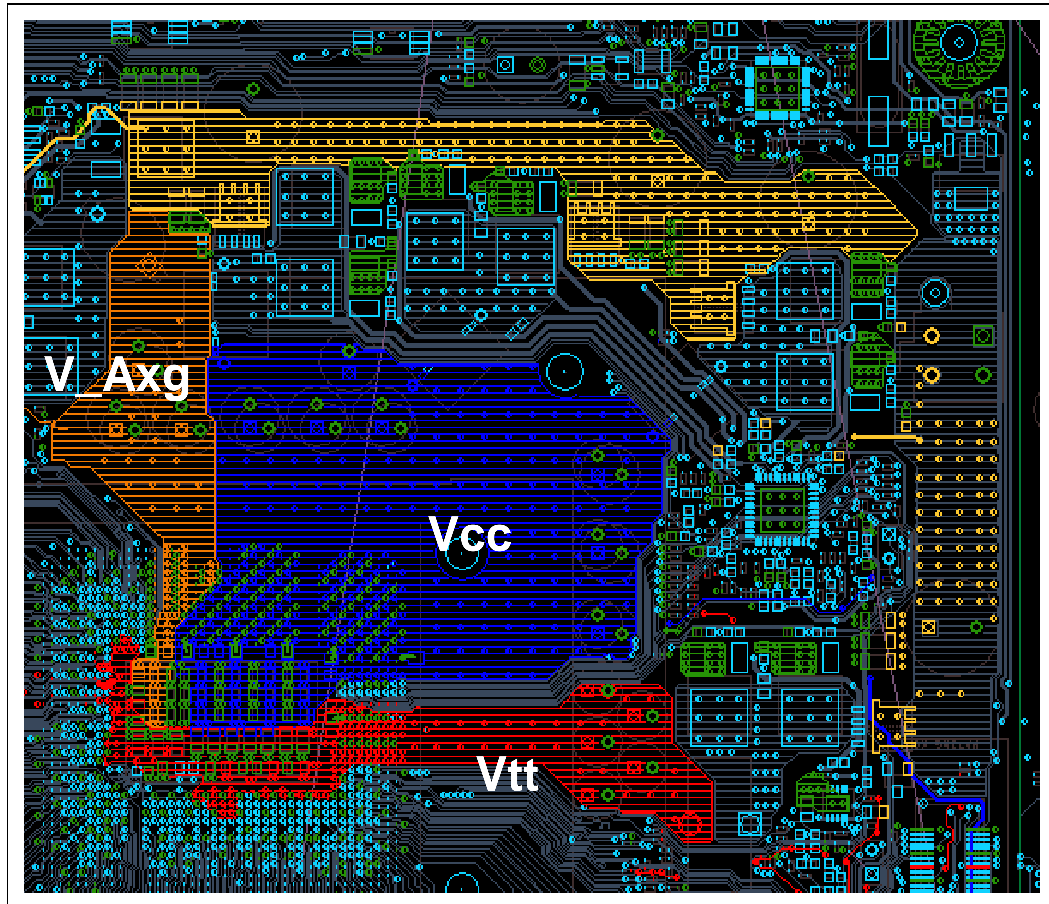


Figure 4-7. Layer 4 V_{CC} Shape for Intel® Reference Four-layer Motherboard

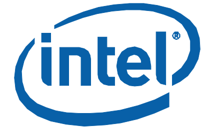


4.4.4 Six-layer Boards

Six-layer boards provide layout engineers with greater design flexibility compared to the four-layer standard. Adjacent plane pairs of the same potential are not useful at higher frequencies, so the best approach is to maximize adjacent, closely spaced V_{CC}/ V_{SS} plane pairs. The plane pair separated by the PCB core material is of lesser importance since it is generally an order of magnitude larger in spacing than other plane pairs in the stack-up. Because the V_{SS} planes are typically full floods of copper, an example of a well-designed six-layer stack-up will have 4 V_{CC} layers and two layers for V_{SS}. The DC resistive requirements (Section 4.4.1) of the power delivery loop can still be met because the V_{SS} floods are larger than the V_{CC} floods, and the higher frequency needs are considered as there are 4 V_{CC}/ V_{SS} plane pairs to deliver current and reduce inductance.

4.4.5 Resonance Suppression

V_{CC} power delivery designs can be susceptible to resonance phenomena capable of creating droop amplitudes in violation of loadline specifications. This is due to the interleaved levels of inductively-separated decoupling capacitance. Furthermore, these resonances may not be detected through standard validation and require engineering analysis to identify and resolve. If not identified and corrected in the design process, these resonant phenomena may yield droop amplitudes in violation of loadline

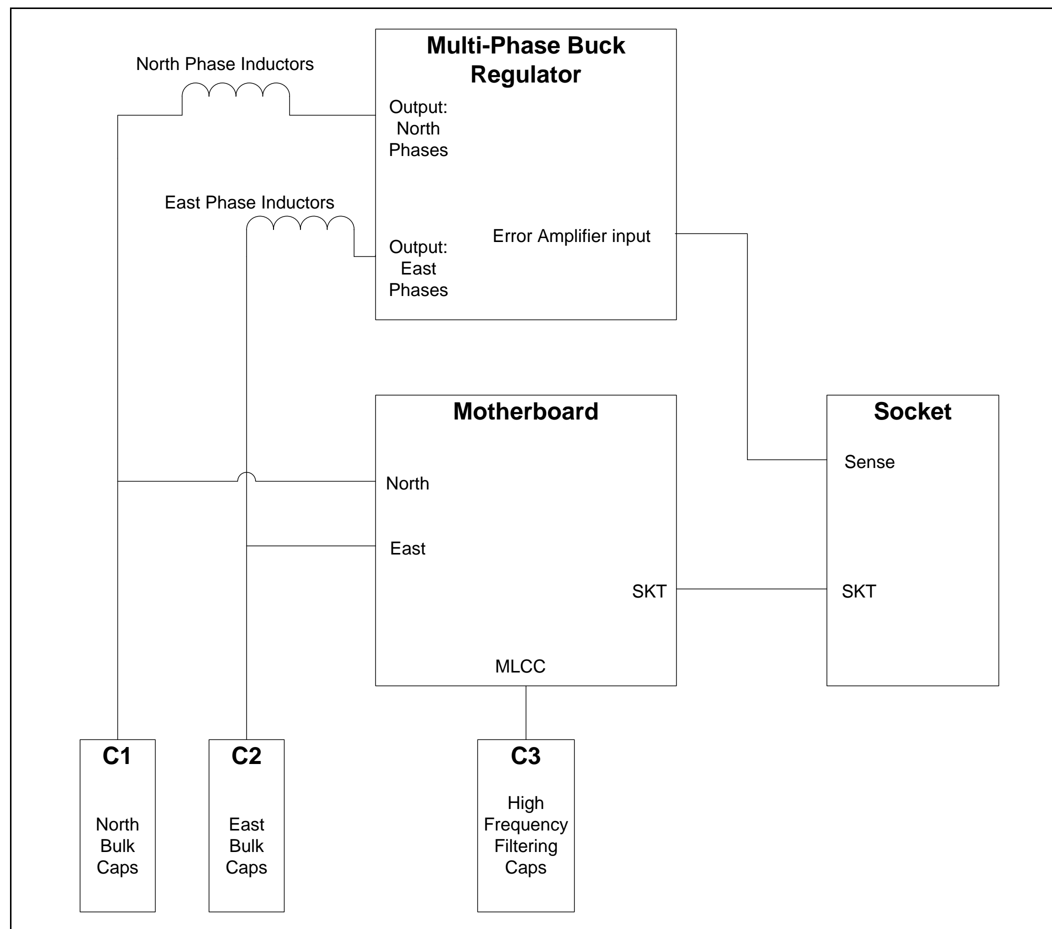


specifications by superimposing with standard VRD droop behavior. Frequency-dependent power delivery network impedance simulations and validation are strongly recommended to identify and resolve power delivery resonances before board are actually built. Careful modeling and validation can help to avoid voltage violations responsible for data corruption, system lock-up, or system ‘blue-screening’.

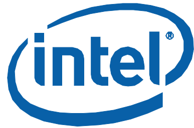
4.5 Electrical Simulation (EXPECTED)

The following electrical models are enclosed to assist with VRD design analysis and component evaluation for loadline compliance. The block diagram shown in Figure 4-8 is a simplified representation of the V_{CC} power delivery network of the Intel four-layer reference board. The board model, detailed in Figure 4-11, characterizes the power plane layout. The multiphase buck regulator and capacitor models should be obtained from each selected vendor. When fully integrated into electrical simulation software, this model can be used to evaluate PWM controller, capacitor, and inductor performance against the loadline and tolerance band requirements detailed in Section 4.2.1. To obtain accurate results, it is strongly recommended to create and use a custom model that represents the specific board design, PWM controller, and passive components that are under evaluation.

Figure 4-8. Simplified Reference Block Diagram



NOTE: Consult Figure 4-4 to Figure 4-7 for reference layout.



The motherboard model of Figure 4-11 represents the power delivery path of the Intel reference four-layer motherboard design. Input and output node locations are identified in Figure 4-12. Feedback to the PWM controller error amplifier should be tied to node 'Sense', the socket-motherboard interface. Nodes 'North' and 'East' are the locations where the output inductors of the buck regulator tie to the motherboard power plane. 'North' bulk capacitors, C1, are also connected to node 'North'. C1 represents the parallel combination of all capacitors and capacitor parasitics at this location. Node 'East' is the location where the 'east' bulk capacitors, C2, connect to the motherboard power plane. C2 represents the parallel combination of all capacitors and capacitor parasitics at this location. Node 'MLCC' represents the parallel combination of all capacitors and capacitor parasitics in the socket cavity and is connected to the mid-frequency filter, C3.

Typical capacitor models are identified in Figure 4-13. Each model represents the parallel combination of the local capacitor placement as identified in the previous paragraph. Recommended parallel values of each parameter are identified in Figure 4-11. Consult Section 1.1 for further details regarding bulk and mid-frequency capacitor selection.

The LGA1156 socket is characterized by two impedance paths that connect to the motherboard at 'North' ('north' connection), and 'East' ('east' connection). I_PWL is a piece-wise linear current step that is used to stimulate the voltage droop as seen at the motherboard-socket interface and is defined in Figure 4-15 and Table 4-11. This load step approximates the low frequency current spectrum that is necessary to evaluate bulk capacitor, mid-frequency capacitor and PWM controller performance. It does not provide high frequency content to excite package noise. The cavity capacitor solution, MLCC, is used as a reference for designing processor packaging material and should not be modified except to reduce ESR/ESL or increase total capacitance. Failure to observe this recommendation may make the motherboard incompatible with some processor designs.

The primary purpose of the simulation model is to identify options in supporting the loadline specification. Evaluation of the full power-path model will allow the designer to perform what-if analysis to determine the cost optimal capacitor and PWM controller configuration. This is especially useful in determining the capacitor configuration that can support loadline specifications across variation such as manufacturing tolerance, age degradation, and thermal drift. The designer is encouraged to evaluate different capacitor configurations and PWM controller designs. However, the designer should be aware that the feedback compensation network of most PWM controllers requires modification when the capacitor solution changes. Consult the PWM controller datasheet for further information.

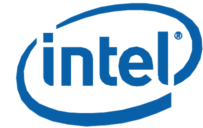


Figure 4-9. Example Voltage Droop Observed At Node 'Sense'

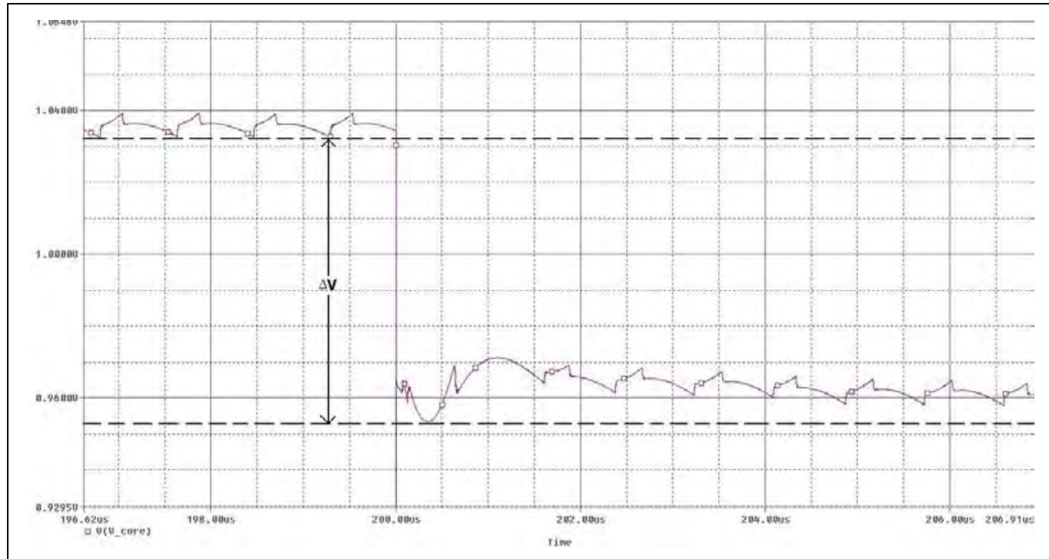
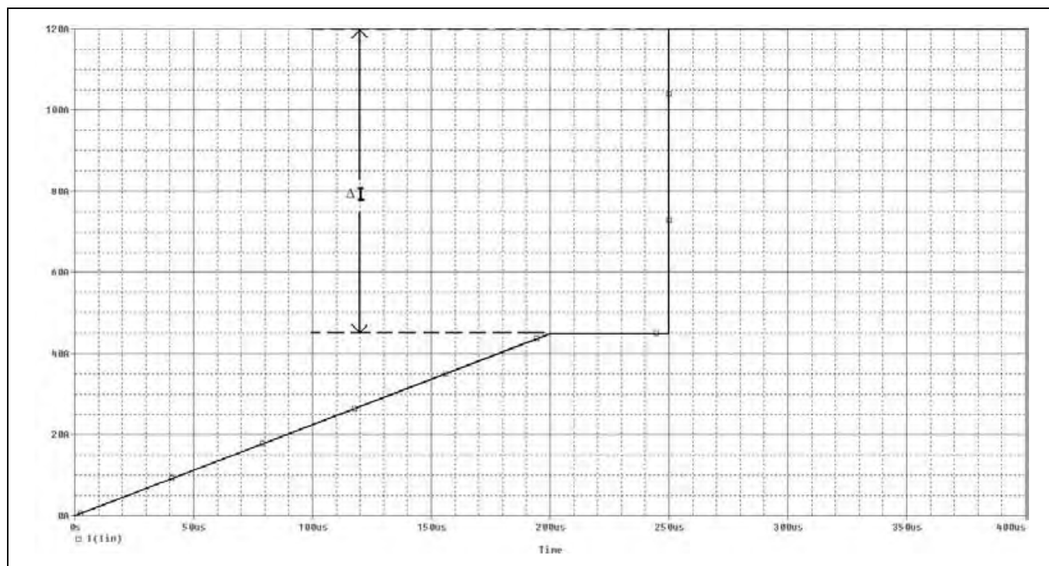


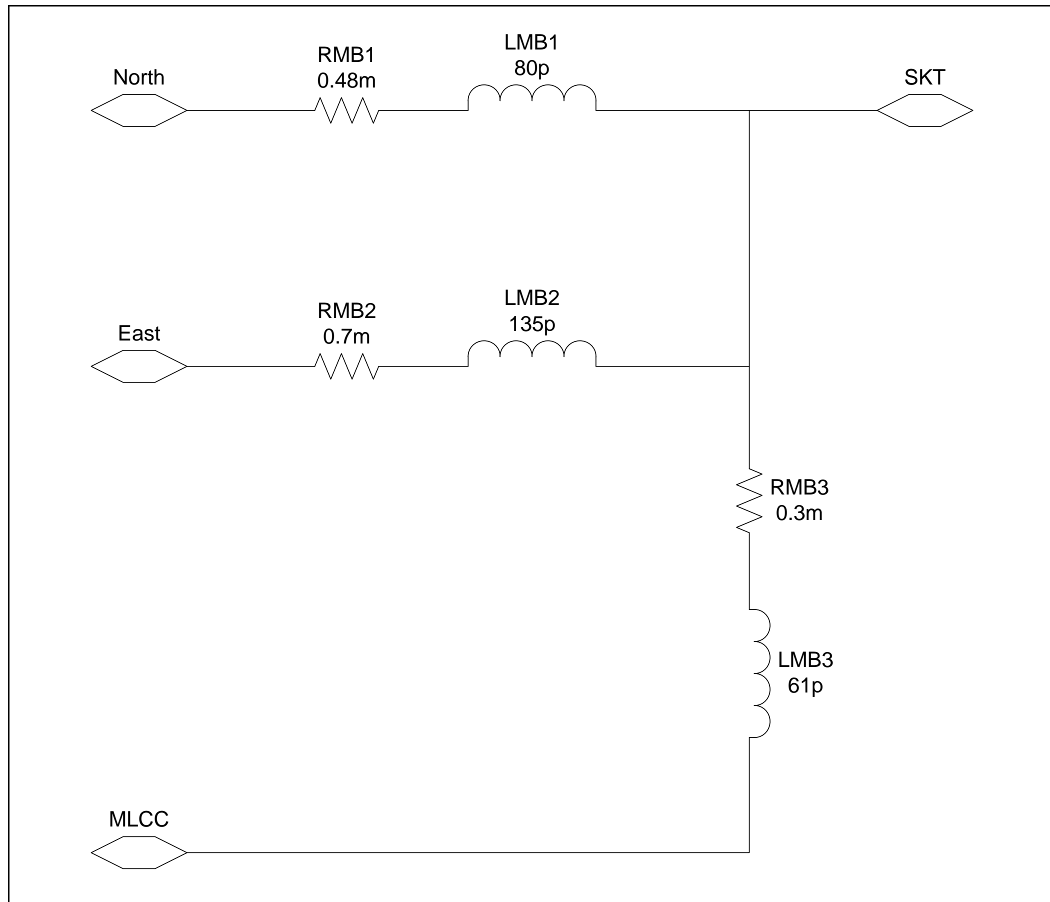
Figure 4-9 provides an example voltage droop waveform at node 'Sense', the socket-motherboard interface. The loadline value is defined as ∆V/∆I with ∆V measured at this node and the current step observed through I_PWL. The voltage amplitude is defined as the difference in the steady state voltage (prior to the transient) and the minimum voltage droop (consult Figure 4-9). Care must be taken to remove all ripple content in this measurement to avoid a pessimistic loadline calculation that will require additional capacitors (cost) to correct. Figure 4-10 provides an example current stimulus. The amplitude is measured as the difference in maximum current and steady state current prior to initiation of the current step. With ∆V and ∆I known, the loadline slope is simply calculated using Ohm's Law: $R_{LL} = \Delta V/\Delta I$.

Figure 4-10. Current Step Observed Through I_PWL



NOTE: To avoid excessive ringing in simulation, the system current should be slowly ramped from zero amps to the minimum recommended DC value prior to initiating the current step.

Figure 4-11. Schematic Diagram for the Four-layer Intel® Reference Motherboard



NOTE: Consult Figure 4-4 to Figure 4-7 for reference layout.

Table 4-8. Parameter Values for the Schematic of Figure 4-11

Parameter	Value	Comments
RMB1	0.48 mΩ	'North' power plane parasitic resistance from the buck regulator north output inductors to the LGA1156 socket connection.
RMB2	0.7 mΩ	Power plane parasitic resistance from 'east' power plane from the buck regulator east output inductor to the LGA1156 socket connection.
RMB3	0.3 mΩ	Power plane parasitic resistance from the LGA1156 socket cavity to the LGA1156 socket connection.
LMB1	80 pH	'North' power plane parasitic inductance from the buck regulator north output inductors to the LGA1156 socket connection.
LMB2	135 pH	Power plane parasitic inductance from 'east' power plane from the buck regulator east output inductor to the LGA1156 socket connection.
LMB3	61 pH	Power plane parasitic inductance from the LGA1156 socket cavity to the LGA1156 socket connection.

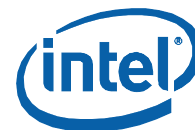


Figure 4-12. Node Location for the Schematic of Figure 4-11

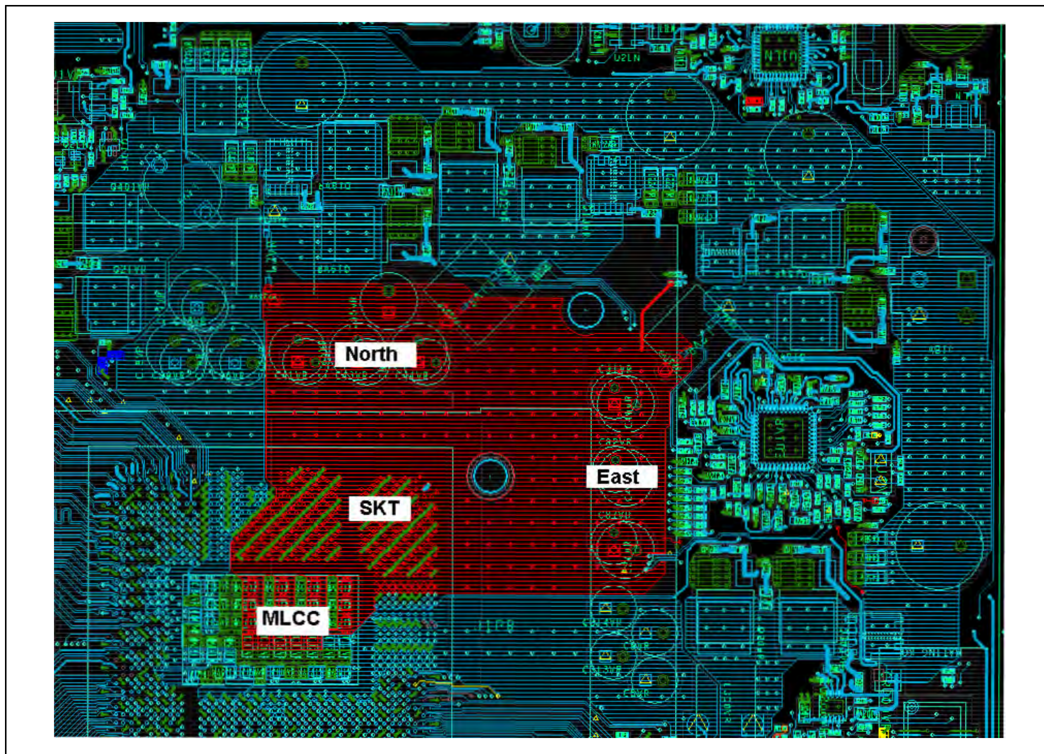
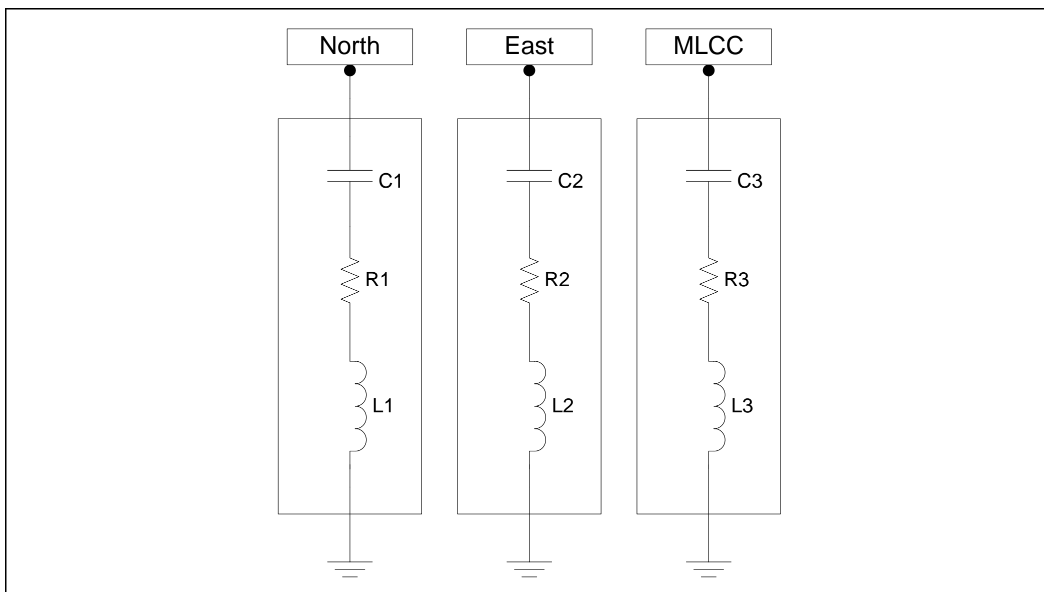


Figure 4-13. Schematic Representation of Mid-frequency Decoupling Capacitors



NOTES:

1. C1 represents the parallel model for 'north' location bulk decoupling.
2. C2 represents the parallel model for 'east' location bulk decoupling.
3. C3 represents the parallel model for mid-frequency decoupling located in the northeast corner of the socket cavity.

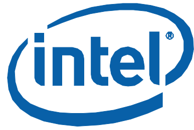


Table 4-9. Recommended Parameter Values for the Capacitors Models

Parameter	Value	Comments
C1	2240 μF[2]	Parallel equivalent for 'north' capacitors prior to age, thermal, and manufacturing degradation.
R1	1.75 mΩ[2]	Parallel equivalent for 'north' capacitor maximum ESR.
L1	500 pH[1, 2]	Parallel equivalent for 'north' capacitor maximum ESL.
C2	1680 μF[2]	Parallel equivalent for 'east' capacitors prior to DC bias, age, thermal, and manufacturing degradation.
R2	2.33 mΩ[2]	Parallel equivalent for 'east' capacitor maximum ESR.
L2	667 pH[1, 2]	Parallel equivalent for 'east' capacitor maximum ESL.
C3	243.1 μF[2]	Parallel equivalent for 'cavity' capacitors prior to age, thermal, and manufacturing degradation.
R3	294 μΩ[2]	Parallel equivalent for 'cavity' capacitor maximum ESR.
L3	32 pH[1, 2]	Parallel equivalent for 'cavity' capacitor maximum ESL.

NOTES:
1. Higher values of ESL may satisfy design requirements.
2. Contact capacitor vendors to identify values for the specific components used in your design.

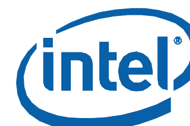


Figure 4-14. Schematic Representation of VR Test Tool Model

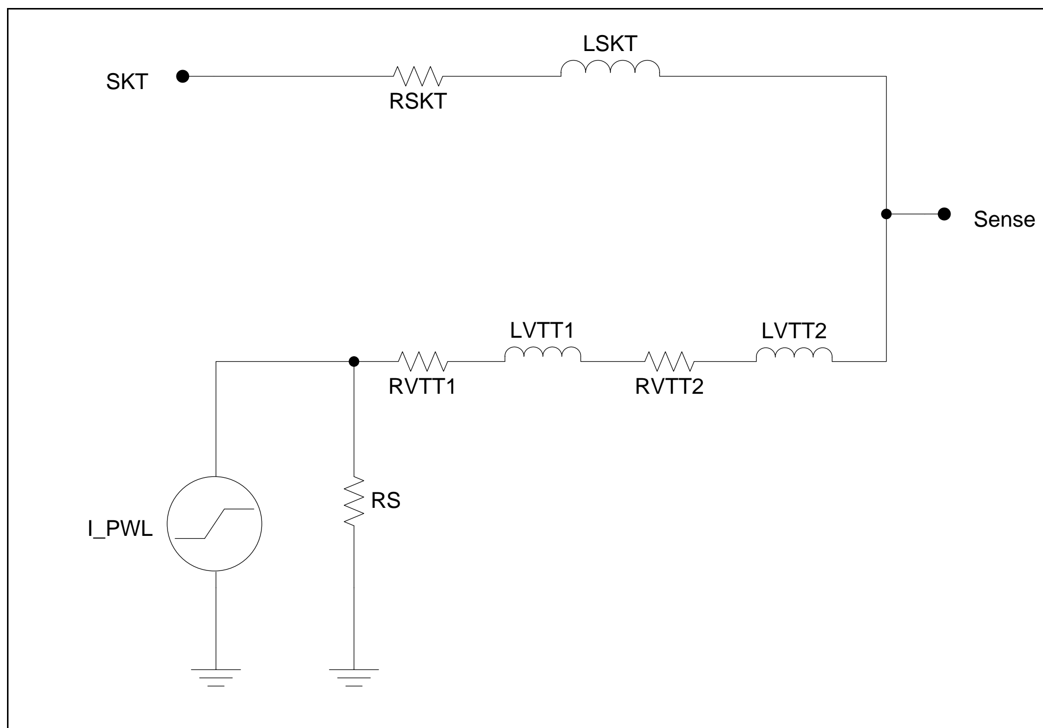


Table 4-10. Recommended Parameter Values for the Socket Model in Figure 4-14

Parameter	Value	Comments
RSKT	0.42 mΩ	LGA1156 'south' segment resistance
RVTT1	0.42 mΩ	Resistance of VTT Tool load board
RVTT2	0.91 mΩ	Resistance of VTT Tool socket adapter (interposer)
RS	100 kΩ	VTT Tool current source resistance
LSKT	40 pH	LGA1156 'north' segment inductance
LVTT1	240 pH	Inductance of VTT Tool load board
LVTT2	42 pH	Inductance of VTT Tool socket adapter (interposer)

NOTES: These values are from the LGA 775 VTT Tool load board. The values will be updated with values from the LGA 1156 VTT Tool load board when they become available.

Figure 4-15. Current Load Step Profile for I_PWL

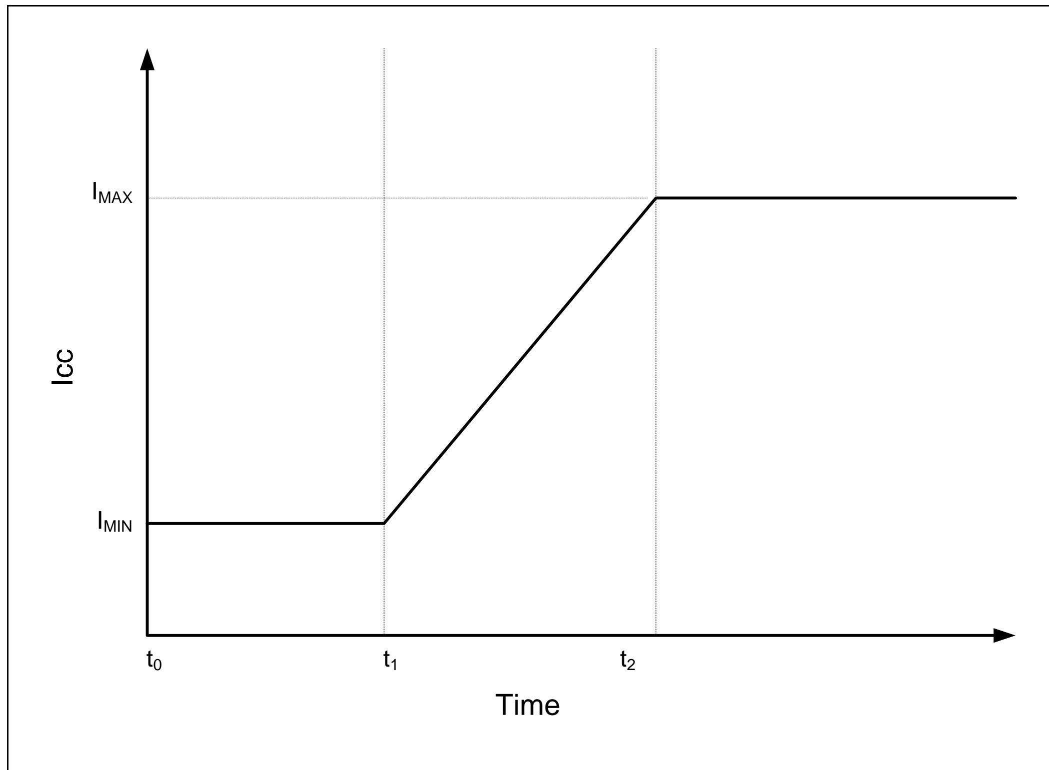
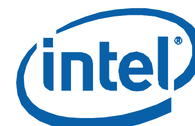


Table 4-11. I_PWL Current Parameters for Figure 4-15

Parameter	Value	Comments
t_0	0 s	Simulation ‘time zero’
t_1	100 µs	Time to initiate the current step. This parameter must be chosen at a time that the V_{CC} rail is residing at steady state.
t_2	t_1 + 50 ns	Time of maximum current[1]
Istep	75 A	Current step for loadline testing[1]
Imin	45 A	Minimum current for simulation analysis[1]
Imax	120 A	Maximum current for simulation analysis[1]

NOTE:

1. See Table 4-5. Intel® Processor Current Step Values for Transient Loadline Testing



4.6 LGA1156 Voltage Regulator Configuration Parameters

Table 4-12. 1156_VR_CONFIG_09A Specification Input Parameters

Definition	Variable Name	Value
Loadline Slope	LL_SLOPE	1.4 mΩ
Loadline Tolerance Band	TOB	19 mV
Maximum Overshoot Above VID	OS_AMP	50 mV
Maximum Overshoot Time Duration Above VID	OS_TIME	25 us
Peak To Peak Ripple Amplitude	RIPPLE	10 mV
Thermal Compensation Voltage Drift	THERMAL_DRIFT	2 mV
Iccmax	Iccmax	75 A
Dynamic Current Step	I_STEP	50 A
Voltage Regulator Thermal Design Current	VR_TDC	60 A
Current step rise time	I_RISE	100 ns
Current step fall time for overshoot	I_FALL	100 ns

Table 4-13. 1156_VR_CONFIG_09B Specification Input Parameters

Definition	Variable Name	Value
Loadline Slope	LL_SLOPE	1.4 mΩ
Loadline Tolerance Band	TOB	19 mV
Maximum Overshoot Above VID	OS_AMP	50 mV
Maximum Overshoot Time Duration Above VID	OS_TIME	25 us
Peak To Peak Ripple Amplitude	RIPPLE	10 mV
Thermal Compensation Voltage Drift	THERMAL_DRIFT	2 mV
Iccmax	Iccmax	110A
Dynamic Current Step	I_STEP	75 A
Voltage Regulator Thermal Design Current	VR_TDC	90 A
Current step rise time	I_RISE	100 ns
Current step fall time for overshoot	I_FALL	100 ns

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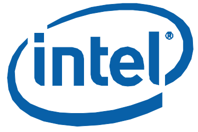

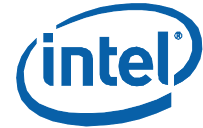

Appendix A Z(f) Impedance References

"Microprocessor Platform Impedance Characterization using VTT tools" by S Chickamenahalli, K. Aygün, M.J. Hill, K. Radhakrishnan, K. Eilert, E. Stanford in the proceedings of the *20th Annual IEEE Applied Power Electronics Conference and Exposition,* Vol. 3. pp. 1466-1469, March 2005.

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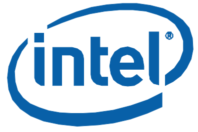
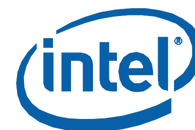




Appendix B Audible Noise Reduction

Audible noise frequency (pitch) is the fundamental plus several harmonics of the stimulus frequency. Presence of multiple harmonics, both odd and even, results in complex and very annoying noise characteristics. Audible noise amplitude (loudness) increases with larger VR output voltage change [dv] and faster output voltage change ramp Rate [dv/dt].

Simple math: I = C * dv / dt. Three conditions that need to be present simultaneously for acoustic noise. They are periodic dv/dt in audible range, large dv, and MLCC capacitors.

On the MCH, the processors have the C4 state enabled with VID changes up to 250 mV in one step when it enters/exits C4. These changes could be periodical at 1 KHz during an idle state. The minimum slew rate dv/dt requirement is 7.6mV/uS. Most designs would need a faster dv/dt for meeting latency requirement of 33 uS. At this fast slew rate and periodical entry/exit, the VR could potentially create audible noise which may be detected by end user in normal operation. There are steps that need to be taken for suppressing the audible noise.

The primary cause is from large inrush current due to high output capacitance. The first step is controlling the output capacitance by sizing output capacitor just enough to meet the transient requirement. A VR controller that has slew rate control with external pin is preferred for optimizing the dv/dt setting. Consult the controller datasheet or vendor FAE on how to program dv/dt. If the slew rate is not set properly, Vccp can slew faster than needed thus worsening the audible noise.

The second step is careful selection of output inductors to prevent inductor buzzing noise. The supplier can provide characterization noise given material selection and construction. In general, ferrite is noisier than metal composite. Make sure the inductor construction is rigid. The core has to be glued well together and cavity should be filled with epoxy.

Last but not least is MLCC, which is well known for making audible noise when exposed to large dv/dt. This is called the Piezo effect. The noise magnitude is proportional to number of MLCC in parallel. The input filter MLCCs should be (2) 4.7 uF X5R per phase. Avoid Y5V type since it is much more susceptible to Piezo effect. Place them on both sides of the input FET, not side by side. Increase the capacitance to 10uF if needed for minimizes the noise. The input bulk capacitors should be (2) 680 uF or larger for reducing dv/dt of the rail. For output high frequency decoupling, use 22 uF MLCC or bigger value to reduced number of needed capacitors. Use polymer chip capacitor in conjunction with MLCC when possible. Placing MLCC symmetrically on top and bottom side of the motherboard cancels out the vibration; thus, helping the noise.

Figure 4-16. Effect of Output Change on Input Currents

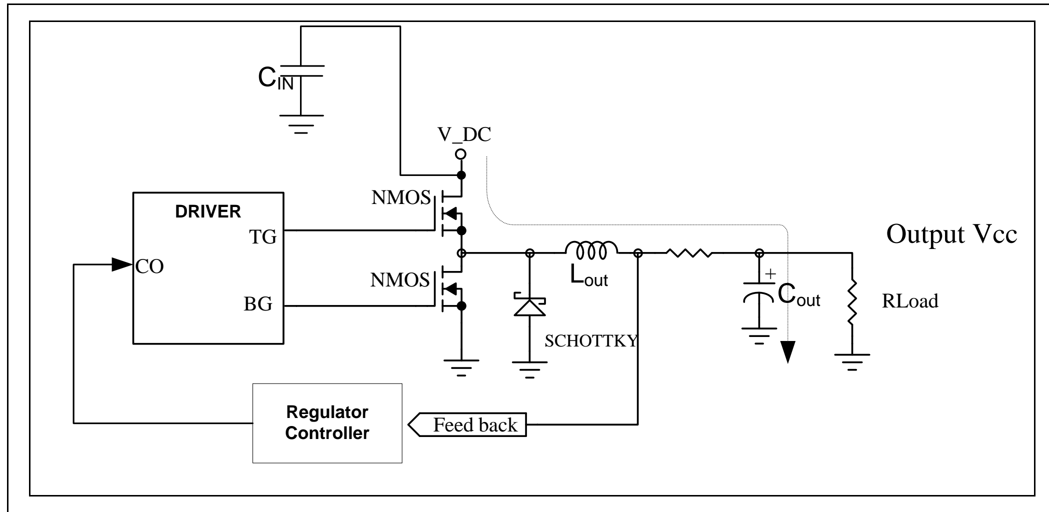
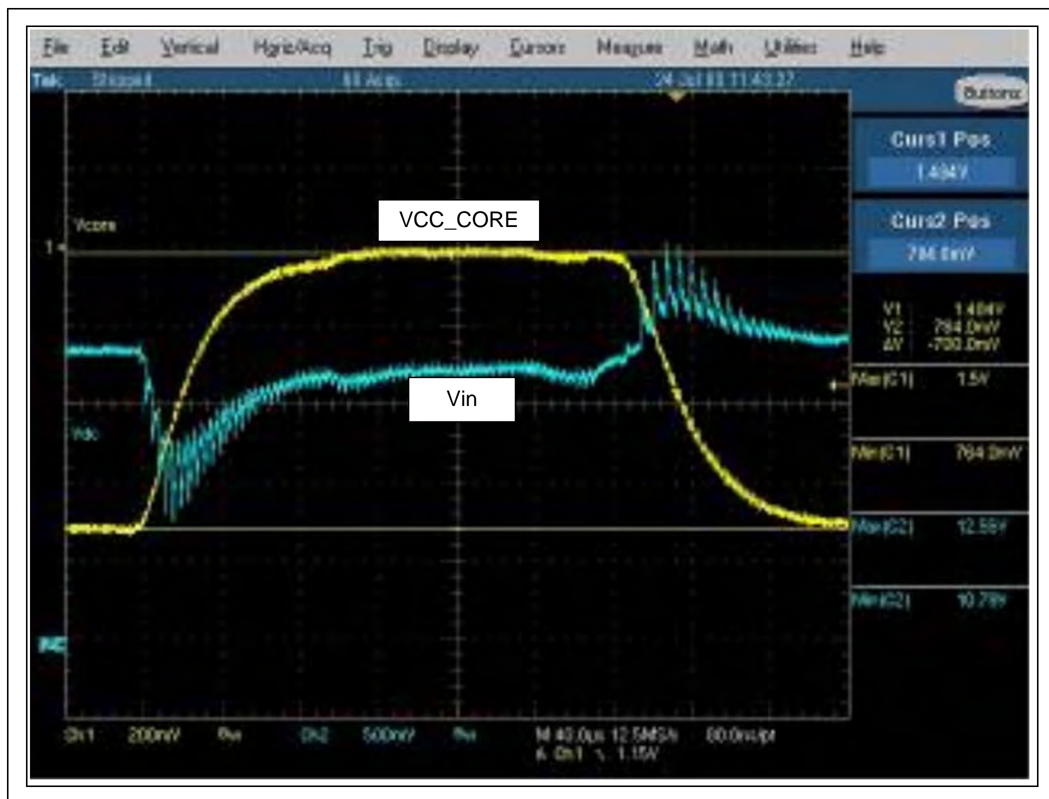


Figure 4-17. Input Voltage Drop Caused by di/dt Event at the Output



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