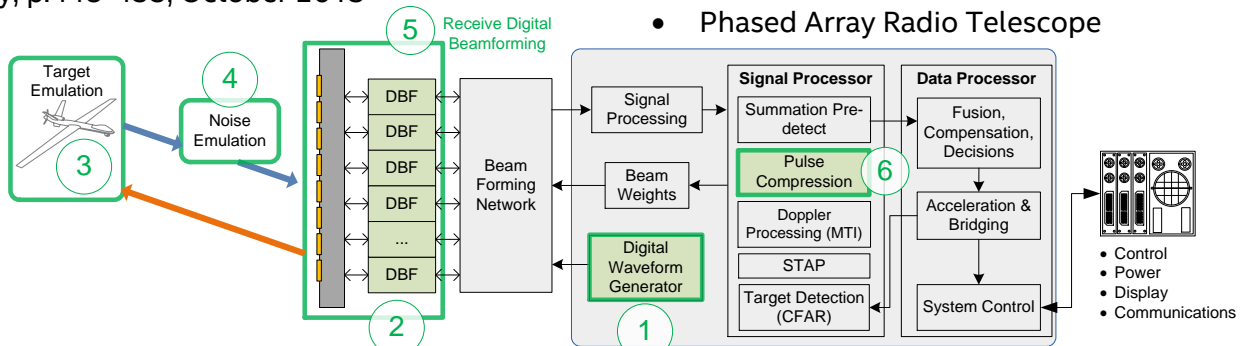# Time Delay Digital Beamforming

Example Design

DESCRIPTION

Radar system has been using a hybrid of analog and digital beamforming (DBF). Sub-arrays of phase shifters are digitized at the sub-array output. Such system suffers from limited bandwidth and produces only one beam at a time. Fully DBF solves both problems. Frequency domain DBF is very efficient in resource, but inherently narrowband.

Time Delay BF (TDBF), on the other hand is natively wideband and allows scalable number of simultaneous beams. With the advance of high density and low power FPGA, TDBF becomes possible. This reference design used a very efficient and precise fractional delay algorithm to achieve sub picosecond time delay. As a result, beamforming at a very fine angle can be achieved.

The design is implemented in Simulink with Altera DSP Builder Advanced Blockset. To test the design in hardware, other supportive components like chirp generator, target range emulation, Rx noise emulation, aperture tapering, and pulse compression are also implemented.

Reference: C. Cheung, R. Shah, M. Parker, "Time Delay Digital Beamforming for Wideband Pulsed Radar Implementation", in IEEE International Symposium on Phased Array Systems & Technology, p.448-455, October 2013

FEATURES

- Efficient DSP time delay algorithm
- BF engine time-shared between Tx and Rx
- Arbitrary fine beam angle resolution – 0.02 degree implemented
- Fully parameterizable design
- 6-8 beams of 32 antenna in a Stratix V
- Also completed with chirp generator, target range emulation, Rx noise emulation, and pulse compression
- Demo hardware controlled in Matlab environment
- Performance and Resource usage of a beam of 32 antennas:

Performance Examples	Spec. #1	Spec. #2	Spec. #3	Spec. #4
Sample Rate (MHz)	300	300	267	250
Signal Bandwidth (MHz)	200	200	200	200
Filter Length	6	8	12	16
Expected SNR (dB)	34	52	60	65
Multipliers (18x18)	416	544	800	1056
Logics (max 260k)	8140	8800	9300	10k
Block RAM	64	64	64	64
Compiled Fmax. (MHz)	310	304	284	284

APPLICATIONS

- Active Electronically Scanned Array (AESA)
- Radar, Sonar
- Electronic Warfare and Software Defined Radio
- Phased Array Radio Telescope

For more information about Intel® FPGA Example Design Contact Intel