

This chapter provides an overview of features available in the HardCopy® III device family. More details about these features can be found in their respective chapters.

HardCopy III devices are Altera's low-cost, high-performance, low-power ASICs with pin-outs, densities, and architectures that complement Stratix® III devices.

HardCopy III device features, such as phase-locked loops (PLLs), embedded memory, and I/O elements (IOEs), are functionally and electrically equivalent to the Stratix III FPGA features. The combination of the Quartus® II software for design, Stratix III FPGAs for in-system prototype and design verification, and HardCopy III devices for high-volume production, provides a complete, low-risk design solution to meet your business needs.

HardCopy III devices improve on the successful and proven methodology of the previous generations of HardCopy devices. Altera® HardCopy III devices use the same base arrays across multiple customer designs for a given device density. They are customized using only two metal and three via layers. The Quartus II software provides a complete set of tools for designing the Stratix III FPGA prototypes and the HardCopy III ASICs. HardCopy III devices are also supported through other front-end design tools from Synopsys and Mentor Graphics®.

Based on a 0.9-V, 40-nm process, the HardCopy III family is an alternative to the standard cell ASIC for low-cost, high-performance logic, digital signal processing (DSP), and embedded designs.

This chapter contains the following sections:

- “Features” on page 1–2
- “Architectural Features” on page 1–9
- “Software Support and Part Number Information” on page 1–13

Features

HardCopy III devices offer the following features:

- General
 - Fine-grained HCell architecture resulting in a low-cost, high-performance, low-power ASIC
 - Fully tested production-quality samples typically available 14 weeks from the date of your design submission
 - Design functionality the same as the Stratix III FPGA prototype
- System performance and power
 - Core logic performance up to 50% faster than the Stratix III FPGA prototype
 - Power consumption reduction of typically 50% or greater from the Stratix III FPGA prototype
 - Robust on-chip hot socketing and power sequencing support
 - Support for instant-on or instant-on-after-50 ms power-up modes
 - I/O:GND:PWR ratio of 8:1:1 along with on-die and on-package decoupling for robust signal integrity



The actual performance and power consumption improvements described in this data sheet are design-dependent.

- Logic and Digital Signal Processing (DSP)
 - 2.7 to 7 million usable gates for both logic and DSP functions (as shown in [Table 1-1](#))
 - High-speed DSP functions supporting 9×9 , 12×12 , 18×18 , and 36×36 multipliers, multiple accumulate functions, and finite impulse response (FIR) filters
- Internal memory
 - TriMatrix memory, consisting of three RAM block sizes to implement true dual-port memory and first-in first-out (FIFO) buffers
 - Up to 16,272 Kbits RAM in embedded RAM blocks (including parity bits)
 - Memory logic array blocks (MLAB) implemented in HCell logic fabric
- Clock resources PLLs
 - Up to 16 global clocks, 88 regional clocks, and 88 peripheral clocks per device
 - Clock control block supporting dynamic clock network enable/disable and dynamic global clock network source selection
 - Up to 12 PLLs per device supporting PLL reconfiguration, clock switchover, programmable bandwidth, clock synthesis, and dynamic phase shifting

- I/O standards, external memory interface, and intellectual property (IP)
 - Support for numerous single-ended and differential I/O standards, such as LVTTTL, LVCMOS, PCI, PCI-X, SSTL, HSTL, and LVDS
 - High-speed differential I/O support with serializer/deserializer (SERDES) and dynamic phase alignment (DPA) circuitry for 1.25 Gbps performance
 - Support for high-speed networking and communications bus standards, including SPI-4.2, SFI-4, SGMII, Utopia IV, 10 Gigabit Ethernet XSLI, Rapid I/O, and NPSI
 - Memory interface support with dedicated DQS logic on all I/O banks
 - Dynamic On-Chip Termination (OCT) with auto-calibration support on all I/O banks
 - Support for high-speed external memory interfaces, including DDR, DDR2, DDR3 SDRAM, RLDRAM II, QDR II, and QDR II+ SRAM on up to 20 modular I/O banks
 - Support for multiple intellectual property megafunctions from Altera MegaCore® functions and Altera Megafunction Partners Program (AMPPSM)
 - Nios® II embedded processor support
- JTAG—IEEE 1149.1 boundary scan testing (BST) support
- Packaging
 - Pin-compatible with Stratix III FPGA prototypes
 - Up to 880 user I/O pins available
 - Flip chip, space-saving FineLine BGA packages available (Table 1-3)

Table 1-1 lists the HardCopy III ASIC devices and available features.

Table 1-1. HardCopy III ASIC Family Features (Part 1 of 2)

HardCopy III ASIC	Stratix III FPGA Prototype	ASIC Equivalent Gates (1)	M9K Blocks	M144K Blocks	Total Dedicated RAM Bits (not including MLABs) (2)	18 × 18-Bit Multipliers (FIR Mode)	PLLs
HC325	EP3SL110	2.7 M	275	12	4,203 Kb	288	4
	EP3SL150	3.6 M	355	16	5,499 Kb	384	4
	EP3SE110	5.8 M	639	16	8,055 Kb	896	4
	EP3SL200	5.3 M	468	32	8,820 Kb	576	4
	EP3SE260	6.9 M	864	32	12,384 Kb	768	4
	EP3SL340	7.0 M	864	32	12,384 Kb	576	4

Table 1-1. HardCopy III ASIC Family Features (Part 2 of 2)

HardCopy III ASIC	Stratix III FPGA Prototype	ASIC Equivalent Gates (1)	M9K Blocks	M144K Blocks	Total Dedicated RAM Bits (not including MLABs) (2)	18 × 18-Bit Multipliers (FIR Mode)	PLLs
HC335	EP3SL150	3.6 M	355	16	5,499 Kb	384	8
	EP3SE110	5.8 M	639	16	8,055 Kb	896	8
	EP3SL200	5.3 M	468	36	9,396 Kb	576	12 (3)
	EP3SE260	6.9 M	864	48	14,688 Kb	768	12 (3)
	EP3SL340	7.0 M	1,040	48	16,272 Kb	576	12 (3)

Notes to Table 1-1:

- (1) This is the number of ASIC equivalent gates available in the HardCopy III base array, shared between both adaptive logic module (ALM) logic and DSP functions from a Stratix III FPGA prototype. The number of ASIC equivalent gates usable is bounded by the ALMs and DSP functions in the companion Stratix III FPGA device.
- (2) MLAB RAMs are implemented with HCells in the HardCopy III ASICs.
- (3) This device has 12 PLLs in the F1517 package and 8 PLLs in the F1152 package.

HardCopy III ASIC and Stratix III FPGA Mapping Paths

HardCopy III devices offer pin-to-pin compatibility with the Stratix III prototype, making them drop-in replacements for the FPGAs. Therefore, the same system board and software developed for prototyping and field trials can be retained, enabling the lowest risk and fastest time-to-market for high-volume production.

HardCopy III devices also offer non-socket replacement mapping paths to smaller standard or customized packages. For example, you can map the EP3SL110 device in the 780-pin FBGA package to the HC325 device in the 484-pin FBGA standard package, or to the 400-pin FBGA customized package. Because the pin-out for the two packages are not the same, you need a separate board design for the Stratix III device and the HardCopy III device.

The non-socket replacement offerings extend cost reduction further and allow for a smaller foot print occupied by the HardCopy III device. The non-socket replacement to a standard package is supported in the Quartus II software. The customized package option is not visible in the Quartus II software. For more information, refer to [“HardCopy III Package Pro”](#) on page 1-7.

For the non-socket replacement to a standard package, select I/Os in the Stratix III device that can be mapped to the HardCopy III device. Not all I/Os in the Stratix III device are available in the HardCopy III non-socket replacement device. Check the pin-out information for both the Stratix III device and HardCopy III device to ensure that the I/Os can be mapped, and select the companion device in the Quartus II project setting during design development. By selecting the companion device, the Quartus II software ensures that common resources and compatible I/Os are used during the mapping from the Stratix FPGA to the HardCopy ASIC.

There are a number of FPGA prototype choices for each HardCopy III device, as listed in [Table 1-2](#). To obtain the best value and the lowest system cost, architect your system to maximize silicon resource utilization.

Table 1–2. Stratix III FPGA Prototype to HardCopy III ASIC Mapping Paths (Note 1)

HardCopy III ASIC	HardCopy III Package	Stratix III FPGA Prototype and Package															
		EP3SL110			EP3SL150			EP3SE110		EP3SL200			EP3SE260			EP3SL340	
		F780	F780	F1152	F780	F1152	F780	F1152	F1517	H780	F1152	F1517	H780	F1152	F1517	H1152	F1517
HC325	484-pin FineLine BGA	✓ (2)	✓ (2)	—	✓ (2)	—	✓ (2)	—	—	✓ (2)	—	—	✓ (2)	—	—	✓ (2)	—
	780-pin FineLine BGA	✓	✓	—	✓	—	✓ (3)	—	—	✓ (3)	—	—	✓ (2)	—	—	✓ (2)	—
HC335	1152-pin FineLine BGA	—	—	✓	—	✓	—	✓	—	—	✓	—	—	—	—	—	—
	1517-pin FineLine BGA	—	—	—	—	—	—	—	—	—	✓	—	—	—	—	—	✓

Notes to Table 1–2:

- (1) HardCopy III device migration paths are not supported for the EP3SL50, EP3SL70, EP3SE50, and EP3SE80 Stratix III devices.
- (2) This mapping is a non-socket replacement path that requires a different board design for the Stratix III device and the HardCopy III device.
- (3) The Hybrid FBGA package requires additional unused board space along the edges beyond the footprint, but its footprint is compatible with the regular FBGA package.

Three different FineLine BGA package substrate options are available for the HardCopy III devices:

- Performance-optimized flip chip package (F)
- Cost-optimized flip chip package (L, LA)
- Low-cost wire bond package (W)

All three package types support direct replacement of the Stratix III FPGA prototype. The performance-optimized flip chip package supports equivalent performance and the same number of I/Os as the corresponding FPGA prototype. The cost-optimized flip chip package uses a substrate with fewer layers and no on-package decoupling (OPD) capacitors to offer a low-cost package option. The performance is reduced from that of the FPGA prototype. However, the number of available I/Os remains the same. The wire bond package offers another low-cost package option, but with the trade-off of reduced performance and fewer available I/Os.



If you are going to use the low-cost wire bond package, make sure your design uses I/Os that are available in that package.

For HardCopy III non-socket replacement devices, only the performance-optimized flip chip package and the low-cost wire bond package are supported.

HardCopy III devices are available in the packages shown in [Table 1–3](#).

Table 1–3. HardCopy III and Stratix III Package, I/O Pin Count, and LVDS Pair Count Mapping Notes (1), (2), (3), (4)

HardCopy III ASIC	WF484 FF484			WF780			FF780			LF1152 FF1152		LF1517 FF1517
	F780	H780	H1152	F780	H780	H1152	F780	H780	H1152	F1152	H1152	F1517
HC325	296, 48			392, 48			488, 56			—		—
HC335	—			—			—			774, 88		880, 88
Companion Mapping	↕			↕			↕			↕		↕
Stratix III FPGA Prototype	F780	H780	H1152	F780	H780	H1152	F780	H780	H1152	F1152	H1152	F1517
EP3SL110	488, 56	—	—	488, 56	—	—	488, 56	—	—	—	—	—
EP3SL150	488, 56	—	—	488, 56	—	—	488, 56	—	—	744, 88	—	—
EP3SE110	488, 56	—	—	488, 56	—	—	488, 56	—	—	744, 88	—	—
EP3SL200	—	488, 56	—	—	488, 56	—	—	488, 56	—	744, 88	—	976, 88
EP3SE260	—	488, 56	—	—	488, 56	—	—	488, 56	—	744, 88	—	976, 112
EP3SL340	—	—	744, 88	—	—	744, 88	—	—	744, 88	—	744, 88	976, 112

Notes to Table 1–3:

- (1) The numbers in the table indicate I/O pin count and full duplex LVDS pairs.
- (2) The first letter in the HardCopy III package name refers to the following: F—Performance-optimized flip-chip package, L—Cost optimized flip-chip package, W—Low-cost wire bond package.
- (3) For the F484, F780, and F1152 packaged devices, the I/O pin counts include the eight dedicated clock inputs (CLK1p, CLK1n, CLK3p, CLK3n, CLK8p, CLK8n, CLK10p, and CLK10n) that can be used for data inputs.
- (4) For the F1517 packaged devices, the I/O pin counts include the eight dedicated clock inputs (CLK1p, CLK1n, CLK3p, CLK3n, CLK8p, CLK8n, CLK10p, and CLK10n) and the eight dedicated corner PLL clock inputs (PLL_L1_CLKp, PLL_L1_CLKn, PLL_L4_CLKp, PLL_L4_CLKn, PLL_R4_CLKp, PLL_R4_CLKn, PLL_R1_CLKp, and PLL_R1_CLKn) that can be used for data inputs.

HardCopy III Package Pro

The HardCopy III Package Pro is a customized package program, which gives you the option to select a package tailored to the number of I/O's used in your design. This customized package will support less I/O's than what is available as a standard package offering. HardCopy III Package Pro will have a smaller foot print than a Stratix III FPGA prototype or a HardCopy III non-socket replacement standard package. The optimized package may further extend the cost savings over traditional HardCopy III device offerings.

Table 1-4 lists the available FineLine Ball-Grid Array (FBGA) packages and the maximum supported I/O for HardCopy III devices.

Table 1-4. HardCopy III FBGA Maximum I/O Pin Count

HardCopy III ASIC	FF400	FF484	WF572 (1)	FF572	WF672 (1)	FF672	FF780	FF1020
Package Dimension (mm) (2)	21 × 21	23 × 23	25 × 25	25 × 25	27 × 27	27 × 27	29 × 29	33 × 33
HC325	216	—	336	336	384	384	—	—
HC335	—	264	—	304	—	352	456	640

Notes to Table 1-4:

- (1) Low-Cost Wirebond Package (W)
- (2) Dimensions are approximate. See the Altera Device Package Information Datasheet for specifications that resemble the package offering in this table.

HardCopy III Package Pro is also offered in Ultra FineLine Ball-Grid Array (UBGA) packages. These packages have a 0.8 mm ball pitch, which increases the I/O count when compared to an FPGA package of the same dimension. Table 1-5 lists the available UBGA packages and the maximum supported I/O for HardCopy III devices.


Table 1-5. HardCopy III UBGA Maximum I/O Pin Count

HardCopy III ASIC	FU572	FU672	WU780 (1)	FU780
Package Dimension (mm) (2)	21 × 21	23 × 23	25 × 25	25 × 25
HC325	336	384	384	480
HC335	—	352	—	456

Notes to Table 1-5:

- (1) Low-Cost Wirebond Package (W)
- (2) Dimensions are approximate. See the Altera Device Package Information Datasheet for specifications that resemble the package offering in this table.

HardCopy III Package Pro is not visible in the Quartus II software, so you will not be able to select a Package Pro device as a companion device to your Stratix III device. However, you still need the Quartus II software to compile your design into an appropriate HardCopy III device prior to migrating to a Package Pro option.

 HardCopy III Package Pro details and specifications are not provided in the HardCopy III handbook, and electrical and thermal performance must be considered when designing with Package Pro. Contact your Altera representative to engage the HardCopy III Package Pro program.

Differences Between HardCopy III and Stratix III Devices

HardCopy III devices have several architectural differences from Stratix III devices. When implementing your design and laying out your board, consider these differences. Use the following information to ensure that your design maps from the Stratix III FPGA to the HardCopy III ASIC:

- Maximum core voltage of 0.9-V in HardCopy III devices compared with selectable core voltages of 0.9-V or 1.1-V in Stratix III devices
- Maximum V_{CCIO} power supply of 3.0-V
- HardCopy III power supply ramp time for fast POR mode is 4 ms, and 12 ms for Stratix III devices
 - You may need to use external clamping diodes on the board to keep the pins operating within specification.
 - 3.3-V LVTTTL/LVCMOS I/O standard is not supported in HardCopy III devices.
- Configuration is not required for HardCopy III devices, so the following Stratix III features are not supported:
 - Programming modes and features such as remote update and Programmer Object File (.pof) encryption
 - Cyclical redundancy check (CRC) for configuration error detection
 - 256-bit (AES) volatile and non-volatile security keys to protect designs
 - JTAG instructions used for configuration
- FPGA configuration emulation mode is not supported in HardCopy III devices.
- Boundary scan (BSCAN) chain length is different and varies with device density.
- HardCopy III devices contain up to a maximum of 20 I/O banks compared with 24 I/O banks in the Stratix III devices.
- Memory Initialization Files (.mif) for embedded memories used as RAM are not supported. The .mifs for memories used as ROM are supported because the data are mask-programmed into the memory cells.
- Stratix III logic array block (LAB), MLAB, and DSP functions are implemented with HCells in HardCopy III devices instead of dedicated blocks.
- Stratix III programmable power technology is not supported in HardCopy III devices. However, the HardCopy III architecture offers performance on par with Stratix III devices with significantly lower power.

Architectural Features

This section describes the architectural features of HardCopy III ASICs.

Logic Array Block and Adaptive Logic Module Function Support

HardCopy III devices fully support the Stratix III LAB and ALM functions. The basic building blocks of Stratix III LABs are composed of ALMs that you can configure to implement logic, arithmetic, and register functions. Each LAB consists of 10 ALMs, carry chains, shared arithmetic chains, LAB control signals, local interconnect, and register chain connection lines.

In HardCopy III devices, the basic building blocks of the core array are HCells, which are a collection of logic transistors connected together to provide the same functionality as the Stratix III LABs and ALMs. The Quartus II software maps these LAB and ALM functions to HCell macros, which define how the HCells are connected together in the HardCopy III core array. Only HCells required to implement the customer design are used, and unused HCells are powered down. This allows efficient use of the core fabric and offers significant static power savings.

The Stratix III LAB derivative, called MLAB, is also supported in HardCopy III devices. The MLAB adds static random access memory (SRAM) capability to the LAB and can provide a maximum of 640 bits of simple dual-port SRAM. Like the LAB functions, the Quartus II software maps MLAB functions to HCell macros in HardCopy III devices to provide the same Stratix III functionality.



For more information about LABs and ALMs, refer to the *Logic Array Block and Adaptive Logic Module Implementation in HardCopy III Devices* chapter.



For more information about MLAB modes, features, and design considerations, refer to the *TriMatrix Embedded Memory Blocks in HardCopy III Devices* chapter.

DSP Function Support

HardCopy III devices fully support the DSP block functions of Stratix III devices. Complex systems such as WiMAX, 3GPP WCDMA, CDMA2000, voice over Internet protocol (VoIP), H.264 video compression, and high-definition television (HDTV) require high-performance DSP circuits to handle large amounts of data with high throughput. These system designs typically use DSP to implement finite impulse response (FIR) filters, complex FIR filters, infinite impulse response (IIR) filters, fast Fourier transform (FFT) functions, and discrete cosine transform (DCT) functions.

In HardCopy III devices, these DSP block functions are implemented with HCells. The Quartus II software maps the Stratix III DSP functions to HCell macros in HardCopy III devices, preserving the same functionality. Implementing DSP functions using HCells also allows efficient use of the HardCopy III device core fabric and offers significant static power savings.

HardCopy III devices support all Stratix III DSP configurations (9×9 , 12×12 , 18×18 , and 36×36 multipliers) and block features, such as dynamic sign controls, dynamic addition and subtraction, dynamic rounding and saturation, and dynamic input shift registers. All five operational modes of the Stratix III DSP block are supported:

- Independent multiplier (9×9 , 12×12 , 18×18 , and 36×36)

- Two-multiplier adder
- Four-multiplier adder
- Multiply accumulate
- Shift mode

 For more information about DSP blocks, refer to the *DSP Block Implementation in HardCopy III Devices* chapter.

TriMatrix Embedded Memory Blocks

TriMatrix embedded memory blocks provide three different sizes of embedded SRAM to efficiently address the needs of HardCopy III ASIC designs. TriMatrix memory includes the following types of blocks:

- 640-bit MLAB blocks optimized to implement filter delay lines, small FIFO buffers, and shift registers. MLAB blocks are implemented in HCell macros.
- 9-Kbit M9K blocks that can be used for general purpose memory applications.
- 144-Kbit M144K blocks that are ideal for processor code storage, packet, and video frame buffering.


You can configure each embedded memory block independently to be a single- or dual-port RAM, ROM, or shift register using the Quartus II MegaWizard™ Plug-In Manager. Multiple blocks of the same type can also be stitched together to produce larger memories with minimal timing penalty. TriMatrix memory provides up to 16,272 Kbits of dedicated, embedded SRAM.

 For more information about TriMatrix memory blocks, modes, features, and design considerations, refer to the *TriMatrix Embedded Memory Blocks in HardCopy III Devices* chapter.

Clock Networks and PLLs

HardCopy III devices provide dedicated global clock networks (GCLKs), regional clock networks (RCLKs), and periphery clock networks (PCLKs). These clocks are organized into a hierarchical clock structure that provides up to 192 unique clock domains (16 GCLK + 88 RCLK + 88 PCLK) within the HardCopy III device and allows up to 60 unique GCLK/RCLK/PCLK clock sources (16 GCLK + 22 RCLK + 22 PCLK) per device quadrant.


HardCopy III devices deliver abundant PLL resources, with up to 12 PLLs per device and up to 10 outputs per PLL. You can configure each output independently, creating a unique, customizable clock frequency with no fixed relation to any other input or output clock. Inherent jitter filtration and fine granularity control over multiply, divide ratios, and dynamic phase-shift reconfiguration provide the high-performance precision required in today's high-speed applications. HardCopy III PLLs are feature-rich, supporting advanced capabilities such as clock switchover, reconfigurable phase shift, PLL reconfiguration, and reconfigurable bandwidth. You can use PLLs for general-purpose clock management, supporting multiplication, phase shifting, and programmable duty cycles. HardCopy III PLLs also support external feedback mode, spread-spectrum input clock tracking, and post-scale counter cascading.

-  For more information about clock networks and PLLs, refer to the *Clock Networks and PLLs in HardCopy III Devices* chapter.

I/O Banks and I/O Structure

HardCopy III devices contain up to 20 modular I/O banks, each containing 24, 32, 40, or 48 I/Os (not including dedicated clock inputs). The left- and right-side I/O banks contain circuitry to support external memory interfaces and high-speed differential I/O interfaces capable of performance at up to 1.25 Gbps. The top and bottom I/O banks also contain circuitry to support external memory interfaces.

HardCopy III devices support a wide range of industry I/O standards, including single-ended, voltage referenced single-ended, and differential I/O standards. The HardCopy III I/O supports bus hold, pull-up resistor, slew rate, output delay control, and open-drain output. HardCopy III devices also support on-chip series (R_S) and on-chip parallel (R_T) termination with auto calibration for single-ended I/O standards. The left and right I/O banks support on-chip differential termination (R_D) to meet LVDS I/O standards. Bidirectional I/O pins on all I/O banks also support Dynamic OCT.


-  For more information about I/O features, refer to the *HardCopy III Device I/O Features* chapter.

External Memory Interfaces

The HardCopy III I/O structure is equivalent to the Stratix III I/O structure, providing high-performance support for existing and emerging external memory standards such as DDR, DDR2, DDR3, QDR II, QDR II+, and RLDRAM II.

Packed with features such as dynamic on-chip termination, trace mismatch compensation, read and write leveling, half-rate registers, and 4- to 36-bit DQ group widths, HardCopy III I/Os supply the built-in functionality required for rapid and robust implementation of external memory interfaces. Double data-rate support is found on all sides of the HardCopy III device. HardCopy III devices provide an efficient architecture to quickly and easily fit wide external memory interfaces precisely.

A self-calibrating soft IP core (ALTMEMPHY) optimized to take advantage of HardCopy III device I/Os along with the Quartus II timing analysis tool (the TimeQuest Timing Analyzer) provides the total solution for the highest reliable frequency of operation across process, voltage, and temperature (PVT).

-  For more information about external memory interfaces, refer to the *External Memory Interfaces in HardCopy III Devices* chapter.

High-Speed Differential I/O Interfaces with DPA

HardCopy III devices contain dedicated circuitry for supporting differential standards at speeds up to 1.25 Gbps. High-speed differential I/O circuitry supports the following high-speed I/O interconnect standards and applications:


- Utopia IV
- SPI-4.2

- SFI-4
- 10 Gigabit Ethernet XSLI
- Rapid I/O
- NPSI

HardCopy III devices support 2×, 4×, 6×, 7×, 8×, and 10× SERDES modes for high-speed differential I/O interfaces, and 4×, 6×, 7×, 8×, and 10× SERDES modes when using the dedicated DPA circuitry. DPA minimizes bit errors, simplifies PCB layout and timing management for high-speed data transfer, and eliminates channel-to-channel and channel-to-clock skews in high-speed data transmission systems. The Stratix III soft CDR function can also be implemented using HCells in HardCopy III devices, enabling low-cost 1.25-Gbps clock-embedded serial links.

HardCopy III devices have the following dedicated circuitry for high-speed differential I/O support:


- Differential I/O buffer
- Transmitter serializer
- Receiver deserializer
- Data realignment
- Dynamic phase aligner (DPA)
- Soft CDR functionality
- Synchronizer (FIFO buffer)
- PLLs


 For more information about dedicated circuitry for high-speed differential support, refer to the *High Speed Differential I/O Interfaces with DPA in HardCopy III Devices* chapter.

Hot Socketing and Power-On Reset

HardCopy III devices offer hot socketing, which is also known as hot plug-in or hot swap, and power sequencing support without the use of any external devices. On-chip hot socketing and power-sequencing support ensures proper device operation independent of the power-up sequence. You can insert or remove a HardCopy III board during system operation without causing undesirable effects to the running system bus or the board itself.


The hot socketing feature also makes it easier to use HardCopy III devices on PCBs that contain a mixture of 3.0-V, 2.5-V, 1.8-V, 1.5-V, and 1.2-V devices. With the HardCopy III hot socketing feature, you do not need to ensure a proper power-up sequence for each device on the board.

 HardCopy III devices have a maximum V_{CCIO} voltage of 3.0 V, but can tolerate a 3.3-V input level.

 For more information about hot socketing, refer to the *Hot Socketing and Power-On Reset in HardCopy III Devices* chapter.

IEEE 1149.1 (JTAG) Boundary Scan Testing


HardCopy III devices support the JTAG IEEE Std. 1149.1 specification. The Boundary-Scan Test (BST) architecture offers the capability to both test pin connections without using physical test probes and capture functional data while a device is operating normally. Boundary-scan cells in the HardCopy III device can force signals onto pins or capture data from the pin or core signals. Forced test data is serially shifted into the boundary-scan cells. Captured data is serially shifted out and externally compared to expected results.


 For more information about JTAG, refer to the [IEEE 1149.1 \(JTAG\) Boundary Scan Testing in HardCopy III Devices](#) chapter.

Signal Integrity

HardCopy III devices simplify the challenge of maintaining signal integrity through a number of chip-, package-, and board-level enhancements to enable efficient high-speed data transfer into and out of the device. These enhancements include:

- 8:1:1 user I/O/GND/ V_{CC} ratio to reduce loop inductance in the package
- Dedicated power supply for each I/O bank, with an I/O limit of 24 to 48 I/Os per bank to help limit simultaneous switching noise (SSN)
- Slew-rate support with up to four settings to match the desired I/O standard, control noise, and overshoot
- Output-current drive strength support with up to four settings to match desired I/O standard performance
- Output-delay support to control rise and fall times and adjust duty cycle, compensate for skew, and reduce simultaneous switching output (SSO) noise
- Dynamic OCT with auto-calibration support for series and parallel OCT and differential OCT support for LVDS I/O standard on the left and right banks

 The supported settings for slew-rate control, output-current drive strength, and output-delay control are mask-programmed into the HardCopy III devices and cannot be changed after the silicon is fabricated.


 For more information about signal integrity support in the Quartus II software, refer to the [Quartus II Handbook](#).

Software Support and Part Number Information

This section describes HardCopy III device software support and part number information.

Software Support

HardCopy III devices are supported by the Altera Quartus II design software, which provides a comprehensive environment for system-on-chip (SOC) design. The Quartus II software includes HDL and schematic design entry, compilation and logic synthesis, full simulation and advanced timing analysis, SignalTap™ II logic analyzer, and device configuration.

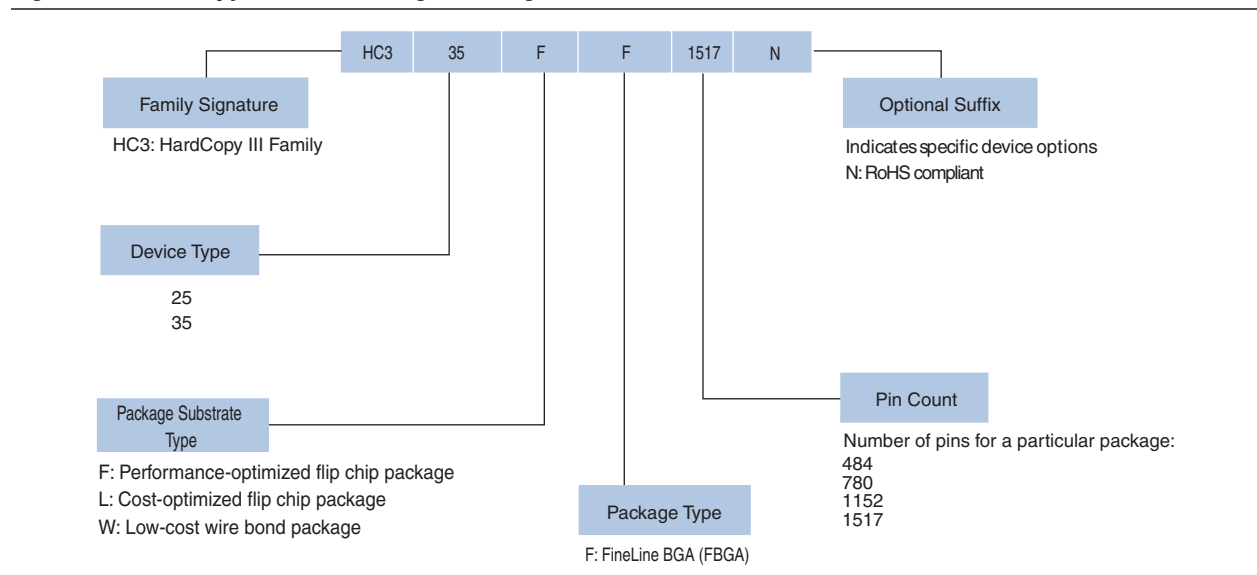
 For more information about the Quartus II software features, refer to the *Quartus II Handbook*.


The Quartus II software supports the Windows and Linux Red Hat operating systems. You can obtain the specific operating system for the Quartus II software from the Quartus II Readme.txt file or <http://www.altera.com/download/os-support/oss-index.html>. The Quartus II software also supports seamless integration with industry-leading EDA tools through the NativeLink interface.

Part Number Information

Figure 1-1 shows the generic part number for HardCopy III devices.

Figure 1-1. HardCopy III Device Package Ordering Information



 For more information about a specific package, refer to the *HardCopy III Device Package Information* chapter.

Document Revision History

Table 1-6 lists the revision history for this chapter.

Table 1-6. Document Revision History

Date	Version	Changes
January 2011	3.2	<ul style="list-style-type: none"> ■ Updated Table 1-1, Table 1-2, and Table 1-3. ■ Updated Figure 1-1. ■ Used new document template. ■ Updated “HardCopy III ASIC and Stratix III FPGA Mapping Paths” on page 1-4. ■ Added “HardCopy III Package Pro” on page 1-7. ■ Made minor text edits.
July 2009	3.1	Updated “Features” on page 1-2.
June 2009	3.0	<ul style="list-style-type: none"> ■ Updated Table 1-3, Table 1-6, and Table 1-9 to include non-socket replacement devices. ■ Updated Figure 1-2.
December 2008	2.0	Edits to Table 1-1.
May 2008	1.0	Initial release.

