2. Logic Array Block and Adaptive Logic Module Implementation in HardCopy III Devices

HIII51002-2.1

This chapter describes how the Stratix® III's logic array blocks (LABs) and memory logic array blocks (MLABs) are implemented in a HardCopy® III device.

In Stratix III devices, the core fabric consists of an array of LABs and MLABs. LABs and MLABs are composed of adaptive logic modules (ALMs) that are configurable and can implement various logic, arithmetic, and register functions of a customer design. In addition, MLABs can implement memory functions.

By comparison, the core fabric in HardCopy III devices are built using an array of flexible, fine-grain architecture blocks called HCells that can efficiently implement all the functionality of the ALMs, LABs, and MLABs. HardCopy III devices offer improved performance and significant static power savings compared to Stratix III FPGA prototype devices because only the HCells required to implement the customer design are used, while the unused HCells are powered down.

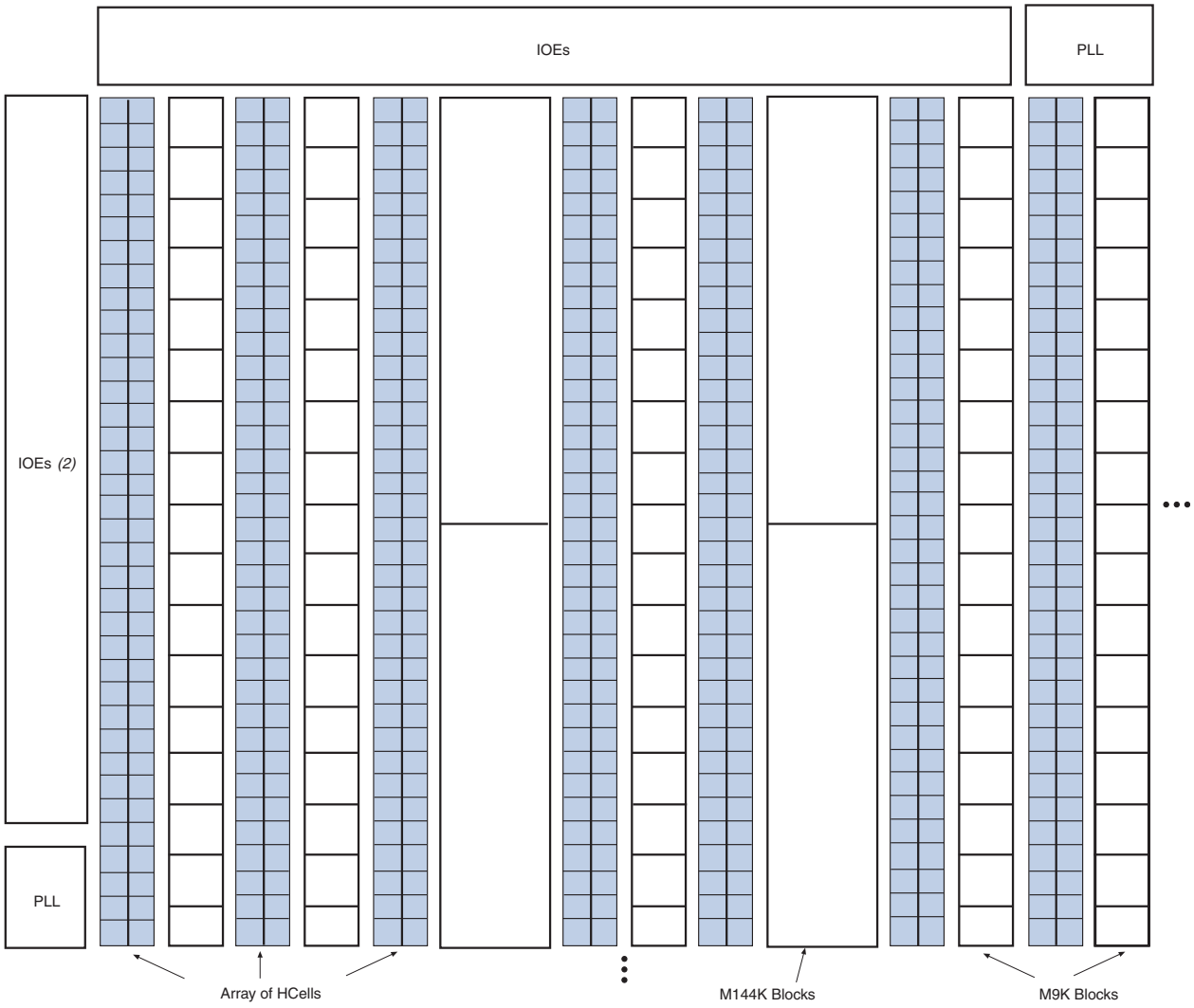
For more information about ALMs, LABs, and MLABs, refer to the *Logic Array Blocks and Adaptive Logic Modules in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

This chapter contains the following sections:

HCells

HCells are a collection of logic transistors based on 0.9-V, 40-nm process technology. The construction of logic using HCells allows flexible functionality such that when HCells are combined, all viable logic combinations of Stratix III functionality are replicated. These HCells constitute the array of the HCell area, as shown in Figure 2–1. Only the HCells needed to implement the design are assembled together, which optimizes HCell use. The unused area of the HCell logic fabric is powered down, resulting in significant static power savings compared with the Stratix III FPGA prototype.

Figure 2–1. Example Block Diagram of HardCopy III Device ***(Note 1)***



Notes to Figure 2–1:

(1) Figure 2–1 shows a graphical representation of the device floorplan. A detailed floorplan is available in the Quartus® II software.

(2) IOEs represents I/O elements.

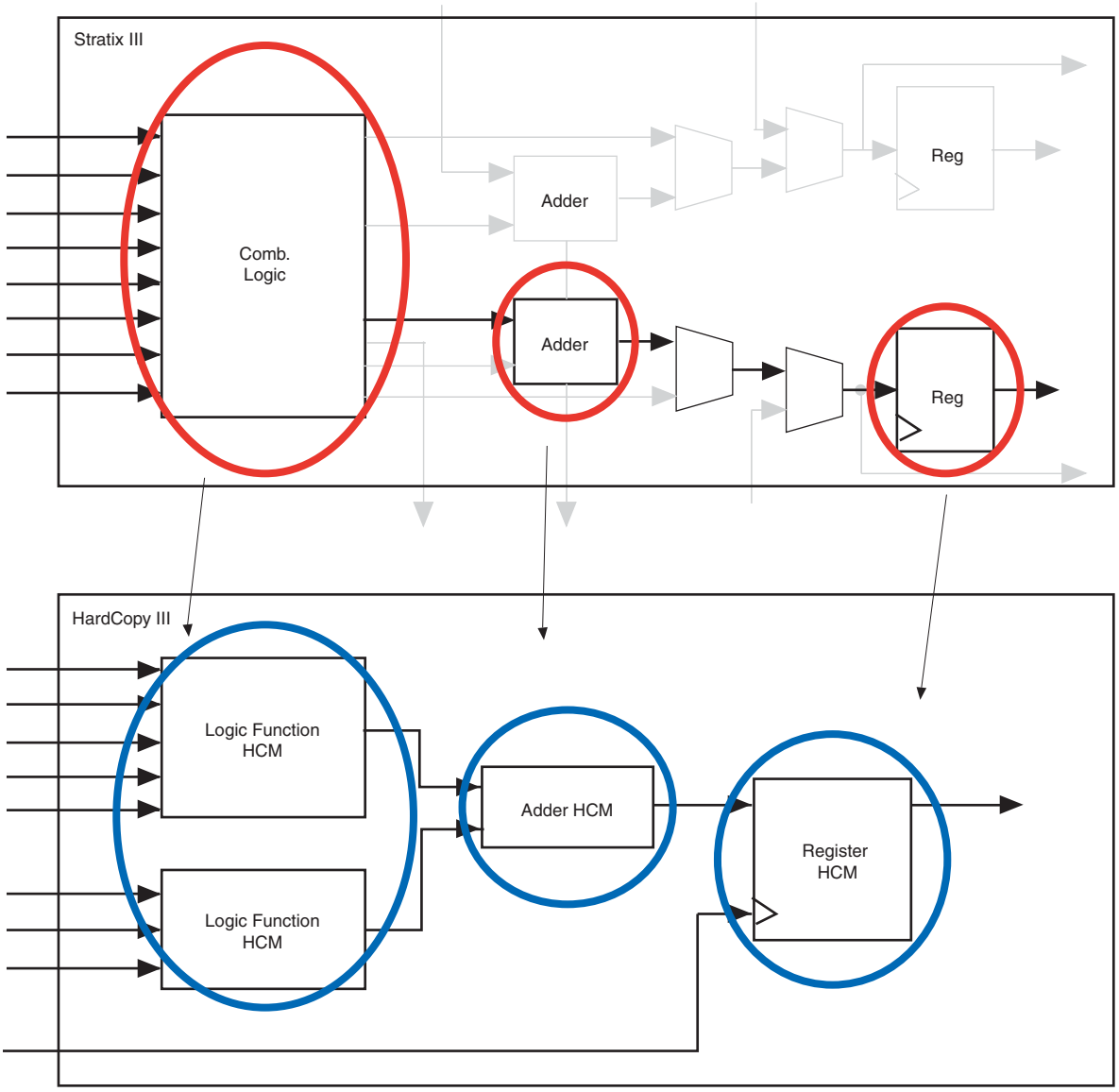
ALM and LAB Function Implementation

The Quartus II software uses a library of pre-characterized HCell macros (HCMs) to place Stratix III ALM configurations into the HardCopy III HCell-based logic fabric. An HCell macro defines how a group of HCells connect within the array. HCell macros can construct all combinations of combinational logic, adder, and register functions that can be implemented by a Stratix III ALM. You can use HCells that are not used for ALM configurations to implement MLAB and DSP block functions.

For more details about implementing DSP block functions using HCells, refer to the *DSP Block Implementation in HardCopy III Devices* chapter.

Based on design requirements, the Quartus II software chooses the appropriate HCell macros to implement design functionality. For example, Stratix III ALMs offer flexible look-up table (LUT) blocks, registers, arithmetic blocks, and LAB-wide control signals. In HardCopy III devices, if your design requires these architectural elements, the Quartus II synthesis tool maps the design to the appropriate HCell macros, resulting in improved design performance compared to the Stratix III FPGA prototype, as shown in Figure 2–2.

Figure 2–2. Example of ALM Functions Mapped to HCell Macros



MLAB Function Implementation

In Stratix III devices, the MLAB is a LAB derivative that you can configure to support up to a maximum of 640 bits of simple dual-port static random access memory (SRAM). Similar to the LAB, each MLAB consists of ten ALMs and can implement all the functionality of the LAB in addition to the memory function. In HardCopy III devices, the MLAB functions are mapped to HCell macros that provide the same memory functionality.

For more information about memory implementation using MLABs, refer to the *TriMatrix Embedded Memory Blocks in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

For more information about HardCopy III memory support, refer to the *TriMatrix Embedded Memory Blocks in HardCopy III Devices* chapter.

In HardCopy III devices, the basic building block of the core array is the HCell. HCells are connected together to form HCell macros that can implement all the functionality of the ALMs, LABs, and MLABs in the Stratix III devices. Only HCells required to implement the design are used, while unused HCells are powered down. This allows the core fabric to be efficiently used and offers significant static power savings compared to the Stratix III FPGA prototype devices.

Document Revision History

Table 2–1 shows the revision history for this chapter.

Table 2–1. Document Revision History

Date	Version	Changes Made
January 2011	2.1	■ Maintenance release—used new document template. ■ Minor text edits.
December 2008	2.0	Added Introductory paragraph.
May 2008	1.0	Initial release.