4. TriMatrix Embedded Memory Blocks in HardCopy III Devices

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This chapter describes TriMatrix memory blocks, modes, features, and design considerations in HardCopy® III devices.

HardCopy III devices offer TriMatrix embedded memory blocks to efficiently address the needs of ASIC designs. TriMatrix memory comes in three different sizes and includes 640-bit memory logic array blocks (MLABs), 9-Kbit M9K blocks, and 144-Kbit M144K blocks. The MLABs have been optimized to implement filter delay lines, small FIFO buffers, and shift registers. You can use the M9K blocks for general purpose memory applications; you can use the M144K blocks for processor code storage, packet buffering, and video frame buffering.

TriMatrix memory in HardCopy III devices support the same memory functions and features as Stratix® III devices. You can independently configure each embedded memory block to be a single- or dual-port RAM, FIFO, ROM, or shift register using the MegaWizard™ Plug-in Manager in the Quartus® II software. You can stitch together multiple blocks of the same type to produce larger memories with minimal timing penalty. TriMatrix memory provides up to 16,272 Kbits of dedicated embedded static random access memory (SRAM).

This chapter contains the following sections:

Memory Resources and Features

HardCopy III embedded memory consists of MLAB, M9K, and M144K memory blocks and has a one-to-one mapping from Stratix III memory. However, the number of available memory blocks differs based on density, package, and the Stratix III device-to-HardCopy III ASIC mapping paths, as shown in Table 4–1.

Table 4–1. Embedded Memory Resources for HardCopy III Devices (Part 1 of 2) *(Note 1)*, *(2)*

HardCopy III ASIC	Stratix III FPGA Prototype	M9K Blocks *(3)*	M144K Blocks *(3)*	Total Dedicated RAM Bits (not including MLABs)
HC325	EP3SL110	275	12	4,203 Kb
	EP3SL150	355	16	5,499 Kb
	EP3SE110	639	16	8,055 Kb
	EP3SL200	468	32	8,820 Kb
	EP3SE260	864	32	12,384 Kb
	EP3SL340	864	32	12,384 Kb

Table 4–1. Embedded Memory Resources for HardCopy III Devices (Part 2 of 2) *(Note 1), (2)*

HardCopy III ASIC	Stratix III FPGA Prototype	M9K Blocks *(3)*	M144K Blocks *(3)*	Total Dedicated RAM Bits (not including MLABs)
HC335	EP3SL150	355	16	5,499 Kb
	EP3SE110	639	16	8,055 Kb
	EP3SL200	468	36	9,396 Kb
	EP3SE260	864	48	14,688 Kb
	EP3SL340	1,040	48	16,272 Kb

Notes to Table 4–1:

(1) In addition to device resource usage, Stratix III packages also determine the optimal HardCopy III device mapping path. For example, the EP3SL150 device comes in F780 and F1152 packages. The mapping paths for the F780 and F1152 packages are the HC325 and HC335 devices, respectively.

(2) HardCopy III devices do not have dedicated MLAB blocks but can support the same Stratix III MLAB functionality. The number of MLABs that are supported in HardCopy III devices varies depending on resource usage and the Stratix III device to HardCopy III device mapping path.

(3) The M9K and M144K blocks may lock up if there is a glitch in the clock source when rden equals 1. For more information and the workaround solution, refer to *M9K and M144K RAM Block Lockup Issue* in the *Stratix III Device Family Errata Sheet*.

With regards to functionality, memory in HardCopy III devices and Stratix III devices is identical. The memory blocks can implement various types of memory with or without parity, including true dual-port, simple dual-port, and single-port RAM, ROM, and FIFO. Table 4–2 lists the size and features of the different memory blocks. In addition, unused memory blocks in HardCopy III devices are powered down, allowing the HardCopy III devices to have significant power savings.

Table 4–2. Embedded Memory Features for HardCopy III Devices (Part 1 of 2) *(1)*

Feature	MLABs	M9K Blocks	M144K Blocks
Maximum performance	TBD	TBD	TBD
Total RAM bits (including parity bits)	640	9,216	147,456
Configurations (depth × width)	16 × 8 16 × 9 16 × 10 16 × 16 16 × 18 16 × 20 *(1)*	8K × 1 4K × 2 2K × 4 1K × 8 1K × 9 512 × 16 512 × 18 256 × 32 256 × 36	16K × 8 16K × 9 8K × 16 8K × 18 4K × 32 4K × 36 2K × 64 2K × 72
Parity bits	✓	✓	✓
Byte enable	✓	✓	✓
Packed mode	—	✓	✓
Address clock enable	✓	✓	✓
Single-port memory	✓	✓	✓
Simple dual-port memory	✓	✓	✓
True dual-port memory	—	✓	✓
Embedded shift register	✓	✓	✓
ROM *(2)*	✓	✓	✓

Table 4–2. Embedded Memory Features for HardCopy III Devices (Part 2 of 2) *(1)*

Feature	MLABs	M9K Blocks	M144K Blocks
FIFO buffer	✓	✓	✓
Simple dual-port mixed width support	—	✓	✓
True dual-port mixed width support	—	✓	✓
Memory initialization file (**.mif**)	Not supported, except in ROM mode	Not supported, except in ROM mode	Not supported, except in ROM mode
Mixed-clock mode	✓	✓	✓
Power-up condition	Outputs cleared if registered. *(3)*	Outputs cleared if registered. *(4)*	Outputs cleared if registered. *(4)*
Register clears	Outputs cleared	Outputs cleared	Outputs cleared
Write and Read operation triggering	Write: Falling clock edges Read: Rising clock edges	Write and Read: Rising clock edges	Write and Read: Rising clock edges
Same-port read-during-write	Outputs set to old data or don't care	Outputs set to old or new data	Outputs set to old or new data
Mixed-port read-during-write	Outputs set to don't care	Outputs set to old data	Outputs set to old data
ECC Support	Soft IP support using the Quartus II software	Soft IP support using the Quartus II software	Built-in support in ×64-wide SDP mode or soft IP support using the Quartus II software

Notes to Table 4–2:

(1) Violating the setup and hold time on the memory block address registers could corrupt the memory contents. This applies to both read and write operations.

(2) In ROM mode, MLABs support the (depth × width) configurations of 64 × 8, 64 × 9, 64 × 10, 32 × 16, 32 × 18, or 32 × 20.

(3) The contents for MLAB in RAM mode are initialized to zero on power-up.

(4) The contents for the M9K and M144K blocks power up randomly, so reads after power up are not valid.

For more information about embedded memory support in Stratix III devices, refer to the *TriMatrix Embedded Memory Blocks in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

CAUTION

When using the memory block in ROM, single-port, simple dual-port, or true dual port mode, you can corrupt the memory contents if you violate the setup or hold time on any of the memory block input registers. This applies to both read and write operations.

MLAB Implementation

While the M9K and M144K memory blocks are dedicated resources that function the same in Stratix III and HardCopy III devices, the MLABs are implemented differently in the two device families. In Stratix III devices, the MLABs are dedicated blocks that you can configure for regular logic functions or memory functions. In HardCopy III devices, the MLAB memory blocks are implemented using HCells. HCells are a collection of logic transistors connected together to form HCell macros (HCMs). The Quartus II software maps the Stratix III MLAB function to the appropriate memory HCell macro that preserves the memory function. This allows the HardCopy III core fabric to be used more efficiently, freeing up unused HCells for adaptive logic module (ALM) or digital signal processing (DSP) functions.

For more information about HCells in HardCopy III devices, refer to the *Logic Array Block and Adaptive Logic Module Implementation in HardCopy III Devices* chapter.

Design Considerations

Unlike Stratix III devices, HardCopy III devices do not have device configuration, so memories that are configured as RAM power up with random content. Therefore, the memory block contents cannot be pre-loaded or initialized with a memory initialization file (**.mif**) in HardCopy III devices. You must ensure that your Stratix III design does not require **.mif**s if you use the memory blocks as RAM. However, if you use the memory blocks as ROM, they are mask programmed to the design's ROM contents.

You can use the ALTMEM_INIT megafunction to initialize the RAM after power up for HardCopy III devices. This megafunction reads from an internal ROM (inside the megafunction) or an external ROM (on chip or off chip) and writes to the RAM after power up.

When using non-registered output mode for the HardCopy III MLAB memory blocks, the outputs power up with memory content. When using registered output mode for these memory blocks, the outputs are cleared on power up. You must take this into consideration when designing logic that might evaluate the initial power up values of the MLAB memory block.

Document Revision History

Table 4–3 lists the revision history for this chapter.

Table 4–3. Document Revision History

Date	Version	Changes
January 2011	3.1	■ Update Table 4–1 and Table 4–2. ■ Updated the "Memory Resources and Features" section. ■ Minor text edits.
June 2009	3.0	■ Updated Table 4–1. ■ Minor text edits. ■ Removed the Conclusion and Referenced Documents sections.
December 2008	2.0	■ Updated Table 4–1. ■ Made minor editorial changes.
May 2008	1.0	Initial release.