

This chapter describes the I/O standards, features, termination schemes, and performance supported in HardCopy® III devices. All HardCopy III devices have configurable high-performance I/O drivers and receivers supporting a wide range of industry standard interfaces. Both the top/bottom (column) and left/right (row) I/O banks of HardCopy III devices support the same I/O standards with different performance specifications.

This chapter includes the following sections:

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Numerous I/O features assist in the high-speed data transfer into and out of the HardCopy device.

HardCopy III devices support the following I/O standards:

- Single-ended, non-voltage-referenced or voltage-referenced I/O standards
- Low-voltage differential signaling (LVDS)
- Reduced swing differential signal (RSDS)
- Mini-LVDS
- High-speed transceiver logic (HSTL)
- Stub series terminated logic (SSTL)
- Single data rate (SDR) and half data rate (HDR—half the frequency and twice the data width of SDR) input and output options
- Up to 88 full duplex 1.25 Gbps true LVDS channels (88 Tx + 88 Rx) on the row I/O banks

Features supported in a single-ended I/O interface include:

- De-skew, read and write leveling, and clock-domain crossing functionality
- Multiple output current strength setting for different I/O standards

- Four slew rate settings
- Four output delay settings
- Six I/O delay settings
- Optional bus-hold
- Optional pull-up resistor
- Optional open-drain output
- Serial, parallel, and dynamic on-chip termination (OCT)

Features supported in a high-speed memory interface include:

- Dedicated DQ strobe (DQS) logic in both column and row I/Os
- Each I/O bank is accessible by two delay-locked loops (DLLs) that have different frequencies and phase shifts
- Low-power option when you do not use the memory interface

Features supported in a high-speed differential I/O interface include:

- Four slew rate settings
- Differential OCT
- Hard dynamic phase alignment (DPA) block with serializer/deserializer (SERDES)
- Four pre-emphasis settings
- Four differential output voltage (V_{OD}) settings

Differences Between HardCopy III ASICs and Stratix III FPGAs

Both HardCopy III and Stratix[®] III devices support the same speed, performance, I/O standards and implementation guidelines, except I/O standards that require 3.3-V in Stratix III devices. You can prototype I/O interfaces with Stratix III devices and map the design to HardCopy III devices. HardCopy III devices do not support 3.3-V V_{CCIO} due to the device reliability of 40nm process technology. However, HardCopy III devices can interface with a 3.3 V interface. Refer to the section [“3.3/3.0-V I/O Interface” on page 6–10](#) for more information.

You must set the HardCopy III companion device for your Stratix III design project in the Quartus[®] II software. Otherwise, you may not be able to map to a HardCopy III device due to varying amounts of resource availability. There are four major differences between HardCopy III and Stratix III families:


- Unlike Stratix III devices, HardCopy III devices require external voltage regulators to regulate V_{CCIO} power from 3.3 V to 3 V for device reliability.
- There are up to eight calibration blocks in HardCopy III devices instead of up to ten calibration blocks in Stratix III devices.
- Stratix III devices support up to 24 I/O banks while HardCopy III devices support up to 20 I/O banks.

Stratix III and HardCopy III devices support different I/O counts per bank. Therefore, always set the HardCopy III companion device for your Stratix III design project in the Quartus II software. For more information, refer to [Table 6-2](#).

Certain HardCopy III densities may have their speed and timing performance affected when compared with their companion FPGA due to the differences in the architectural layout of the PLLs and I/O pins:

- I/O pin overhang—refers to some of the vertical I/Os that are located sufficiently away from the HCell core and RAM blocks. This can result in a larger skew when compared with an I/O placed next to the HCell or RAM block. For more information, refer to [Figure 6-1](#), [Figure 6-2](#), and [Table 6-1](#).
- I/O pin adjacent to the PLL—Some HardCopy III devices have the PLL placed in the core when compared with their companion FPGA, which may have the PLL located in the periphery. In this instance, when using I/Os adjacent to the PLLs in the HardCopy III device, if the source/destination in the HCell is blocked by the PLL, a larger skew may result when compared with the I/Os not located next to the HCell or RAM block.

I/O pin overhang and I/O pin adjacent to the PLL can cause different skew results and timing performance between the FPGA and the HardCopy III device.

 If your HardCopy III device design has timing closure challenges containing a wide parallel interface with a very tight skew budget, consider avoiding these I/O pins. Instead, use these I/O pins for a slower data rate or as controls.

When migrating from the FPGA to the HardCopy III device, use the Chip Planner in both the FPGA and the HardCopy III device to plan with these I/Os.

[Figure 6-1](#) and [Figure 6-2](#) show the locations of the I/O pin overhang and I/O pin adjacent to the PLL. Use the Chip Planner in the Quartus II software to obtain a more accurate layout of these I/Os.

Figure 6-1. HC325 Devices Not Affected by I/O Pin Overhang and PLL Obstruction

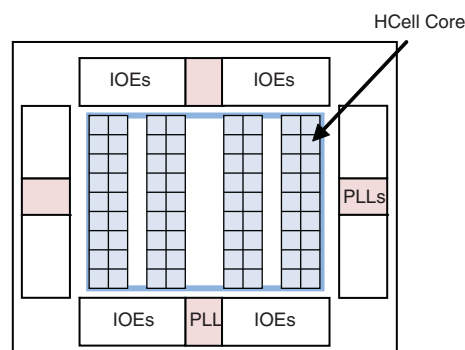


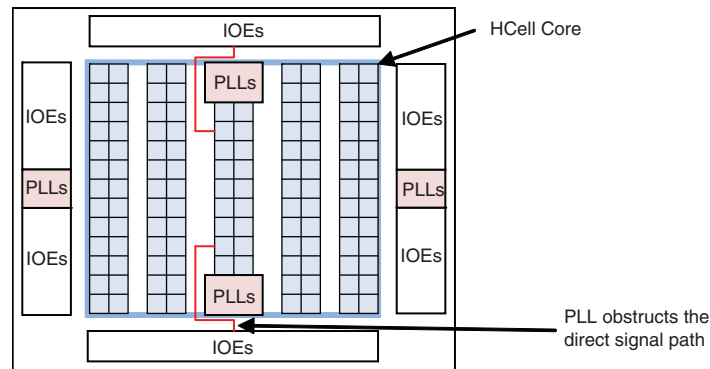
Figure 6–2. HC335 Devices Have a PLL Obstruction Issue for the Top and Bottom I/Os

Table 6–1 lists the HardCopy III devices that may be affected by architectural differences in your I/O pin layouts.

Table 6–1. I/O Pin Layout for HardCopy III Devices

I/O Pin Layout Differences	Devices Affected
Not affected	HC325FF484, HC325FF780, HC325WF484, and HC325WF780
VIO overhang	None
I/O pins adjacent to the PLL	HC335FF1152, HC335LF1152, HC335FF1517, and HC335LF1517

I/O Standards and Voltage Levels

HardCopy III devices support a wide range of industry I/O standards, including single-ended, voltage-referenced single-ended, and differential I/O standards.

Table 6–2 lists the supported I/O standards and the typical values for input and output V_{CCIO} , V_{CCPD} , V_{REF} , and board V_{TT} .

Table 6–2. I/O Standards and Voltage Levels HardCopy III Devices (Part 1 of 3) (Note 1)

I/O Standard	Standard Support	$V_{CCIO}(V)$				$V_{CCPD}(V)$ (Pre-Driver Voltage)	$V_{REF}(V)$ (Input Ref Voltage)	$V_{TT}(V)$ (Board Termination Voltage)
		Input Operation		Output Operation				
		Column I/O Banks	Row I/O Banks	Column I/O Banks	Row I/O Banks			
3.0-V LVTTTL	JESD8-B	3.0/2.5	3.0/2.5	3.0	3.0	3.0	—	—
3.0-V LVCMOS	JESD8-B	3.0/2.5	3.0/2.5	3.0	3.0	3.0	—	—
2.5-V LVTTTL/LVCMOS	JESD8-5	3.0/2.5	3.0/2.5	2.5	2.5	2.5	—	—
1.8-V LVTTTL/LVCMOS	JESD8-7	1.8/1.5	1.8/1.5	1.8	1.8	2.5	—	—
1.5-V LVTTTL/LVCMOS	JESD8-11	1.8/1.5	1.8/1.5	1.5	1.5	2.5	—	—
1.2-V LVTTTL/LVCMOS	JESD8-12	1.2	1.2	1.2	1.2	2.5	—	—
3.0-V PCI (4)	PCI Rev 2.2	3.0	3.0	3.0	3.0	3.0	—	—
3.0-V PCI-X (4)	PCI-X Rev 1.0	3.0	3.0	3.0	3.0	3.0	—	—

Table 6-2. I/O Standards and Voltage Levels HardCopy III Devices (Part 2 of 3) (Note 1)


I/O Standard	Standard Support	$V_{CCIO}(V)$				$V_{CCPD}(V)$ (Pre-Driver Voltage)	$V_{REF}(V)$ (Input Ref Voltage)	$V_{TT}(V)$ (Board Termination Voltage)
		Input Operation		Output Operation				
		Column I/O Banks	Row I/O Banks	Column I/O Banks	Row I/O Banks			
SSTL-2 Class I	JESD8-9B	(2)	(2)	2.5	2.5	2.5	1.25	1.25
SSTL-2 Class II	JESD8-9B	(2)	(2)	2.5	2.5	2.5	1.25	1.25
SSTL-18 Class I	JESD8-15	(2)	(2)	1.8	1.8	2.5	0.90	0.90
SSTL-18 Class II	JESD8-15	(2)	(2)	1.8	1.8	2.5	0.90	0.90
SSTL-15 Class I	—	(2)	(2)	1.5	1.5	2.5	0.75	0.75
SSTL-15 Class II (3)	—	(2)	(2)	1.5	—	2.5	0.75	0.75
HSTL-18 Class I	JESD8-6	(2)	(2)	1.8	1.8	2.5	0.90	0.90
HSTL-18 Class II	JESD8-6	(2)	(2)	1.8	1.8	2.5	0.90	0.90
HSTL-15 Class I	JESD8-6	(2)	(2)	1.5	1.5	2.5	0.75	0.75
HSTL-15 Class II (3)	JESD8-6	(2)	(2)	1.5	—	2.5	0.75	0.75
HSTL-12 Class I	JESD8-16A	(2)	(2)	1.2	1.2	2.5	0.6	0.6
HSTL-12 Class II (3)	JESD8-16A	(2)	(2)	1.2	—	2.5	0.6	0.6
Differential SSTL-2 Class I	JESD8-9B	(2)	(2)	2.5	2.5	2.5	—	1.25
Differential SSTL-2 Class II	JESD8-9B	(2)	(2)	2.5	2.5	2.5	—	1.25
Differential SSTL-18 Class I	JESD8-15	(2)	(2)	1.8	1.8	2.5	—	0.90
Differential SSTL-18 Class II	JESD8-15	(2)	(2)	1.8	1.8	2.5	—	0.90
Differential SSTL-15 Class I	—	(2)	(2)	1.5	1.5	2.5	—	0.75
Differential SSTL-15 Class II	—	(2)	(2)	1.5	—	2.5	—	0.75
Differential HSTL-18 Class I	JESD8-6	(2)	(2)	1.8	1.8	2.5	—	0.90
Differential HSTL-18 Class II	JESD8-6	(2)	(2)	1.8	1.8	2.5	—	0.90
Differential HSTL-15 Class I	JESD8-6	(2)	(2)	1.5	1.5	2.5	—	0.75
Differential HSTL-15 Class II	JESD8-6	(2)	(2)	1.5	—	2.5	—	0.75
Differential HSTL-12 Class I	JESD8-16A	(2)	(2)	1.2	1.2	2.5	—	0.60
Differential HSTL-12 Class II	JESD8-16A	(2)	(2)	1.2	—	2.5	—	0.60
LVDS (6)	ANSI/TIA/EIA-644	(2)	(2)	2.5	2.5	2.5	—	—
RSDS (7), (8)	—	(2)	(2)	2.5	2.5	2.5	—	—

Table 6-2. I/O Standards and Voltage Levels HardCopy III Devices (Part 3 of 3) (Note 1)

I/O Standard	Standard Support	$V_{CCIO}(V)$				$V_{CCPD}(V)$ (Pre-Driver Voltage)	$V_{REF}(V)$ (Input Ref Voltage)	$V_{TT}(V)$ (Board Termination Voltage)
		Input Operation		Output Operation				
		Column I/O Banks	Row I/O Banks	Column I/O Banks	Row I/O Banks			
mini-LVDS (7), (8)	—	(2)	(2)	2.5	2.5	2.5	—	—
LVPECL	—	(5)	2.5	—	—	2.5	—	—

Notes to Table 6-2:

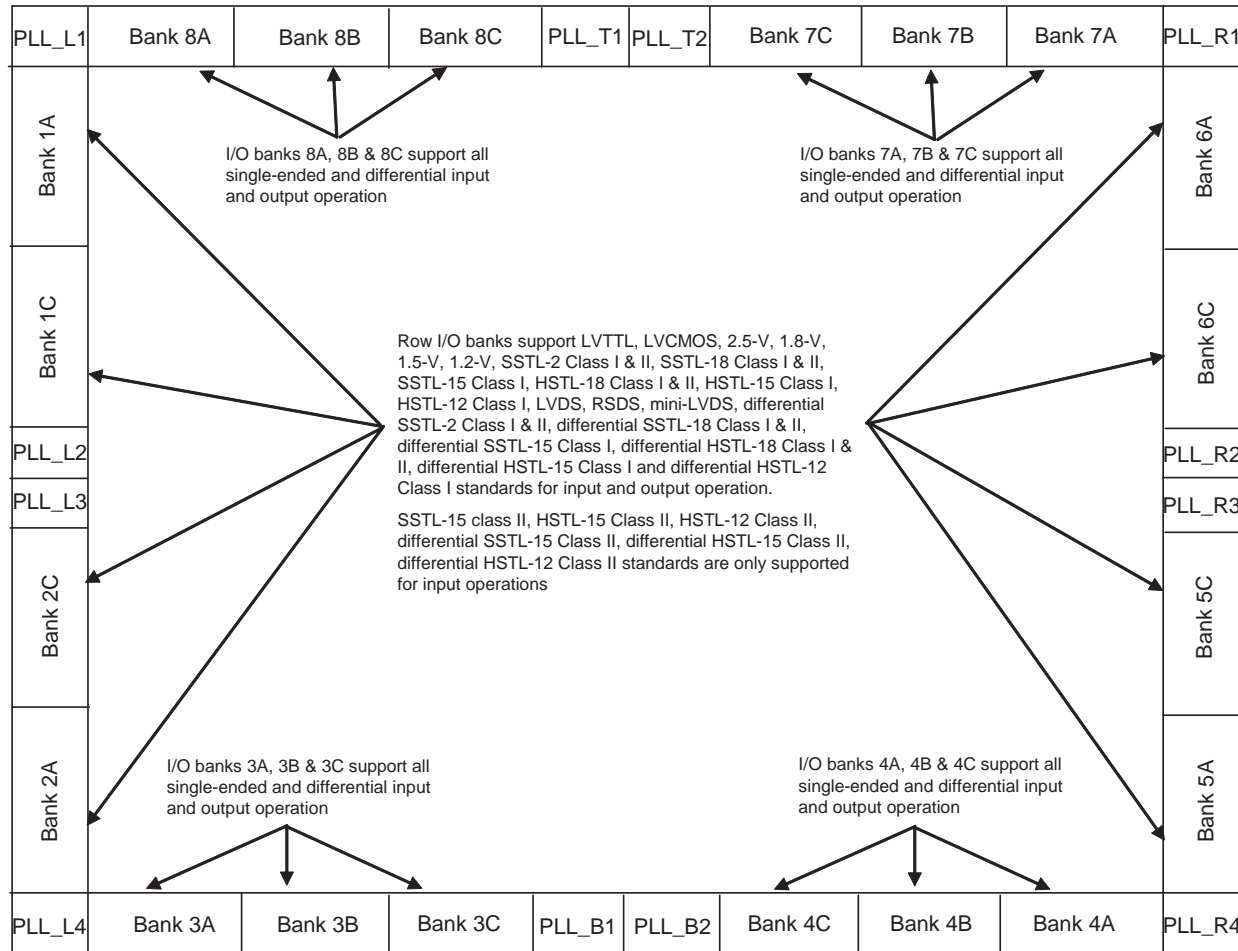
- (1) HardCopy III devices do not support the 3.3-V I/O standard. V_{CCPD} is either 2.5 V or 3.0 V. For a 3.0-V I/O standard, $V_{CCPD} = 3.0$ V. For 2.5 V and below I/O standards, $V_{CCPD} = 2.5$ V. However, HardCopy III devices can interface with a 3.3 V interface. For more information, refer to the section “3.3/3.0-V I/O Interface” on page 6-10.
- (2) Single-ended HSTL/SSTL, differential SSTL/HSTL, and LVDS input buffers are powered by V_{CCPD} . Row I/O banks support both true differential input buffers and true differential output buffers. Column I/O banks support true differential input buffers, but not true differential output buffers. I/O pins are organized in pairs to support differential standards. Column I/O differential HSTL and SSTL inputs use LVDS differential input buffers without on-chip RD support.
- (3) Row I/Os do not support HSTL-12 Class II output, HSTL-15 Class II output, or SSTL-15 Class II output.
- (4) Column I/O supports PCI/PCI-X with an on-chip clamping diode. Row I/O supports PCI/PCI-X with an external clamping diode.
- (5) Column I/O banks support LVPECL I/O standards only for input clock operation. Differential clock inputs in column I/O use $V_{CCCLKIN}$.
- (6) Column I/O banks support LVDS outputs using two single-ended output buffers and external one-resistor (LVDS_E_1R) and a three-resistor (LVDS_E_3R) network.
- (7) Row I/O banks support RSDS and mini-LVDS I/O standards using a dedicated LVDS output buffer without a resistor network.
- (8) Column I/O banks support RSDS and mini-LVDS I/O standards using two single-ended output buffers with one-resistor (RSDS_E_1R and mini-LVDS_E_1R) and three-resistor (RSDS_E_3R and mini-LVDS_E_3R) networks.

 For detailed electrical characteristics of each I/O standard, refer to the *DC and Switching Characteristics of HardCopy III Devices* chapter in volume 2 of the *HardCopy III Device Handbook*.

HardCopy III I/O

HardCopy III devices contain up to 20 I/O banks, as shown in Figure 6-3. Row I/O banks contain true differential input and output buffers and banks with dedicated circuitry to support differential standards at speeds up to 1.25 Gbps.

Figure 6-3. I/O Banks for HardCopy III Devices (Note 1), (2), (3), (4), (5), (6), (7), (8), (9)



Notes to Figure 6-3:

- (1) There are 12 I/O banks for the 484-pin package, 16 I/O banks for the 780-pin package, and 20 I/O banks for the 1152- and 1517-pin packages.
- (2) Differential HSTL and SSTL outputs are not true differential outputs. They use two single-ended outputs with the second output programmed as inverted.
- (3) Column I/O differential HSTL and SSTL inputs use LVDS differential input buffers without differential OCT support.
- (4) Column I/O supports LVDS outputs using single-ended buffers and external resistor networks.
- (5) Column I/O supports PCI/PCI-X with an on-chip clamping diode. Row I/O supports PCI/PCI-X with an external clamping diode.
- (6) Differential clock inputs on column I/O use $V_{CCCLKIN}$. All outputs use the corresponding bank V_{CCIO} .
- (7) Row I/O supports the dedicated LVDS output buffer.
- (8) Column I/O banks support LVPECL-only standards for input clock operation.
- (9) Figure 6-3 is a top view of the silicon die that corresponds to a reverse view for flip chip packages. It is a graphical representation only.
- (10) Single-ended inputs and outputs are not allowed when true differential IO (DPA and non-DPA) exist in a given I/O bank.

Every I/O bank in HardCopy III devices can support high-performance external memory interfaces with dedicated circuitry. The I/O pins are organized in pairs to support differential standards. Each I/O pin pair can support both differential input and output buffers. The only exceptions are the `clk1`, `clk3`, `clk8`, `clk10`, `PLL_L1_clk`, `PLL_L4_clk`, `PLL_R1_clk`, and `PLL_R4_clk` pins which support differential input operations only.



For more information about the number of channels available for the LVDS I/O standard, refer to the *High-Speed Differential I/O Interface with DPA in HardCopy III Devices* chapter in volume 1 of the *HardCopy III Device Handbook*.

HardCopy III I/O Banks

The I/O pins in HardCopy III devices are arranged in groups called modular I/O banks. Depending on the device package, the number of I/O banks varies. The size of each bank can also vary. Table 6-3 lists the I/O count per bank for all available pin packages.

Table 6-3. I/O Count Per Bank for HardCopy III Devices (Part 1 of 2) (Note 1)

Bank	Device Package Pin Count			
	484	780	1152	1517
1A	24	32	48	50
1C	24	26	42	42
2A	24	32	48	50
2C	24	26	42	42
3A	—	40	40	48
3B	—	—	24	48
3C	24	24	32	32
4A	—	40	40	48
4B	—	—	24	48
4C	24	24	32	32
5A	24	32	48	50
5C	24	26	42	42
6A	24	32	48	50
6C	24	26	42	42
7A	—	40	40	48
7B	—	—	24	48
7C	24	24	32	32
8A	—	40	40	48
8B	—	—	24	48
8C	24	24	32	32
Total Banks	12	16	20	20

Table 6-3. I/O Count Per Bank for HardCopy III Devices (Part 2 of 2) (Note 1)

Bank	Device Package Pin Count			
	484	780	1152	1517
Total I/O Pins	288	488	744	880 (2)

Notes to Table 6-3:

- (1) These numbers include dedicated clock pins and regular I/O pins.
- (2) The HardCopy III F1517-pin package supports less I/O count than the Stratix III F1517-pin package. Therefore, always set HardCopy companion devices in your Quartus II project to ensure proper mapping.

HardCopy III I/O Structure

The I/O element (IOE) in HardCopy III devices contains a bidirectional I/O buffer and I/O registers to support a complete embedded bidirectional SDR or DDR transfer. Figure 6-3 shows that certain I/O banks support certain I/O standards. The IOEs are located in I/O blocks around the periphery of the HardCopy III device.

The HardCopy III bidirectional IOE also supports features such as:

- MultiVolt I/O interface
- Dedicated circuitry for external memory interface
- Input delay
- Four output-current strength settings for single-ended I/Os
- Four slew rate settings for both single-ended and differential I/Os
- Four output delay settings for single-ended I/Os
- Six I/O delay settings for single-ended I/Os
- Optional bus-hold
- Optional pull-up resistor
- Optional open-drain output
- Optional on-chip series termination with or without calibration
- Optional on-chip parallel termination with calibration
- Optional on-chip differential termination
- Optional PCIe clamping diode

MultiVolt I/O Interface

The HardCopy III architecture supports the MultiVolt I/O interface feature that allows HardCopy III devices in all packages to interface with systems of different supply voltages.

The V_{CCIO} pins can be connected to a 1.2-, 1.5-, 1.8-, 2.5-, or 3.0-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply. (For example, when V_{CCIO} pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems.)

The HardCopy III V_{CCPD} power pins must be connected to a 2.5- or 3.0-V power supply. Using these power pins to supply the pre-driver power to the output buffers increases the performance of the output pins. Table 6-4 lists HardCopy III MultiVolt I/O support.

Table 6-4. MultiVolt I/O Support for HardCopy III Devices (Note 1)


V_{CCIO} (V)	Input Signal (V)						Output Signal (V)					
	1.2	1.5	1.8	2.5	3.0	3.3	1.2	1.5	1.8	2.5	3.0	3.3
1.2	✓	—	—	—	—	—	✓	—	—	—	—	—
1.5	—	✓	✓ (2)	—	—	—	—	✓	—	—	—	—
1.8	—	✓ (2)	✓	—	—	—	—	—	✓	—	—	—
2.5	—	—	—	✓	✓ (2)	✓ (2)	—	—	—	✓	—	—
3.0	—	—	—	✓	✓	✓ (2)	—	—	—	—	✓	—
3.3 (3)	—	—	—	—	—	—	—	—	—	—	—	—

Notes to Table 6-4:

- (1) HardCopy III devices do not support the 3.3-V I/O standard.
- (2) The pin current may be slightly higher than the default value. You must verify that the driving device's V_{OL} maximum and V_{OH} minimum voltages do not violate the applicable HardCopy III V_{IL} maximum and V_{IH} minimum voltage specifications.
- (3) Column I/O supports PCI/PCI-X with an on-chip clamping diode. Row I/O supports PCI/PCI-X with an external clamping diode.


3.3/3.0-V I/O Interface

Unlike Stratix III, HardCopy III I/O buffers do not support 3.3-V I/O standards. The maximum I/O voltage is 3.0-V. However, for 3.3-V LVTTTL, the output high voltage (V_{OH}), output low voltage (V_{OL}), input high voltage (V_{IH}), and input low voltage (V_{IL}) levels meet the 3.3-V LVTTTL standard of Stratix III devices. For 3.3V-LVCMOS, these parameters are compatible, except V_{OH} , which depends on V_{CCIO} .

 For more information about 3.3/3.0-V I/O interfaces, refer to *DC and Switching Characteristics of HardCopy III Devices* chapter in volume 2 of the *HardCopy III Device Handbook*.

To ensure device reliability and proper operation when interfacing with a 3.3-V I/O system using HardCopy III devices, it is important to make sure that the absolute maximum ratings of HardCopy III devices are not violated.


 For information about ensuring device reliability and proper operation, refer to the *DC and Switching Characteristics of HardCopy III Devices* chapter in volume 2 of the *HardCopy III Device Handbook*.

 Altera recommends performing IBIS simulation to determine that the overshoot and undershoot voltages are within the guidelines.

When using the HardCopy III device as a transmitter, you can use several techniques to limit the overshoot and undershoot at the I/O pins, such as using slow slew rate and series termination, but they are not required. Transmission line effects that cause large voltage deviation at the receiver are associated with impedance mismatch between the driver and transmission line. By matching the impedance of the driver to


the characteristic impedance of the transmission line, you can significantly reduce overshoot voltage. You can use a series termination resistor placed physically close to the driver to match the total driver impedance to transmission line impedance. HardCopy III devices support series on-chip termination (OCT) for all LVTTTL/LVCMOS I/O standards in all I/O banks.

When using the HardCopy III device as a receiver, a technique you can use to limit the overshoot, though not required, is using a clamping diode (on-chip or off-chip). HardCopy III devices provide an optional on-chip PCIe clamping diode for column I/O pins. You can use this diode to protect I/O pins against overshoot voltage.

 For more information about absolute maximum rating and maximum allowed overshoot during transitions, refer to the *DC and Switching Characteristics of HardCopy III Devices* chapter in volume 2 of the *HardCopy III Device Handbook*.

The following features are identical to those in Stratix III devices:

- External memory interface
- High-speed differential I/O with DPA support
- Four levels of pre-emphasis for LVDS transmitters
- Four levels of differential output voltage for LVDS transmitters
- Output current strength
- Slew rate control
- Output buffer delay
- Open-drain output
- Bus hold
- Pull-up resistor


 For more information about particular features, refer to the *Stratix III Device I/O Features* chapter in volume 1 of the *Stratix III Device Handbook*.

On-Chip Termination Support and I/O Termination Schemes

HardCopy III devices support the same termination schemes and on-chip termination (OCT) architecture as Stratix III devices. I/O termination provides impedance matching and helps maintain signal integrity while on-chip termination saves board space and reduces external component costs.

HardCopy III devices support on-chip series termination (R_S) with or without calibration, parallel (R_T) with calibration, dynamic series and parallel termination for single-ended I/O standards, and on-chip differential termination (R_D) for differential LVDS I/O standards.

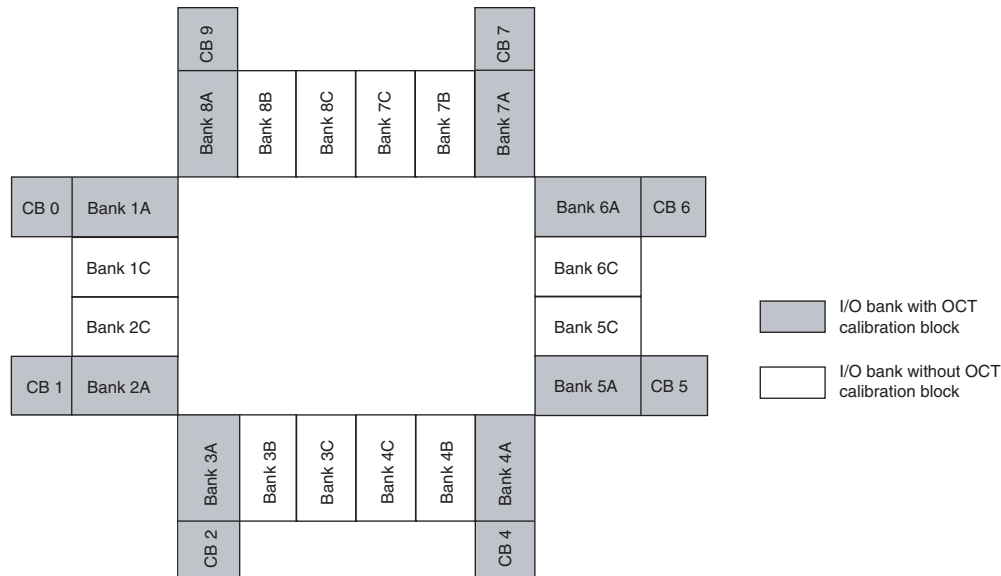
HardCopy III devices support OCT in all I/O banks by selecting one of the OCT I/O standards. Unlike Stratix III devices, which support up to ten calibration blocks, HardCopy III devices support up to eight OCT calibration blocks.

 For more information about termination schemes for I/O standards, refer to the *Stratix III Device I/O Features* chapter in volume 1 of the *Stratix III Device Handbook*.

OCT Calibration Block Location

Figure 6-4 shows the location of OCT calibration blocks in HardCopy III devices.

Figure 6-4. OCT Calibration Block Location in HardCopy III Devices (Note 1)



Note to Figure 6-4:

(1) Figure 6-4 is a top view of the silicon die that corresponds to a reverse view for flip-chip packages. It is a graphical representation only.

You can calibrate the I/O banks with any OCT calibration block with the same V_{CCIO} . Also, I/Os are allowed to transmit data during OCT calibration.

 For more information about the OCT calibration modes of operation and their implementation, refer to the *Stratix III Device I/O Features* chapter in volume 1 of the *Stratix III Device Handbook*.

Design Considerations

While HardCopy III devices feature various I/O capabilities for high-performance and high-speed system designs, there are several other considerations that require attention to ensure the success of those designs. These design practices are consistent with the design practices for Stratix III devices.

I/O Banks Restrictions

Each I/O bank can simultaneously support multiple I/O standards. The following sections provide guidelines for mixing non-voltage-referenced and voltage-referenced I/O standards in HardCopy III devices.

Non-Voltage-Referenced Standards

Each HardCopy III I/O bank has its own V_{CCIO} pins and can be powered by only one V_{CCIO} voltage supply level, either 1.2-, 1.5-, 1.8-, 2.5-, or 3.0-V. An I/O bank can simultaneously support any number of input signals with different I/O standard assignments, as shown in Table 6-4. For example, an I/O bank with a 2.5-V V_{CCIO} setting can support 2.5-V standard inputs and outputs and 3.0-V LVCMOS inputs (not output or bidirectional pins).

For output signals, a single I/O bank supports non-voltage-referenced output signals that are driving at the same voltage as V_{CCIO} . Because an I/O bank can only have one V_{CCIO} value, it can only drive out that one value for non-voltage-referenced signals.

Voltage-Referenced Standards

To accommodate voltage-referenced I/O standards, each HardCopy III device's I/O bank, such as 1A and 1C, supports separate V_{REF} pins feeding its individual V_{REF} bus. You cannot use the V_{REF} pins as generic I/O pins. Thus, if an I/O bank does not use any voltage-referenced I/O standards, the V_{REF} pin for that I/O bank must be tied to V_{CCIO} or GND. Each bank can only have a single V_{CCIO} voltage level and a single V_{REF} voltage level at a given time.

An I/O bank featuring single-ended or differential standards can support voltage-referenced standards as long as all voltage-referenced standards use the same V_{REF} setting.

For performance reasons, voltage-referenced input standards use their own V_{CCPD} level as the power source. This feature allows you to place voltage-referenced input signals in an I/O bank with a V_{CCIO} of 2.5 or below. For example, you can place HSTL-15 input pins in an I/O bank with a 2.5-V V_{CCIO} .

Voltage-referenced bidirectional and output signals must be the same as the I/O bank's V_{CCIO} voltage. For example, you can only place SSTL-2 output pins in an I/O bank with a 2.5-V V_{CCIO} .

Mixing Voltage-Referenced and Non-Voltage-Referenced Standards

An I/O bank can support both non-voltage-referenced and voltage-referenced pins by applying each of the rule sets individually. For example, an I/O bank can support SSTL-18 inputs and 1.8-V inputs and outputs with a 1.8-V V_{CCIO} and a 0.9-V V_{REF} . Similarly, an I/O bank can support 1.5-V standards, 1.8-V inputs (but not outputs), and HSTL and HSTL-15 I/O standards with a 1.5-V V_{CCIO} and 0.75-V V_{REF} .

Non-Socket Replacement and I/O Resource Availability

HardCopy III devices offer non-socket replacement of the FPGA devices. Non-socket replacement requires a board re-design. Table 6-5 lists the non-socket replacement options.



To ensure I/O resource availability, refer to the *Mapping Stratix III Device Resources to HardCopy III Devices* chapter in volume 2 of the *HardCopy III Device Handbook*.

Table 6-5. Non-Socket Replacement I/O Resource Availability for HardCopy III Devices

HardCopy III Device	Stratix III Prototype Device	HardCopy III I/O Pins	Stratix III I/O Pins	HardCopy III Full Duplex LVDS Pairs	Stratix III Full Duplex LVDS Pairs
HC325WF484	EP3SL110--F780	296	488	48	56
	EP3SL150--F780	296	488	48	56
	EP3SE110--F780	296	488	48	56
	EP3SL200--H780	296	488	48	56
	EP3SE260--H780	296	488	48	56
	EP3SL340--H1152	296	744	48	88
HC325FF484	EP3SL110--F780	296	488	48	56
	EP3SL150--F780	296	488	48	56
	EP3SE110--F780	296	488	48	56
	EP3SL200--H780	296	488	48	56
	EP3SE260--H780	296	488	48	56
	EP3SL340--H1152	296	744	48	88
HC325WF780	EP3SL340--H1152	392	744	48	88
HC325FF780	EP3SL340--H1152	488	744	56	88

Document Revision History

Table 6-6 lists the revision history for this chapter.

Table 6-6. Document Revision History

Date	Version	Changes
January 2011	3.1	<ul style="list-style-type: none"> ■ Updated Table 6-5 and Table 6-2. ■ Updated the “Differences Between HardCopy III ASICs and Stratix III FPGAs” section. ■ Added Figure 6-1 and Figure 6-2. ■ Added Table 6-1. ■ Minor text edits.
June 2009	3.0	<ul style="list-style-type: none"> ■ Added Note 10 to Figure 6-1 ■ Replaced Note 3 in Table 6-7 ■ Added new section “Non-Socket Replacement and I/O Resource Availability” on page 6-21 ■ Added Table 6-9
December 2008	2.0	<ul style="list-style-type: none"> ■ Updated “Introduction” ■ Updated “Voltage-Referenced Standards” on page 6-11 ■ Made minor editorial changes
May 2008	1.0	Initial release.