9. Hot Socketing and Power-On Reset in HardCopy III Devices

HIII51009-2.0

This chapter contains information about hot-socketing specifications, power-on reset (POR) requirements, and their implementation in HardCopy® III devices.

HardCopy III devices offer hot socketing, which is also known as hot plug-in or hot swap, and power sequencing support without the use of any external devices. You can insert or remove a HardCopy III device or a board in a system during system operation without causing undesirable effects to the running system bus or the board that was inserted into the system.

The hot-socketing feature also removes some of the difficulty when you use HardCopy III devices or PCBs that contain a mixture of 3.0-, 2.5-, 1.8-, 1.5-, and 1.2-V devices. With the HardCopy III hot-socketing feature, you no longer need to ensure a proper power-up sequence for each device on the board.

The HardCopy III hot-socketing feature provides:

- Board or device insertion and removal without external components or board manipulation
- Support for any power-up sequence
- Non-intrusive I/O buffers to system buses during hot insertion

This chapter also discusses hot-socketing specification, its implementation, and the POR circuitry in HardCopy III devices. The POR circuitry keeps the devices in the reset state until the power supplies are within operating range.

HardCopy III Hot-Socketing Specifications

HardCopy III devices are hot-socketing compliant without the need for any external components or special design requirements. Hot-socketing support in HardCopy III devices has the following advantages:

- You can drive the device before power-up without damaging it.
- I/O pins remain tri-stated during power-up. The device does not drive out before or during power-up and does not affect other buses in operation.
- You can insert or remove a HardCopy III device from a powered-up system board without damaging or interfering with normal system and board operation.

Devices Can Be Driven Before Power-Up

You can drive signals into I/O pins, dedicated input pins, and dedicated clock pins of HardCopy III devices before or during power-up or power-down without damaging the device. HardCopy III devices support power-up or power-down of all power supplies in any sequence to simplify system level design.

HardCopy III ASICs power up to user mode instantly, while Stratix III devices require configuration after power up. If you design a board where a HardCopy III device will replace the Stratix III device, check that all the important signals in your design are ready before the HardCopy III device enters usermode. For example: clocks, resets, and control signals. Otherwise, your system's operation may be erratic until the proper reset and initialization of your design is performed.

For more information about the HardCopy III power up behavior, refer to the *Matching Stratix III Power and Configuration Requirements with HardCopy III Devices* chapter in volume 2 of the *HardCopy III Device Handbook*.

I/O Pins Remain Tri-Stated During Power-Up

A device that does not support hot socketing may interrupt system operation or cause contention by driving out before or during power-up. In a hot-socketing situation, the HardCopy III device's output buffers are turned off during system power-up or power-down. Also, the HardCopy III device does not drive out until the device is in user mode and working within recommended operating conditions.

Insertion or Removal of a HardCopy III Device from a Powered-Up System

Devices that do not support hot socketing can short power supplies when powered up through the device signal pins. This irregular power-up can damage both the driving and driven devices and can disrupt card power-up.

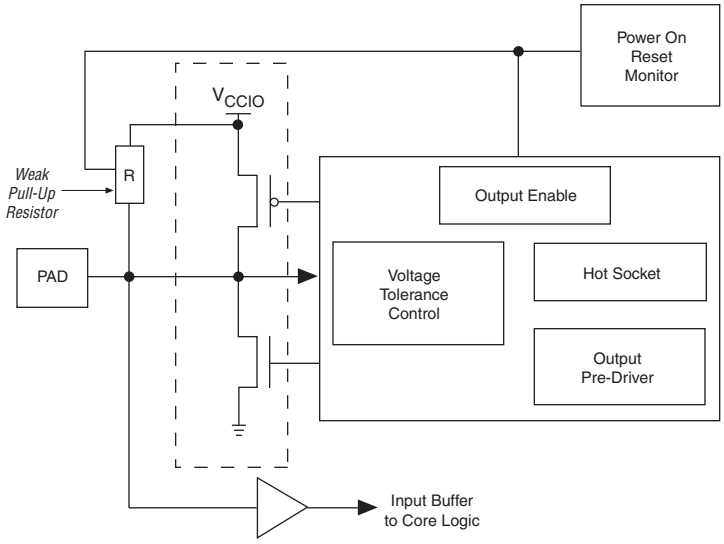
A HardCopy III device may be inserted into (or removed from) a powered-up system board without damaging or interfering with system board operation. You can power-up or power-down all power supplies in any sequence, as long as they are all ramped up to full rail before the HardCopy III device starts to communicate with other devices on the board. This requirement is discussed in "Power-On Reset Circuitry" on page 9–4. HardCopy III devices are immune to latch-up when performing hot socketing.

For more information about the hot-socketing specification, refer to the *DC and Switching Characteristics of HardCopy III Devices* chapter in volume 2 of the *HardCopy III Handbook*.

Hot-Socketing Feature Implementation in HardCopy III Devices

The hot-socketing feature turns off the output buffer during power-up and power-down of the V_{CC}, V_{CCIO}, V_{CCPGM}, or V_{CCPD} power supplies. Each I/O pin has the circuitry shown in Figure 9–1.

Figure 9–1. Hot-Socketing Circuit Block Diagram for HardCopy III Devices

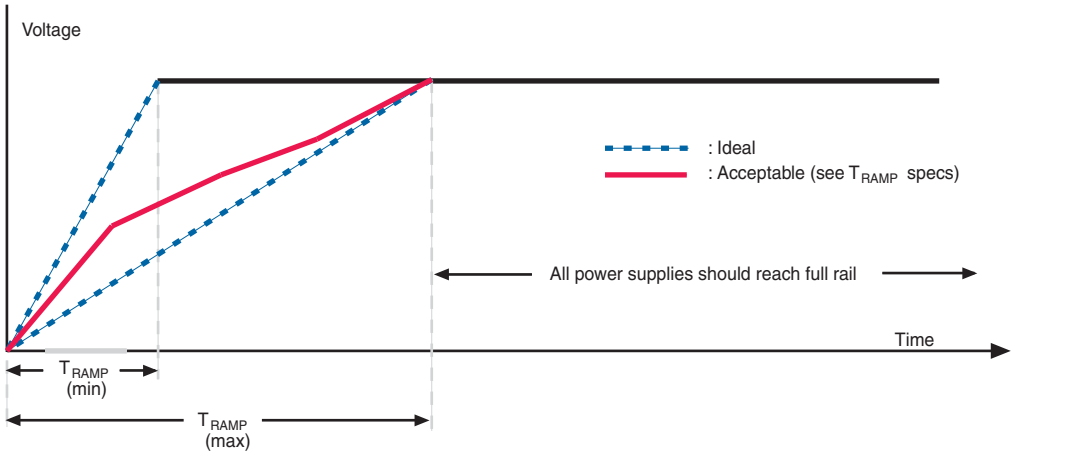


The POR circuit monitors the voltage level of power supplies (V_{CC}, V_{CCL}, V_{CCPD}, and V_{CCAUX}) and keeps the I/O pins tri-stated until the device is in user mode. The weak pull-up resistor (R) in the HardCopy III input/output element (IOE) keeps the I/O pins from floating. The voltage tolerance control circuit permits the I/O pins to be driven by external voltages before V_{CC}, V_{CCIO}, V_{CCPGM}, and/or V_{CCPD} supplies are powered, and it prevents the I/O pins from driving out when the device is not in user mode.

Power-On Reset Circuitry

A power-on reset event occurs if all the POR-monitored power supplies, shown in Figure 9–1 reach the recommended operating range within a certain period of time (specified as power supply ramp time, T_{RAMP}). Figure 9–2 shows the power supply specification. All power supplies' voltages have to rise monotonically within T_{RAMP}. This ensures the voltage levels do not remain indeterminate for a long time during power-up.

Figure 9–2. Power Supply Ramp Behavior

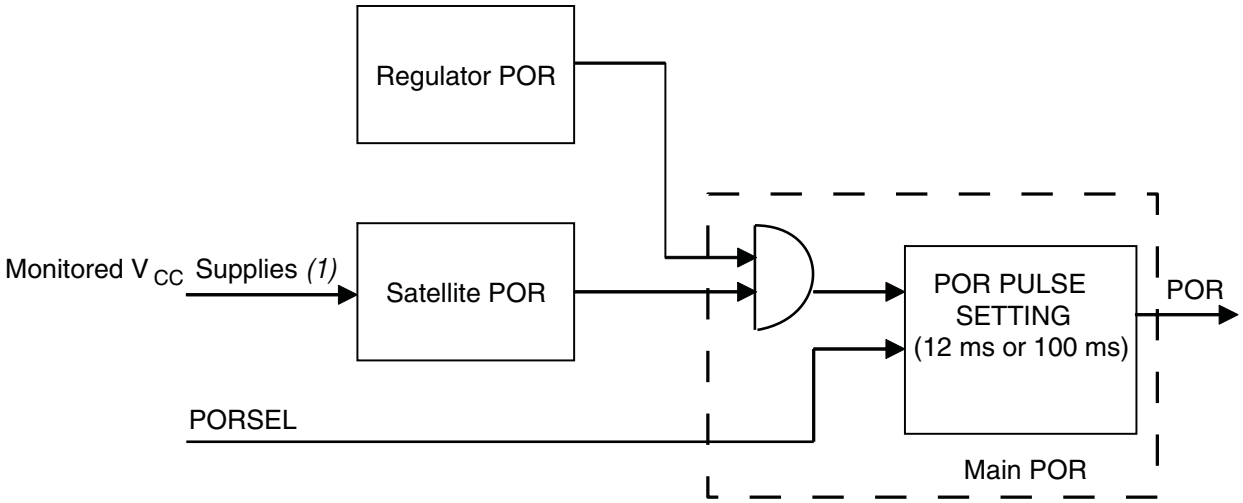


HardCopy III devices provide a dedicated input pin (PORSEL) to select a T_{RAMP} range from 50 µ to 4 ms or from 50 µ to 100 ms for all power supplies to ramp up. When the PORSEL pin is connected to ground, the T_{RAMP} can be from 50 µ to 100 ms. When the PORSEL pin is set to high, the T_{RAMP} can be from 50 µ to 4 ms.

The POR block consists of a regulator POR, satellite POR, and main POR to check the power supply levels for proper device operation. The regulator POR monitors the internal reference voltage for the temperature sensing diode and POR. The satellite POR monitors V_{CC}, V_{CCL}, V_{CCPD}, V_{CCPGM}, and V_{CCAUX} power supplies to ensure proper device operation. It also checks for functionality of I/O level shifters powered by V_{CCPD} and V_{CCPGM} during power-up mode. The main POR collects signals from both regulator and satellite PORs and generates POR pulse according to the PORSEL signal. A simplified block diagram of the POR block is shown in Figure 9–3.

All configuration-related dedicated and dual function I/O pins must be powered by V_{CCPGM}.

Figure 9–3. Simplified POR Block Diagram



Note to Figure 9–3:

(1) For more details about these supplies, refer to Table 9–1.

The POR circuit monitors the power supplies specified in Table 9–1.

Table 9–1. Power Supplies Monitored by the POR Circuitry

Power Supply	Description	Setting (V)
V_{CC}	I/O registers power supply	0.9
V_{CCL}	Core voltage power supply	0.9
V_{CCAUX} *(1)*	Power supply for temperature sensing diode and POR circuitry	2.5
V_{CCPD}	I/O pre-driver power supply	2.5, 3.0
V_{CCPGM}	Configuration pins power supply	1.8, 2.5, 3.0

Note to Table 9–1:

(1) This power supply is for the auxiliary power supply in Stratix III devices.

The POR circuit does not monitor the power supplies listed in Table 9–2.

Table 9–2. Power Supplies Not Monitored by the POR Circuitry

Voltage Supply	Description	Setting (V)
V_{CCIO}	I/O power supply	1.2, 1.5, 1.8, 2.5, 3.0
V_{CCA_PLL}	PLL analog global power supply	2.5
V_{CCD_PLL}	PLL digital power supply	0.9
V_{CC_CLKIN}	PLL differential clock input power supply (top and bottom I/O banks only)	2.5
V_{CCBAT}	Battery back-up power supply for design security volatile key storage	N/A

The POR signal pulse width is selectable using the PORSEL input pin. When PORSEL is set to low, the POR signal pulse width is set to 100 ms minimum. When the PORSEL is set to high, the POR signal pulse width is set to minimum. The POR specification is designed to ensure that all circuits in the HardCopy III device are at certain known states during power up.

Because not all power supplies are monitored by POR, ensure that the power supplies are fully ramped up before the device starts to communicate with other devices on the system.

Regardless of the voltage level of these power supplies, a HardCopy III device continues to enter user-mode. One difference between Stratix III and HardCopy III devices is that Stratix III devices allow more time for power supplies to ramp up during the configuration phase, before the device enters user mode. HardCopy III devices, however, can enter user mode and release CONF_DONE within 12 ms or 100 ms. Therefore, you should always verify the voltage level of the power supply system before the HardCopy III device starts to run.

For more information about the POR specification, refer to the *DC and Switching Characteristics of HardCopy III Devices* chapter in volume 2 of the *HardCopy III Handbook*.

Conclusion

HardCopy III devices are hot-socketing compliant and allow successful device power-up without the need for any power sequencing. The POR circuitry keeps the devices in the reset state until the power supply voltage levels are within operating range.

Document Revision History

Table 9–3 shows the revision history for this chapter.

Table 9–3. Document Revision History

Date	Version	Changes Made
January 2011	2.1	■ Updated PORSEL and POR signal pulse information. ■ Updated "Devices Can Be Driven Before Power-Up" on page 9–1.
December 2008	2.0	■ Updated "Power-On Reset Circuitry" on page 9–4. ■ Updated Table 9-1. ■ Updated Figure 9-1. ■ Updated Figure 9-3. ■ Made minor editorial changes.
May 2008	1.0	Initial release.