

Altera FPGAs for radar and advanced sensors

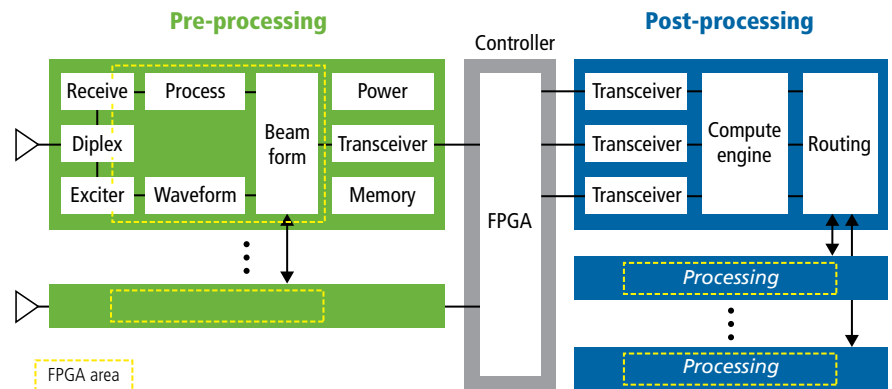
State-of-the-art military sensors have unprecedented requirements in the volume of environmental data to be measured and processed. To handle this data and provide *actionable intelligence* to the soldier as soon as possible, Altera® FPGAs offer the best combination of logic and digital signal processing (DSP) density, high-speed transceivers, and power vs. performance design flexibility. To support an efficient design process, our FPGAs also enable a high-assurance, low-risk design flow.

Active Electronically Scanned Arrays (AESA) are a powerful technology for creating highly adaptive steerable beams able to track multiple targets. In order to take full advantage of a system's steering capabilities, designers move as much signal processing capability as possible into the forward radiating elements of the system. This may include waveform creation and compression, beam forming, correlation, and pre-processing.

As more of these functions are performed in optimized, parallel FPGA logic, beam-forming algorithms and waveform adaptivity can be accelerated, increasing system reaction times.

Altera Stratix® series high-density FPGAs offer a rich feature set that optimizes radar system performance. High logic density allows more functions on a single chip. Increased DSP elements streamline matrix mathematical functions and increase flexibility. Highly flexible 18-bit x 18-bit multipliers can be split into 9-bit x 9-bit elements, or combined into power- and logic-efficient 54-bit multipliers for floating point operations. High-speed transceivers allow fast telemetry streaming on a variety of serial digital interface standards (SerialLite II, PCI Express, Gigabit Ethernet, etc.).

Making Active Electronically Scanned Arrays more flexible



Power and heat advantages with Stratix FPGAs

Never before have system designers had direct control over the power consumption and heat dissipation of their programmable logic.

The Altera design flow offers five advantages in letting you select the optimal balance of power and performance in your system:

1. Optimized silicon process at 65 nm
2. Altera's patented Programmable Power Technology, available in Stratix III FPGAs and providing the ability to channel power to the critical logic path where it is needed, and reduce power where it is not needed
3. Between 0.9-V and 1.1-V FPGA core voltage, with the ability to trade power versus performance

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4. The powerful Altera Quartus® II design environment, providing the intelligence to dynamically terminate unused power connections
5. The ability to optimize power routing in your design using Quartus II software

Using an example design space at right, an FPGA designer has a flexible design space to tailor an application for both power and performance requirements.

Simplified design flow with Quartus II software and SOPC Builder

The complexity of radar and sensor system design is increasing almost exponentially. Designers need tools that reduce compile times, manage design risk, and streamline test and verification time, yet still offer powerful DSP design features.

Getting started on Altera design tools is easy with our Quartus II design software. Quartus II software is the only design environment that includes everything you need for the entire cycle of FPGA and ASIC design for radar and advanced sensor systems. The software includes DSP Builder block set support for The MathWorks MATLAB, SOPC Builder, as well as capabilities including Altera's PowerPlay early power estimator, incremental placement and routing, power optimization, and TimeQuest timing analyzer.

Altera solutions for modern radar and sensor systems

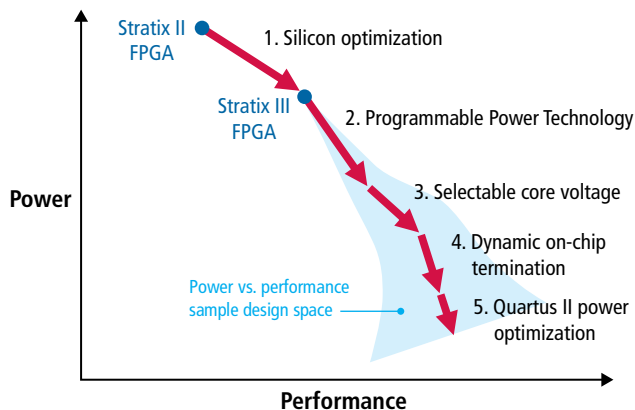
- Stratix series FPGAs—maximum functionality at minimum power across the broadest range of radar and electronic warfare platforms
- HardCopy® series structured ASICs—seamless migration path from Stratix series FPGAs to achieve the lowest power implementations for handheld and sensor applications with up to 70% additional lower core power than the FPGA
- Partnership with White Electronic Designs Corporation (WEDC) for multi-chip module (MCM) and smaller form factor packaging
- Radar white papers at www.altera.com/literature/lit-wp.jsp:
 - *Optimizing Radar and Advanced Sensor Functions with Altera FPGAs*
 - *Radar Prototyping with the HardCopy Design Flow*

Want to dig deeper?

Visit our website or call your local Altera sales representative today to learn more about how you can solve your radar and sensor design challenges with Altera FPGAs.

www.altera.com/military

Demonstrating power/performance advantages



Designers have five ways to optimize power and performance for radar and sensor applications

Altera design flow advantages for advanced sensor systems

Requirement	Altera device solution
DDR3 memory	Quartus II software with 65-nm FPGAs provide the only design solution to support DDR3 memory, with twice the density and 50% more bandwidth than DDR2
Timing support	Only TimeQuest timing analyzer offers native support for Synopsis Design Constraint (SDC) standard for timing analysis
Fast compile times	<ul style="list-style-type: none"> • Common design benchmarks show that Altera designs compile twice as fast as those of the nearest competitor at 65 nm • Quartus II software is the only design environment with full 64-bit support on Windows OS, supporting more memory (>2 Gbytes) for faster compile times • Altera's simple design partitioning allows for incremental compile and up to 70% reduction in recompile time
Power analysis and programmability	<ul style="list-style-type: none"> • Quartus II PowerPlay power analyzer gives you trusted power estimates with unbiased consistency • Scalable, reversible fast Fourier transform (FFT)\inverse FFT (IFFT) with bit exact C models
Large selection of signal processing and serial interface IP	<ul style="list-style-type: none"> • Floating point math support and performance benchmarks in GFlops and GFlops per Watt • IP cores for Serial RapidIO®, PCI Express, 10G Ethernet, Fibre Channel, and many more standards

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