Intel® Agilex™ F-Series FPGA and SoC FPGA Product Table

PRODUCT LINE		AGF 006	AGF 008	AGF 012	AGF 014	AGF 019	AGF 022	AGF 023	AGF 027
Resources	Logic elements (LEs)	573,480	764,640	1,178,525	1,437,240	1,918,975	2,208,075	2,308,080	2,692,760
	Adaptive logic modules (ALMs)	194,400	259,200	399,500	487,200	650,500	748,500	782,400	912,800
	ALM registers	777,600	1,036,800	1,598,000	1,948,800	2,602,000	2,994,000	3,129,600	3,651,200
	High-performance crypto blocks	0	0	0	0	2	0	2	0
	eSRAM memory blocks	0	0	2	2	1	0	1	0
	eSRAM memory size (Mb)	0	0	36	36	18	0	18	0
	M20K memory blocks	2,844	3,792	5,900	7,110	8,500	10,900	10,464	13,272
	M20K memory size (Mb)	56	74	115	139	166	212	204	259
	MLAB memory count	9,720	12,960	19,975	24,360	32,525	37,425	39,120	45,640
	MLAB memory size (Mb)	6	8	12	15	20	23	24	28
	I/O PLL	12	12	16	16	10	16	10	16
	Variable-precision digital signal processing (DSP) blocks	1,640	2,296	3,743	4,510	1,354	6,250	1,640	8,528
	18 x 19 multipliers	3,280	4,592	7,486	9,020	2,708	12,500	3,280	17,056
	Single-precison or half-precision tera floating point operations per second (TFLOPS)	2.5 / 5.0	3.5 / 6.9	6.0 / 12.0	6.8 / 13.6	2.0 / 4.0	9.4 / 18.8	2.5 / 5.0	12.8 / 25.6
	Maximum EMIF x72	2	2	4	4	2	4	2	4
Maximum Available Device Resources	Maximum differential (RX or TX) pairs	192	288	384	384	240	384	240	384
	AIB interfaces	2	2	2	2	4	4	4	4
	Memory devices supported	DDR4 and QDR IV							
	Secure data manager	AES-256/SHA-256 bitstream encryption/authentication, physically unclonable function (PUF), ECDSA 256/384 boot code authentication, side channel attack protection							
	Hard processor system	Quad-core 64 bit Arm Cortex-A53 up to 1.50 GHz with 32 KB I/D cache, NEON coprocessor, 1 MB L2 cache, direct memory access (DMA), system memory management unit, cache coherency unit, hard memory controllers, USB 2.0x2, 1G EMAC x3, UART x2, serial peripheral interface (SPI) x4, I2C x5, general purpose timers x7, watchdog timer x4							
Tile Resources	F-Tile	PCI Express(PCIe) hard IP block (Gen4 x16) or Bifurcateable 2x PCIe Gen4 x8 (EP) or 4x Gen4 x4 (RP) Transceiver channel count : 16 channels at 32 Gbps (NRZ) /12 channels at 58 Gbps (PAM4) - RS & KP FEC Advanced networking support: - Bifurcatable 400 GbE hard IP block (10/25/50/100/200/400 GbE FEC/PCS/MAC) - Bifurcatable 200 GbE hard IP block (10/25/50/100/200 Gbps FEC/PCS) IEEE 1588 v2 support PMA direct							
	E-Tile	Transceiver channel count : Up to 24 channels at 28.9 Gbps (NRZ) / 12 channels at 57.8 Gbps (PAM4) - RS & KP FEC[1] Networking support : - 400GbE (4 x 100GbE hard IP blocks (10/25 GbE FEC/PCS/MAC)) IEEE 1588 v2 support PMA direct							
	P-Tile	PCIe hard IP block (Gen4 x16) or Bifurcateable 2x PCIe Gen4 x8 (EP) or 4x Gen4 x4 (RP) SR-IOV 8PF / 2kVF VirtIO support Scalable IOV							

Note 1: Only 4 instances of KP-FEC are supported when using 100GE MAC

Intel® Agilex™ F-Series FPGA and SoC FPGA Product Table

PRODUCT LINE	AGF 006	AGF 008	AGF 012	AGF 014	AGF 019	AGF 022	AGF 023	AGF 027
F- Tile - Package Options and I/O Pins				**GPIO (LVDS) / F-Tile 32G NRZ (58G PAM4)**				
1546A (37.5 mm x 34 mm, 0.92 mm Hex)	384(192)/32(24)	384(192)/32(24)						
2340A (45 mm x 42 mm, 0.92 mm Hex)	576(288)/32(24)	576(288)/32(24)	744(372)/32(24)	744(372)/32(24)	480(240)/32(24)	480(240)/32(24)	744(372)/32(24)	744(372)/32(24)
3184C (56 mm x 45 mm, 0.92 mm Hex)					480(240)/64(48)	480(240)/64(48)	720(360)/64(48)	720(360)/64(48)
E-Tile and P-Tile - Package Options and I/O Pins				**GPIO (LVDS) / E-Tile 28.9G NRZ (57.8G PAM4) / P-Tile 16G PCIe**				
2486A (55 mm x 42.5 mm, 1.0 mm Hex)			768(384)/16(8)/16	768(384)/16(8)/16				
2581A (52.5 mm x 40.5 mm, 0.92/0.94 mm Hex)[1]					480(240)/24(12)/32	624/(312)/24(12)/32	480(240)/24(12)/32	624(312)/24(12)/32

[1] Conditional migration path from AGF 019/023 to AGF 022/027 devices