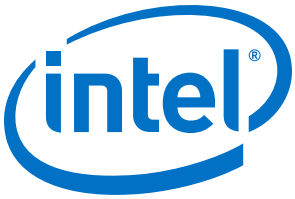

RapidIO Intel FPGA IP Core Release Notes

Attention: The RapidIO Intel FPGA IP is part of a product obsolescence and support discontinuation schedule.

For the schedule, refer to the Product Discontinuation Notice PDN2025.

For new designs, Intel recommends that you use other IPs with equivalent functions. To see a list of available IPs, refer to the Intel® FPGA IP Portfolio web page.

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Contents

1. RapidIO Intel FPGA IP Core Release Notes

If a release note is not available for a specific IP version, the IP has no changes in that version. For information on IP update releases up to v18.1, refer to the *Intel® Quartus® Prime Design Suite Update Release Notes*.

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.

The IP version (X.Y.Z) number may change from one Intel Quartus Prime software version to another. A change in:

- X indicates a major revision of the IP. If you update your Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

Related Information

- Intel Quartus Prime Design Suite Update Release Notes
- Introduction to Intel FPGA IP Cores
- RapidIO Intel FPGA IP User Guide
- Errata for the RapidIO Intel FPGA IP in the Knowledge Base

1.1. RapidIO Intel FPGA IP v19.2.0

Table 1. v19.2.0 2020.09.28

Intel Quartus Prime Version	Description	Impact
20.3	Discontinued support for RapidIO Intel FPGA IP.	There is no further development or customer support for this IP starting from next Intel Quartus Prime software version.

1.2. RapidIO Intel FPGA IP Core v18.0

Table 2. Version 18.0 May 2018

Description	Impact	Notes
Added Intel Cyclone® 10 GX device support.	—	
Added Xcelium* simulator support.	—	
Renamed RapidIO IP core to RapidIO Intel FPGA IP core per Intel rebranding.	—	

Related Information

- RapidIO Intel FPGA IP Core User Guide
- Errata for RapidIO IP core in the Knowledge Base

1.3. RapidIO IP Core v15.1

Table 3. Version 15.1 November 2015

Description	Impact	Notes
Added new parameter **Packet-Not-Accepted to Link Request timeout**. This parameter specifies whether or not the IP core enters a Fatal Error state if it sends a `packet-not-accepted` control symbol and then does not receive any `link-request` control symbol from the RapidIO link partner within the period of time indicated in the VALUE field of the PLTCTRL register at offset 0x120. By default, for backward compatibility, this parameter is turned on.	The default value of this parameter turns on the feature, which is always on in the previous version of the IP core. Turning off this parameter changes the IP core behavior.	

Related Information

- RapidIO MegaCore Function User Guide
- Errata for RapidIO IP core in the Knowledge Base

1.4. RapidIO IP Core v15.0

Table 4. Version 15.0 May 2015

Description	Impact	Notes
The IP core loses lane synchronization when a lane receives three errored characters. Previously the IP core lost lane synchronization after receiving two errored characters on a lane.	Lane synchronization is slightly more robust.	

Table 5. RapidIO IP Core Signal Changes

Signals added or modified in version 15.0.

Old Signal Name	New Signal Name	Notes
—	`no_sync_indicator`	When this new output signal is low, it indicates at least one lane is not synchronized.

Related Information

- RapidIO MegaCore Function User Guide
- Errata for RapidIO IP core in the Knowledge Base

1.5. RapidIO IP Core v14.1

Table 6. Version 14.1 December 2014

Description	Impact	Notes
The Quartus II software v14.1 requires that you specify a device if your IP core targets the Arria 10 device family. If you do not specify your target Arria 10 device, the IP Upgrade tool insists that your IP core requires upgrade, but does not clarify the reason.	You must ensure that you specify a device for your v14.0 Arria 10 Edition IP core variation and regenerate it in the Quartus II software v14.1.	

Related Information

- RapidIO MegaCore Function User Guide
- Errata for RapidIO IP core in the Knowledge Base

1.6. RapidIO IP Core v14.0 Arria 10 Edition

Table 7. Version 14.0 Arria 10 Edition August 2014

Description	Impact	Notes
Verified in the Quartus II software v14.0 Arria 10 Edition. (Added support for Arria 10 devices). RapidIO IP core variations that target an Arria 10 device have the following differences from the variations that target earlier device families.	Upgrading your existing IP core from a previous release of the Quartus II software requires migrating it to the Arria 10 device family. To migrate your IP core to the Arria 10 device family, you must regenerate the IP core manually in the Quartus II v14.0 Arria 10 Edition software and reconnect it in your design.	
Arria 10 variations require that you instantiate and connect a TX transceiver PLL IP core and a reset controller in your design.	Upgrading your existing IP core from a previous release of the Quartus II software requires migrating it to the Arria 10 device family. To migrate your IP core to the Arria 10 device family, you must regenerate the IP core manually in the Quartus II v14.0 Arria 10 Edition software and reconnect it in your design.	The new interface signals are listed in the RapidIO IP Core Signal Changes table.
Arria 10 variations do not require that you instantiate and connect a dynamic reconfiguration controller. Instead, if you turn on the new parameter **Enable transceiver dynamic reconfiguration**, these variations have an internal reconfiguration controller that the user accesses through an Avalon-MM interface.	Upgrading your existing IP core from a previous release of the Quartus II software requires migrating it to the Arria 10 device family. To migrate your IP core to the Arria 10 device family, you must regenerate the IP core manually in the Quartus II v14.0 Arria 10 Edition software and reconnect it in your design.	The new interface signals are listed in the RapidIO IP Core Signal Changes table.
If a RapidIO IP core that targets an Arria 10 device includes an I/O Logical layer Avalon-MM slave interface or an I/O Logical layer Avalon-MM master interface, the following conditions apply:	Unsupported parameters and parameter values are not available in the parameter editor or cause error messages that block IP core generation. If your IP core is already in this subset of variations, you can recreate the precise variation. However, you	

continued...

Description	Impact	Notes
• The IP core must include both an I/O Logical layer slave interface and an I/O Logical layer master interface. It cannot include one but not the other. • The I/O Logical layer slave module preserves transaction ordering between read and write operations. • The number of RX address translation windows is 16. • The number of TX address translation windows is 16.	must still regenerate the IP core manually and reconnect it in your design, because of other changes.	
If a RapidIO IP core that targets an Arria 10 device includes an I/O Maintenance Logical layer module, the following conditions apply: • The module has both master and slave ports. • The number of Maintenance transmit address translation windows is 16. • The module supports both reception and transmission of `port-write` requests, or supports neither.	Unsupported parameters and parameter values are not available in the parameter editor or cause error messages that block IP core generation. If your IP core is already in this subset of variations, you can recreate the precise variation. However, you must still regenerate the IP core manually and reconnect it in your design, because of other changes.	
A RapidIO IP core that targets an Arria 10 device supports both outbound and inbound DOORBELL messages, or it supports neither.	Unsupported parameters and parameter values are not available in the parameter editor or cause error messages that block IP core generation. If your IP core is already in this subset of variations, you can recreate the precise variation. However, you must still regenerate the IP core manually and reconnect it in your design, because of other changes.	
If a RapidIO IP core that targets an Arria 10 device supports DOORBELL messages, it preserves transaction order between DOORBELL messages and I/O write request transactions.	Unsupported parameters and parameter values are not available in the parameter editor or cause error messages that block IP core generation. If your IP core is already in this subset of variations, you can recreate the precise variation. However, you must still regenerate the IP core manually and reconnect it in your design, because of other changes.	
A RapidIO IP core that targets an Arria 10 device automatically synchronizes transmitted ackIDs.	Unsupported parameters and parameter values are not available in the parameter editor or cause error messages that block IP core generation. If your IP core is already in this subset of variations, you can recreate the precise variation. However, you must still regenerate the IP core manually and reconnect it in your design, because of other changes.	
In a RapidIO IP core that targets an Arria 10 device, the number of `link-request` attempts before declaring a fatal error is tied to 7.	Unsupported parameters and parameter values are not available in the parameter editor or cause error messages that block IP core generation. If your IP core is already in this subset of variations, you can recreate the precise variation. However, you must still regenerate the IP core manually and reconnect it in your design, because of other changes.	
In a RapidIO IP core that targets an Arria 10 device, the Physical layer receive and transmit buffers are 32 Kbytes each.	Unsupported parameters and parameter values are not available in the parameter editor or cause error messages that block IP core generation. If your IP core is	

continued...

Description	Impact	Notes
	already in this subset of variations, you can recreate the precise variation. However, you must still regenerate the IP core manually and reconnect it in your design, because of other changes.	
In the parameter editor for RapidIO IP core variations that target an Arria 10 device, the **Disable Destination ID checking by default** parameter is not available. Arria 10 variations do not check destination IDs, by default. However, support for controlling this feature through the IP core registers is available in all RapidIO IP core variations, as it was in the previous release.	Unsupported parameters and parameter values are not available in the parameter editor or cause error messages that block IP core generation. If your IP core is already in this subset of variations, you can recreate the precise variation. However, you must still regenerate the IP core manually and reconnect it in your design, because of other changes.	

Table 8. RapidIO IP Core Signal Changes

Signals added or modified in version 14.0 Arria 10 Edition.

Old Signal Name	New Signal Name	Notes
—	tx_bonded_clocks_ch<n>[5:0]	New interface to external TX PLL. Relevant for Arria 10 variations only. Individual transceiver channel clock signals. One signal (_ch<n>) for each RapidIO lane <n>.
—	reconfig_clk_ch<n>	New Arria 10 transceiver reconfiguration interface. This interface is available if you turn on **Enable transceiver dynamic reconfiguration** in the RapidIO parameter editor. Relevant for Arria 10 variations only. One signal (_ch<n>) for each RapidIO lane <n>.
—	reconfig_reset_ch<n>	
—	reconfig_read_ch<n>	
—	reconfig_write_ch<n>	
—	reconfig_address_ch<n>[9:0]	
—	reconfig_readdata_ch<n>[31:0]	
—	reconfig_waitrequest_ch<n>	
—	reconfig_writedata_ch<n>[31:0]	
—	tx_analogreset[N-1:0]	New interface to external reset controller. Relevant for Arria 10 variations only. N is the number of RapidIO lanes.
—	rx_analogreset[N-1:0]	
—	tx_digitalreset[N-1:0]	
—	rx_digitalreset[N-1:0]	
reconfig_togxb	Not present in Arria 10 variations.	Transceiver reconfiguration interface for Arria V, Cyclone V, and Stratix V variations. This interface is present only in Arria V, Cyclone V, and Stratix V variations (as supported in past and future versions of the Quartus II software). These signals are not present in Arria 10 variations.
reconfig_fromgxb	Not present in Arria 10 variations.	

Related Information

- RapidIO MegaCore Function User Guide
- Errata for RapidIO IP core in the Knowledge Base

1.7. RapidIO IP Core v14.0

Table 9. Version 14.0 June 2014

Description	Impact	Notes
Removed support for Cyclone III, Cyclone III LS, and Stratix III device families. The Quartus II software v14.0 does not support these device families.	If your IP core variation targets one of these device families, this change requires that you revise your IP core variation and regenerate it.	
Removed support for Physical-layer only variations.	If your IP core variation is no longer supported, and you choose to upgrade the IP core, this change requires that you revise your IP core variation and regenerate it.	
Removed support for external transceivers. All supported variations include configuration of the high-speed transceivers on the target device.	If your IP core variation is no longer supported, and you choose to upgrade the IP core, this change requires that you revise your IP core variation and regenerate it.	
Removed naming differences between Qsys-generated and non-Qsys-generated IP core variations. New variations generated in the 14.0 software, whether in Qsys or outside Qsys, use the port names previously identified with the Qsys variations.	If your IP core was generated in the MegaWizard Plug-In Manager flow, and you choose to upgrade the IP core, this change requires that you revise your IP core variation, upgrade it, and reconnect your IP core in your design.	
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.	This change is optional for v13.1 IP cores. However, IP upgrade is required for IP cores v13.0 and earlier.	

Related Information

- Introduction to Altera IP Cores
- RapidIO MegaCore Function User Guide
- Errata for RapidIO IP core in the Knowledge Base

1.8. RapidIO IP Core v13.1

Table 10. Version 13.1 November 2013

Description	Impact	Notes
Removed support for the Arria GX, Cyclone II, HardCopy II, HardCopy III, HardCopy IV E, HardCopy IV GX, Stratix II, and Stratix II GX device families.		

Related Information

- RapidIO MegaCore Function User Guide
- Errata for RapidIO IP core in the Knowledge Base

1.9. RapidIO IP Core v13.0

Table 11. Version 13.0 May 2013

Description	Impact	Notes
Added 2x mode for Arria V, Cyclone V, and Stratix V devices.		
Removed support for SOPC Builder design flow.		

Related Information

- RapidIO MegaCore Function User Guide
- Errata for RapidIO IP core in the Knowledge Base

2. RapidIO Intel FPGA IP User Guide Archives

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.

If an IP core version is not listed, the user guide for the previous IP core version applies.

IP Core Version	User Guide
18.0	RapidIO Intel FPGA IP User Guide
17.1	RapidIO IP Core User Guide
17.0	RapidIO IP Core User Guide
14.0	RapidIO MegaCore Function User Guide