Implementing Efficient Low-Power PCIe Interfaces with Low-Cost FPGAs

WP-01193-1.0 White Paper

A history of architectural and process advancements has enabled Altera® Cyclone® V FPGAs to be used in numerous low-cost and low-power applications in the industrial, automotive, military, communication and consumer markets, among others. This white paper outlines a real-life PCI Express® (PCIe®) Gen1x4 reference design including a DDR3 memory controller. It shows just how effective Cyclone V FPGAs are in minimizing total system cost while achieving performance and power targets.

Introduction

To illustrate the advantages of the Cyclone V FPGA family, a PCIe Gen1x4 reference design performing direct memory access (DMA) read and writes to an external DDR3 memory has been chosen as an example. (Figure 1 shows a high-level representation of this reference design.) The design includes a high-performance chaining DMA that transfers data between a Cyclone V GX FPGA and the internal memory or external memory. The reference design includes a Windows-based software application that sets up the DMA transfers, and enables evaluation of the performance of the PCIe protocol in Cyclone V devices. The resulting performance data is from the external DDR3 memory read and write commands via PCIe Gen1x4 through the host windows system. However, before presenting these performance results, the basics of low power process and technology in 28 nm, PCIe architecture fundamentals, and hard memory controller (HMC) innovations are reviewed.

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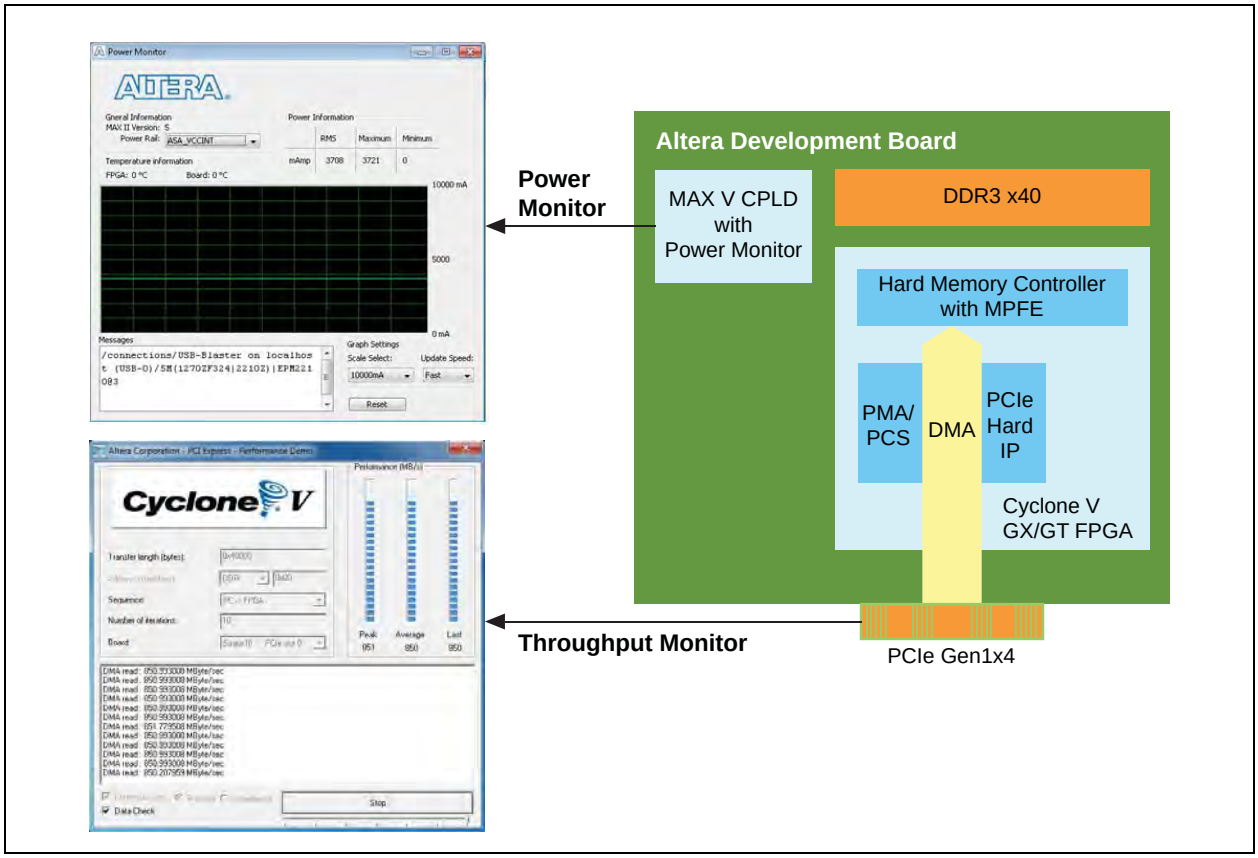
Figure 1. Overview of the PCIe Gen1x4-Based DDR3 Reference Design

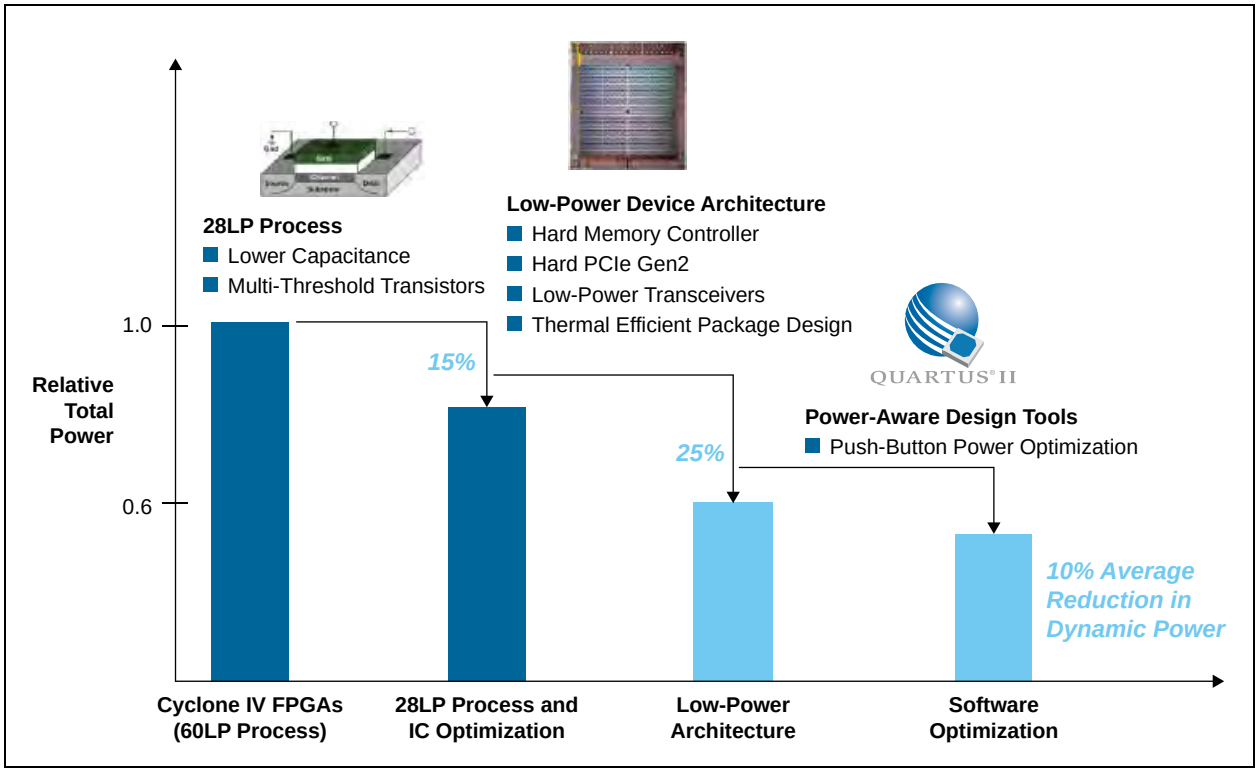


Low-Power 28 nm Advancements

Altera's low-cost Cyclone V FPGAs are manufactured using Taiwan Semiconductor Manufacturing Company (TSMC)'s 28 nm low power (28LP) process, which is designed to provide the lowest total power and is ideal for low standby power applications such as cellular baseband and portable devices. The 28LP process is based on silicon oxynitride (SiON) and is expected to provide twice the density and up to 25% lower power consumption than TSMCs' 40LP technology.

Relative to the previous-generation Cyclone IV FPGAs based on the 60LP process, Cyclone V FPGAs produce up to a 40% total relative power savings, as shown in Figure 2. The 28LP process features low gate capacitance to reduce active power gate capacitances. Overall, Cyclone V FPGAs utilize both architectural, process, and software enhancements to achieve the 40% power reduction. The use of low gate capacitance and multithreshold transistors with the 28LP process accounts for 15% of the power savings. A further 25% savings is obtained by architectural enhancements such as hardening the PCIe and memory controllers.

Figure 2. 28LP Process and Architecture Advancements in Cyclone V FPGAs



The reduced die area and associated capacitance translates to lower dynamic power. In addition, there have been enhancements in more thermally efficient package design and lower power designed transceivers that only consume a maximum of 88 mW per channel at 5 Gbps. Finally, due to advancements in synthesis, place and route algorithms within Quartus® II software using the PowerPlay early power estimator yield an additional 10% dynamic power savings. PowerPlay, Altera's power-driven synthesis- and power-driven place-and-route methodology, employs such techniques as clock gating and minimizing dynamic power by localizing high toggle nets.

Hard IP for PCIe in Cyclone V FPGAs

PCIe is a high-performance interconnect protocol for use in a variety of applications including network adapters, storage area networks (SANs), embedded controllers, graphic accelerator boards, and audio-video products. It is a packet-based, serial, point-to-point interconnect between two devices. Cyclone V devices support hard PCIe Gen1x4 at 2.5 Gbps per lane and PCIe Gen2x4 at 5.0 Gbps per lane configurations, thereby complying with PCIe Base Specification Revision 2.1.

Some of the basic features supported in the hard IP for PCIe in Cyclone V FPGAs include:

- Complete protocol stack including the transaction, data link, and physical layer, which are hardened in the device
- Multifunction support for up to eight endpoint functions
- Support of x1 and x4 Gen1 and Gen2 configurations for root ports and endpoints
- Dedicated 6 KB receive buffer

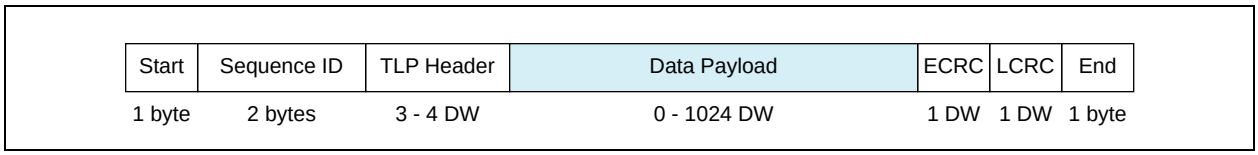
- Dedicated hard reset controller
- MegaWizard™ Plug-In Manager and Qsys support using the Avalon® Streaming (Avalon-ST) interconnect with a 64 bit or 128 bit interface to the application layer.

The flexibility, efficiency and extensive built-in functionality of the PCIe hard IP block allow designs to operate at near-theoretical throughput values. For example, the configuration in Figure 1 uses a PCIe Gen1x4 link. This 4-lane link operates at 2.5 Gbps per lane. Hence, aggregated over 4 lanes, the link would produce 1.25 Gbps throughput. However, PCIe uses 8B/10B encoding in which every byte of data is converted into a 10-bit data code. This coding overhead of 20% reduces the maximum theoretical throughput of the system on the PCIe side to 1 Gbps or 250 MB per lane. In addition, two factors limit maximum PCIe throughput:

- Transaction layer packet (TLP) format and data payload framing overhead
- Data link layer packets (DLLPs) and physical layer packets (PLPs) overhead

Figure 3 outlines the basic TLP frame format that controls the high-level transaction type from the transport protocol level.

Figure 3. PCIe TLP Format



The theoretical throughput of the PCIe data based on this TLP format can be expressed using the following equation:

$$\text{Throughput \%} = \frac{\text{Payload Size}}{\text{Payload Size} + \text{Overhead}}$$

The reference design demo uses a 256 byte payload size. Assuming a 3 dword TLP header, the maximum throughput then becomes (256/(256 + 20)) = 92%. Due to various other protocol overhead factors and DLLP/PLP overhead, the theoretical maximum throughput achievable is slightly less than the calculated 92%. Nonetheless, Cyclone V FPGAs with PCIe hard IP implementations are able to operate near the theoretical maximum speeds permitted by the protocol. Therefore, the maximum data throughput the demo can support between the host CPU and an FPGA via the PCIe link is:

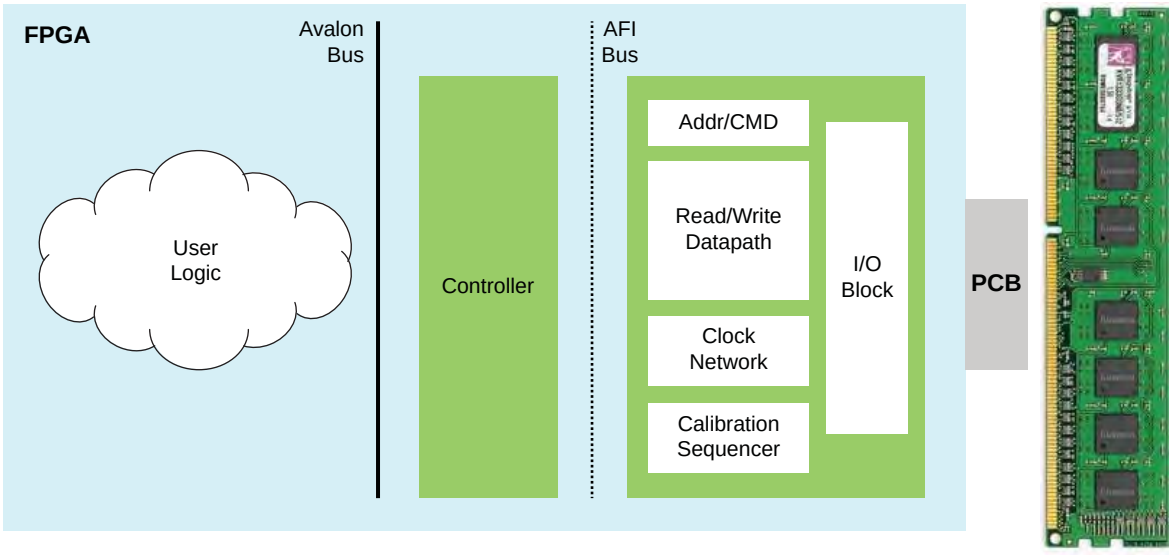
$$0.92 \times 1 \text{ Gbps} = 920 \text{ MBps}$$

Because the demo in Figure 1 not only transfers read and write operations via the PCIe link but also uses the external DDR3 hard memory interface, a similar theoretical maximum throughput calculation is required between the FPGA internal logic block and the external DDR3 memory that is located on the Cyclone V GX150 FPGA development board.

Flexible and Efficient External DDR3 HMC

Cyclone V FPGAs are able to support both soft and hard IP external memory interface solutions. Dedicated HMCs allow support for simplified design and low latency in comparison to the Cyclone V FPGA memories implemented using core logic. Figure 4 shows a simplified block diagram of the Cyclone V FPGA's memory interface.

Figure 4. Simplified Block Diagram of a Cyclone V Memory Interface



The memory interface is comprised of three parts:

- Multiport front end
- Controller
- Physical layer interface (PHY)

The multiport front-end logic allows up to six local interfaces from the core logic to access a controller. The controller translates Avalon read/write commands into memory Altera PHY Interface (AFI) commands. The PHY handles the detailed timing on the data path and the sequencer block within the PHY performs the calibration of the PHY at runtime (such as I/O delay chain settings for the DQ/DQS).

As with the PCIe link, it is necessary to calculate the maximum theoretical performance achievable between the FPGA core and the external memory. The performance as well as the efficiency of the memory controller must be considered. Efficiency for memories is defined as the percentage of bus utilization time that data is being transferred, or by the following expression:

$$\text{DDR3 Memory Efficiency} = \frac{\text{Number of Clock Cycles Transferring Data}}{\text{Total Clock Cycles}}$$

This equation can then be used to calculate the overall DDR3 to FPGA bandwidth. Total bandwidth is expressed as:

$$\text{Total DDR3 Bandwidth} = 40 \text{ bits} \times 400 \text{ MHz} \times 2 \text{ Clock Edges (DDR)} \times \text{Efficiency}$$

Assuming a typical DDR3 memory efficiency of 70%, this calculation produces a total aggregate bandwidth of 22.4 Gbps or 2.8 GBps. This bandwidth is significantly greater than the peak theoretical bandwidth between the FPGA and PCIe Gen1x4 link of 920 MBps, so the system bottleneck is determined by the PCIe-to-FPGA core link.

Reference Design with PCIe

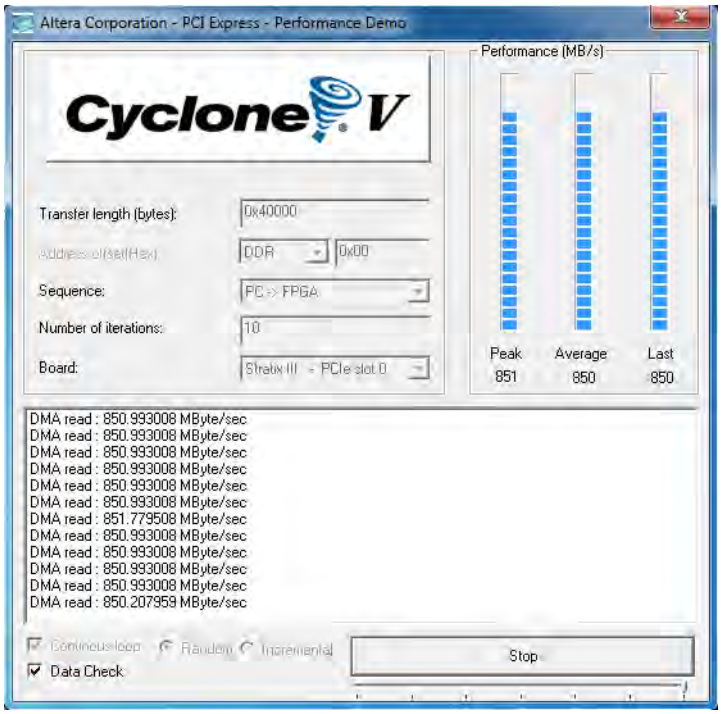
To this point, the performance metrics are theoretical maximum values. The Windows-based tool used in this design shows the actual performance of a PCIe Gen1x4 operation consisting of memory read and write operations to external DDR3 memory using the Altera HMC are shown. The configuration consists of a 150K-logic element (LE) Cyclone V GX FPGA development board (Figure 5) plugged into the PCIe slot of a PC system containing an Intel Core i7 Sandy Bridge E series processor.

Figure 5. Cyclone V GX FPGA Development Board

Through this host, a series of read and/or write operations to DDR3 are executed. The design can support simultaneous DMA read and DMA write transactions. The DMA write module implements write operations in which the data is transferred from the endpoint memory to the root complex (system memory) across the PCIe link. The DMA read module implements read operations in which data is transferred from the root complex (system memory) across the PCIe link to the endpoint memory.

Figure 6 shows the results of the DMA write performance results from the host. The actual throughput measurements are calculated by the Altera PCIe performance GUI. This GUI measures and reports the actual bandwidth of the PCIe link.

Figure 6. PCIe Performance GUI Results



For writes, the actual bandwidth is 850 MBps. With a theoretical maximum of 920 MBps, where the system performance bottleneck is located, the PCIe controller is achieving a 92% utilization or efficiency level. Metrics slightly lower than the theoretical maximum are due to maximum theoretical calculations that did not take into account the additional protocol overhead for DLLP and PLPs. This overhead marginally reduces the real throughput depending on the traffic transmitted.

Conversely, the measured bandwidth for the DMA read operation is 808 MBps. Read throughput is usually lower than write throughput because the data for read completions may be split into multiple packets rather than being returned in a single packet. The high efficiency of the HMC, which enables 32 bit data +8 bit error correcting code (ECC), can leverage the extra bandwidth to add ECC support for higher data integrity.

Conclusion

An efficient low-power PCIe interface can be easily implemented using a low-cost FPGA, such as a Cyclone V FPGA. By integrating hard IP blocks for both PCIe and DDR3 memory controller, Cyclone V FPGAs enable designers to easily implement low-power interfaces. These design examples clearly illustrate how efficient IP implementations of PCIe Gen1x4 and DDR3 can achieve bandwidth that is near to the theoretical maximum limits allowed by the protocol. In addition, Altera offers a wide range of hard and soft IP blocks for Cyclone V FPGAs with a combination of efficiency and high performance to meet customers' 28 nm low-cost solution needs.

Further Information

- Cyclone V FPGAs: Lowest System Cost and Power: www.altera.com/devices/fpga/cyclone-v-fpgas/cyv-index.jsp
- *Cyclone V Device Handbook*: www.altera.com/literature/hb/cyclone-v/cyclone5_handbook.pdf
- *Application Note: PCI Express High Performance Reference Design*: www.altera.com/literature/an/an456.pdf
- *White Paper: Using External Memory Interfaces to Achieve Efficient High-Speed Memory Solutions*: www.altera.com/literature/wp/wp-01169-high-speed-memory.pdf

Acknowledgements

- Elias Ahmed, Product Marketing Manager, Altera Corporation

Document Revision History

Table 1 shows the revision history for this document.

Table 1. Document Revision History

Date	Version	Changes
February 2013	1.0	Initial release.